A CAHNERS PUBLICATION INTERNATIONAL EDITION NOVEMBER 27, 1986

EDN

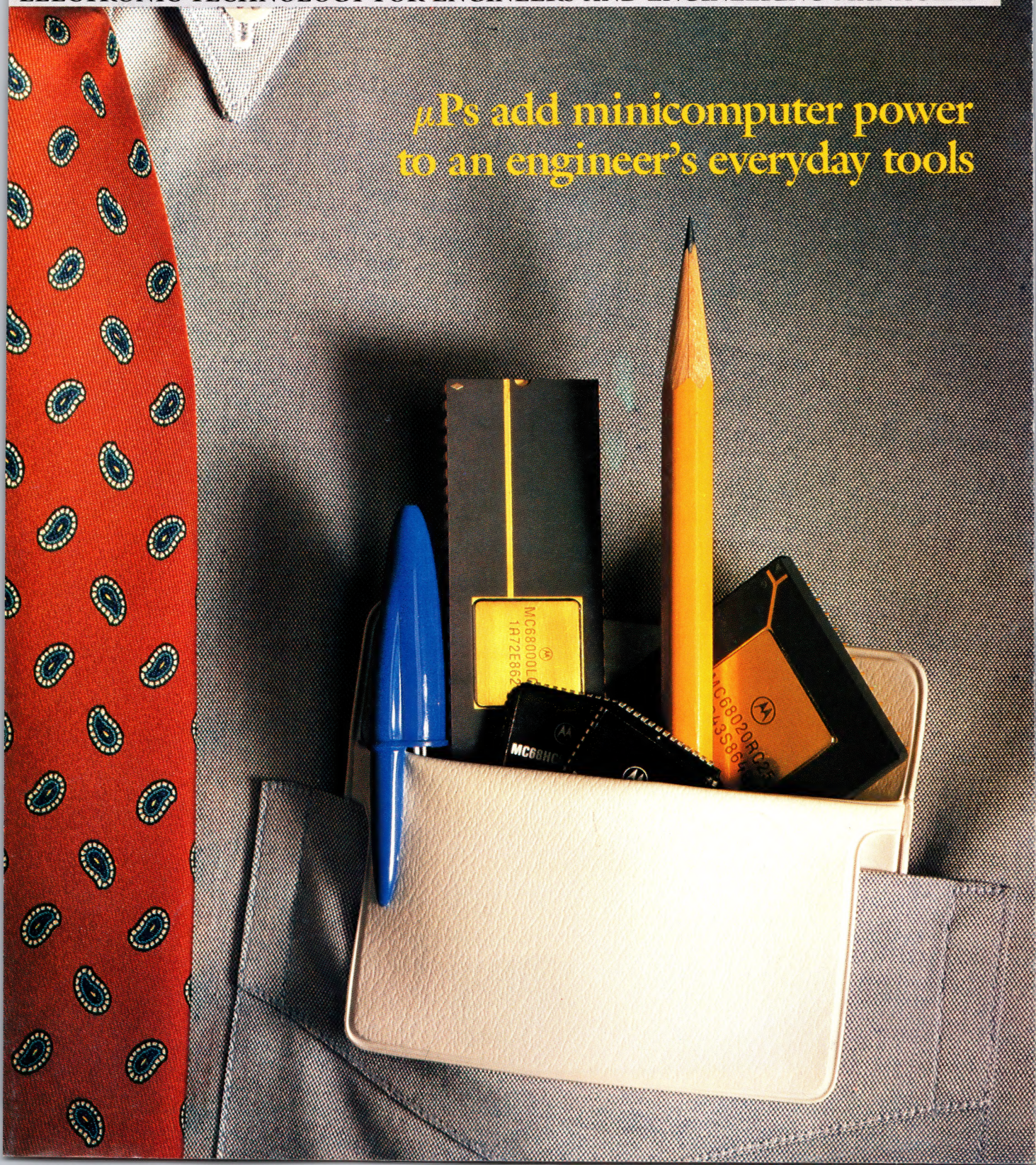
Thirteenth Annual μP/μC Chip Directory

ASIC verification systems speed prototype testing

Low-cost circuitry augments CRT-controller chip set

Digital optical encoders

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



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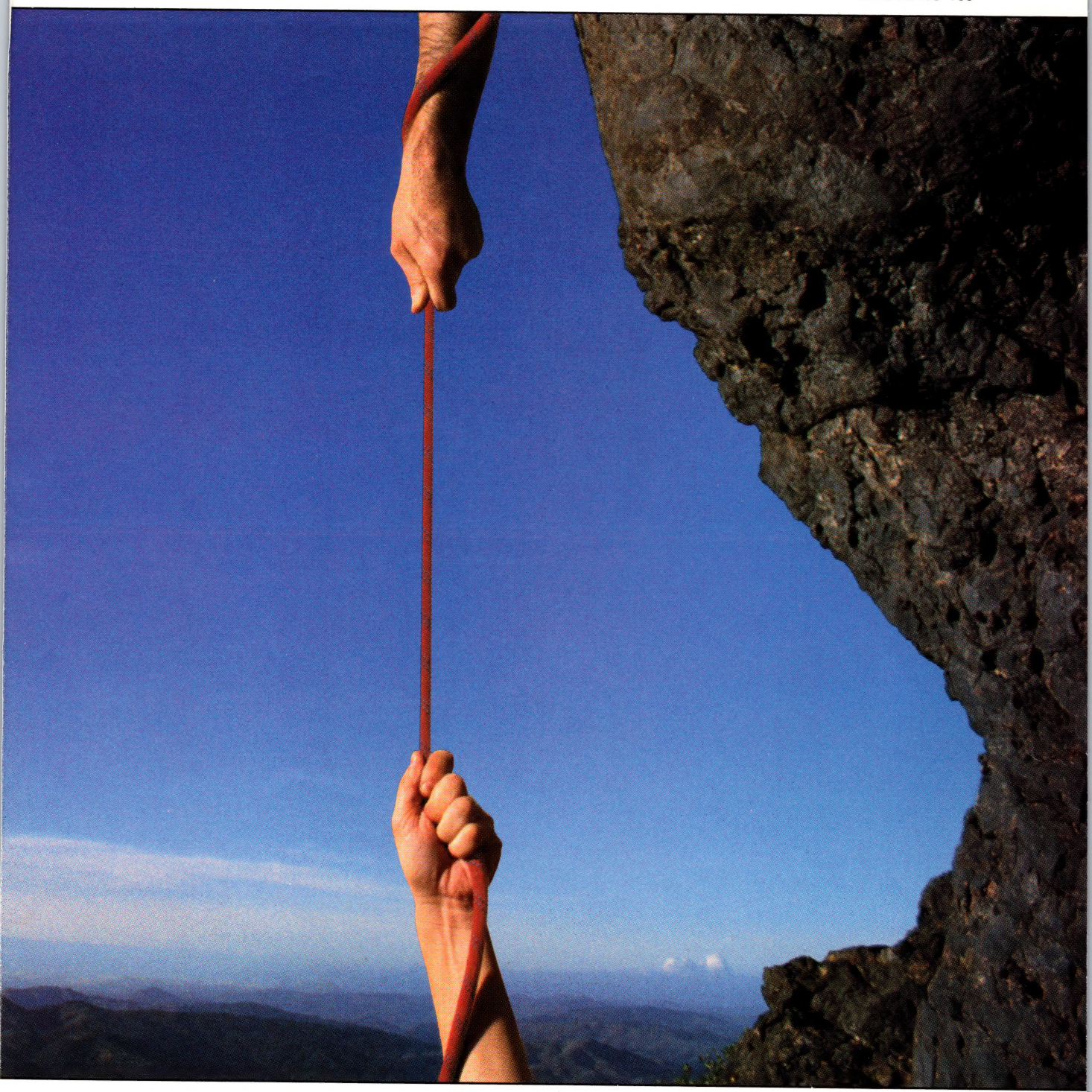

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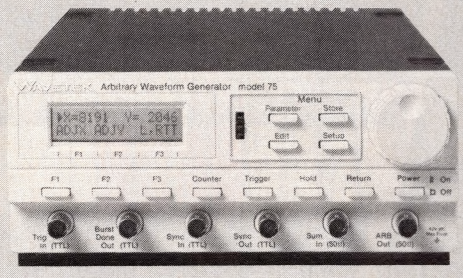
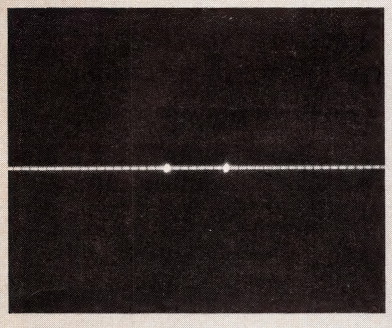
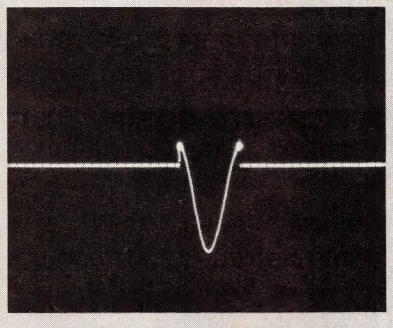
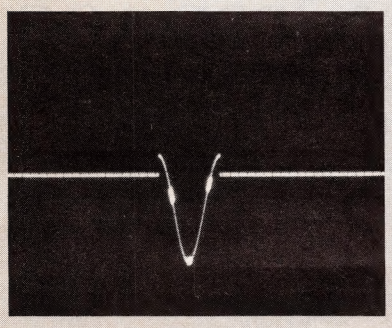




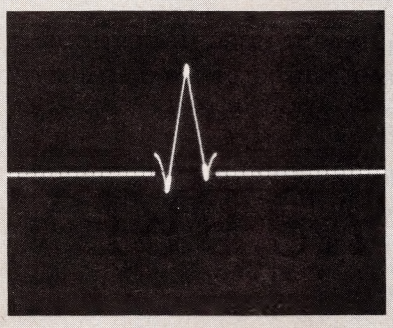
1. Place "thumbtack" markers.



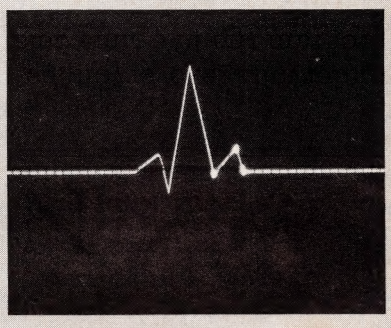
2. Insert standard waveform.



3. Reset "thumbtack" marker positions.



4. Stretch "rubberband" with edit cursor.

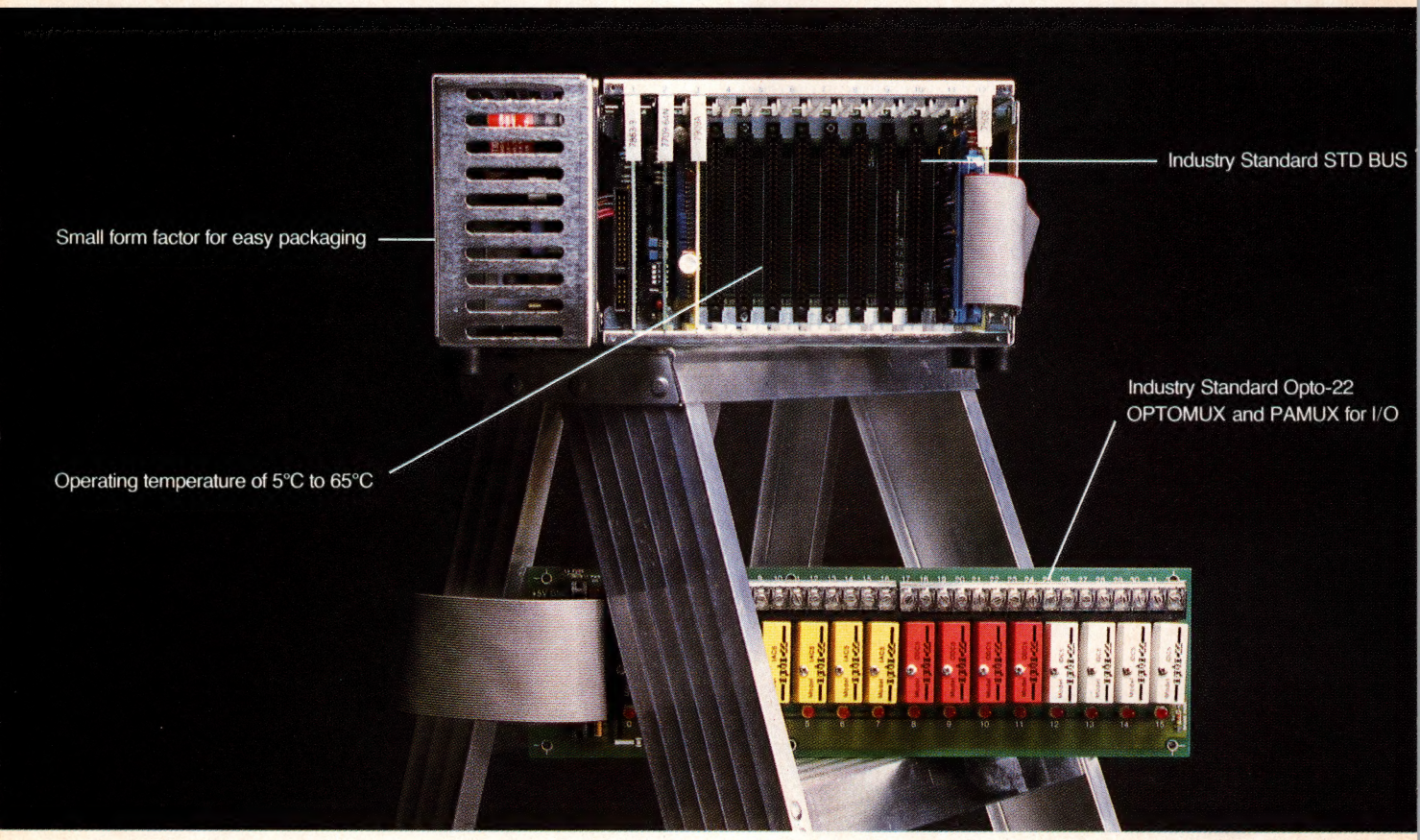


5. Move "thumbtacks" and complete waveform editing.

Circle 196 for Demonstration

Circle 157 for Literature

REAL-TIME MULTITASKING INDUSTRIAL CONTROL WITHOUT BEING LOCKED INTO A PROGRAMMABLE CONTROLLER



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EDN

November 27, 1986

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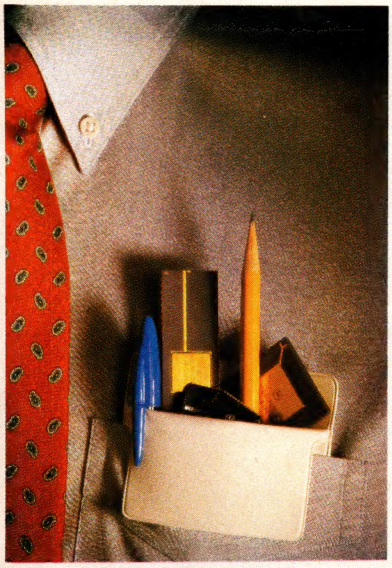

On the cover: *In this year's μP/μC Chip Directory, you'll find several new DSP chips; also μP cores are appearing in ASIC libraries. But the significant news is the ubiquitousness of two general-purpose μP families. See pg 102. (Cover concept by Staats Falkenberg & Partners with photography by Tomas Pantin, courtesy Motorola Inc)*

DESIGN FEATURES

Continued on page 7

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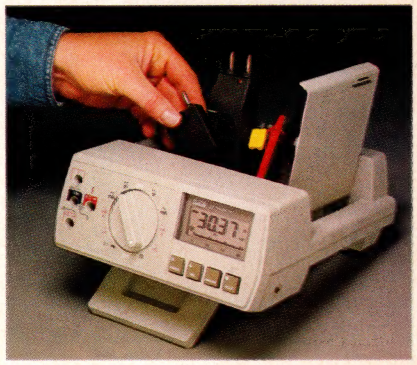

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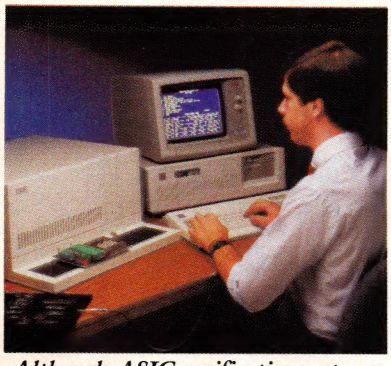

Although ASIC-verification systems all basically generate a stimulus and acquire and display results, they offer widely different user-interface features, test fixtures, and test-pattern-generation and data-analysis tools (pg 51).

TECHNOLOGY UPDATE

PRODUCT UPDATE

DESIGN IDEAS

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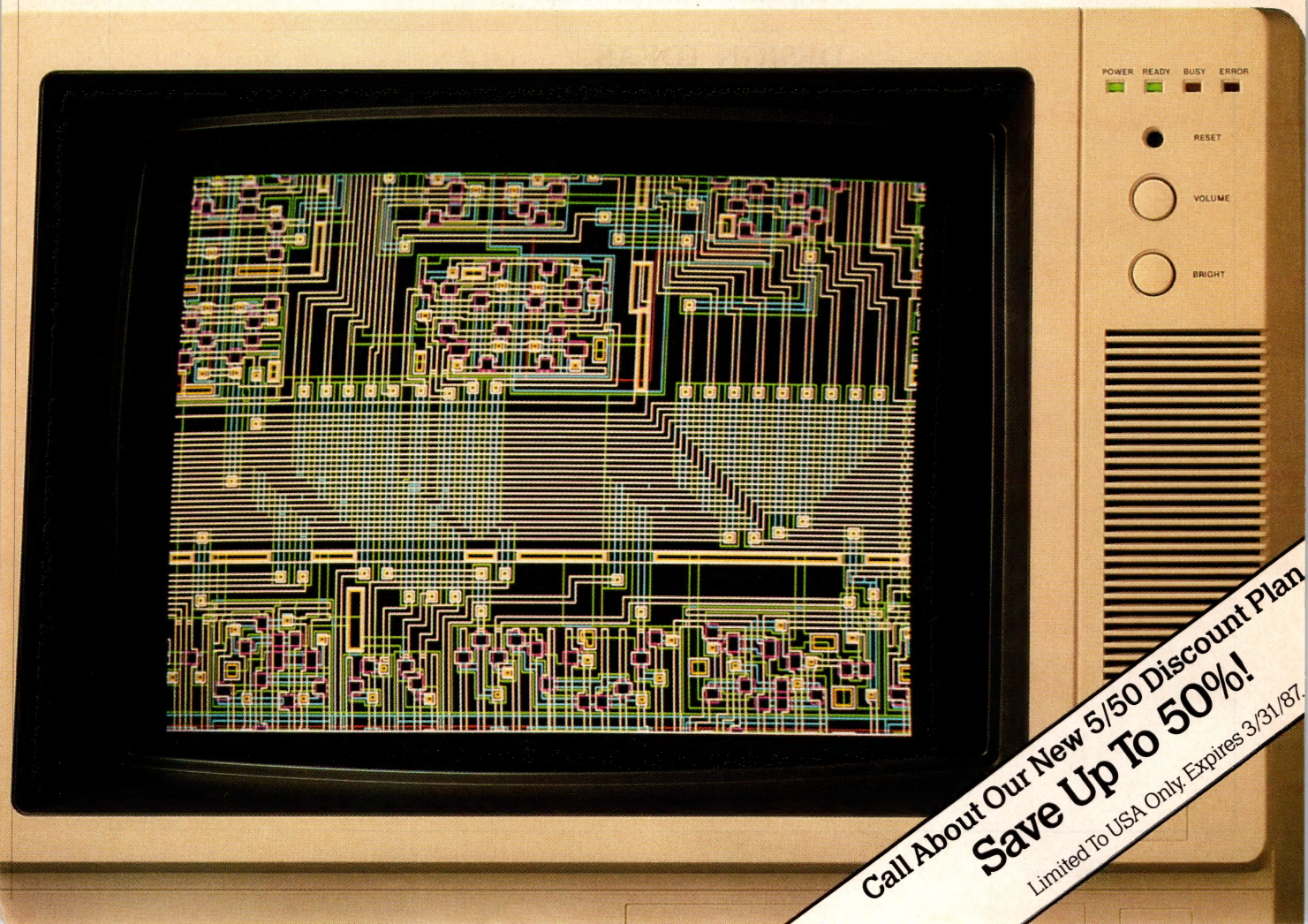

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National security means more than just defense against foreign powers, and redirecting the government's defense dollar needn't hurt engineers.

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GaAs IC market: Slower growth than expected . . . Use of position sensors to double in Europe by '95.

DEPARTMENTS

VBPA ABP

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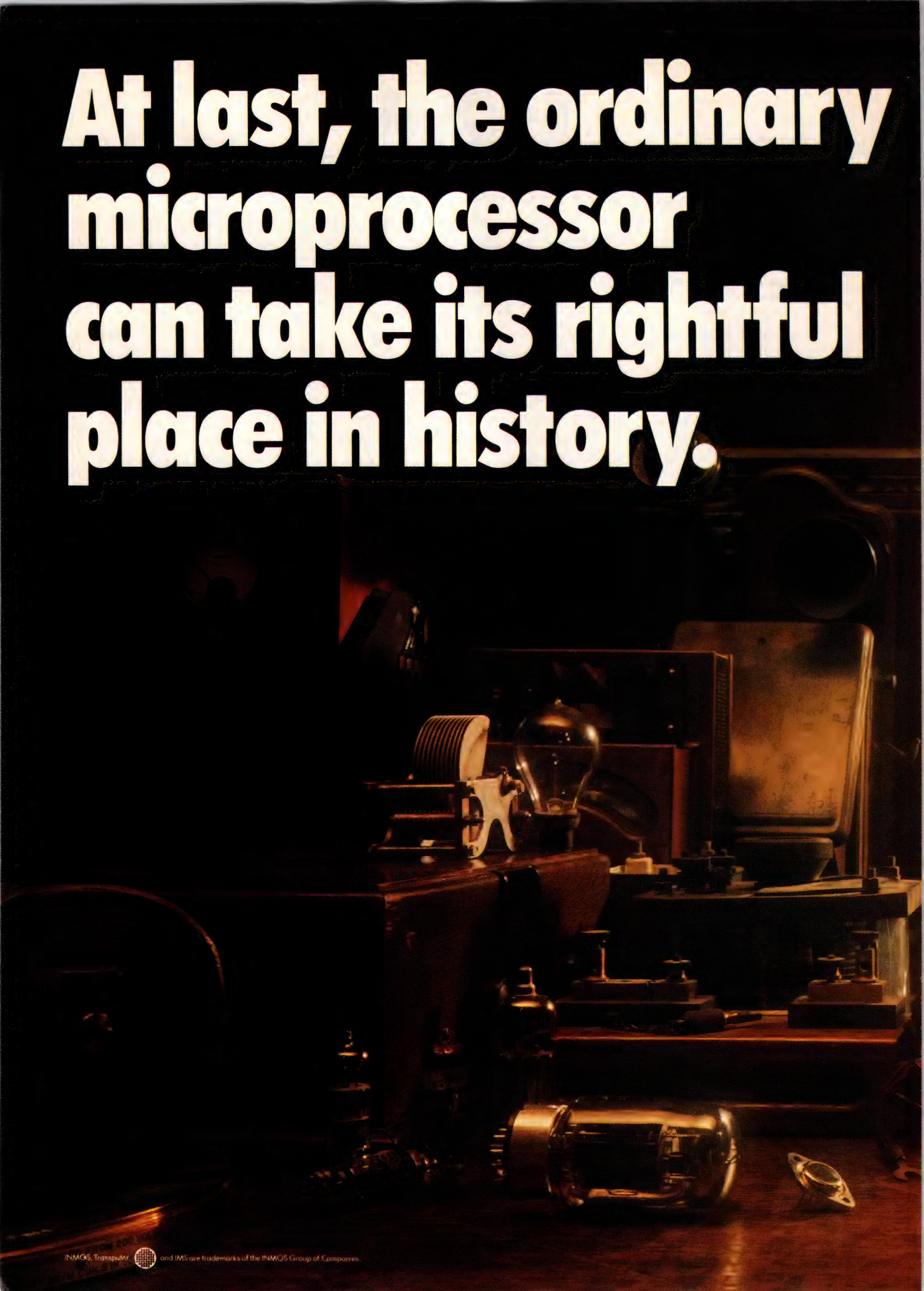
At last, the ordinary microprocessor can take its rightful place in history.



It had to happen—the conventional microprocessor has had its day. Relegated to the ranks of yesterday's devices by the new transputer family from INMOS. It's history in the making.

The IMS T414 transputer is a fast, easy-to-use VLSI component, integrating a 32-bit processor, four inter-transputer communication links, 2K bytes Static RAM, 32-bit memory interface and DRAM controller. All on a single CMOS chip—offering execution rates up to 10 MIPs.

While transputers excel in single-processor systems, their real power can be unleashed by connecting any number of transputers together via the high-speed serial links. Multi-transputer systems can deliver the performance you need today, and can be easily expanded in the future as your processing requirements increase.

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INMOS transputers are available now and have already found their way into companies who are evaluating, prototyping and manufacturing transputer-based systems. Applications include supercomputers, DSP, graphics, robotics, AI, distributed control systems, PC's, engineering workstations and many others.

Write or phone for more information on the transputer family and start making history yourself.

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IMS T212	16 bit Transputer–2Kbyte —4 links
IMS M212	16 bit Disc Processor–1Kbyte—2 links
DEVELOPMENT TOOLS	
IMS D701-2	IBM PC—Transputer Development System.
IMS D600	VAX/VMS—Transputer Development System.
EVALUATION BOARDS	
IMS B002-2	Double Eurocard + IMS T414 + 2Mbyte DRAM + 2 x RS232.
IMS B003-1	Double Eurocard + 4 x IMS T414 + 4 x 256Kbyte DRAM.
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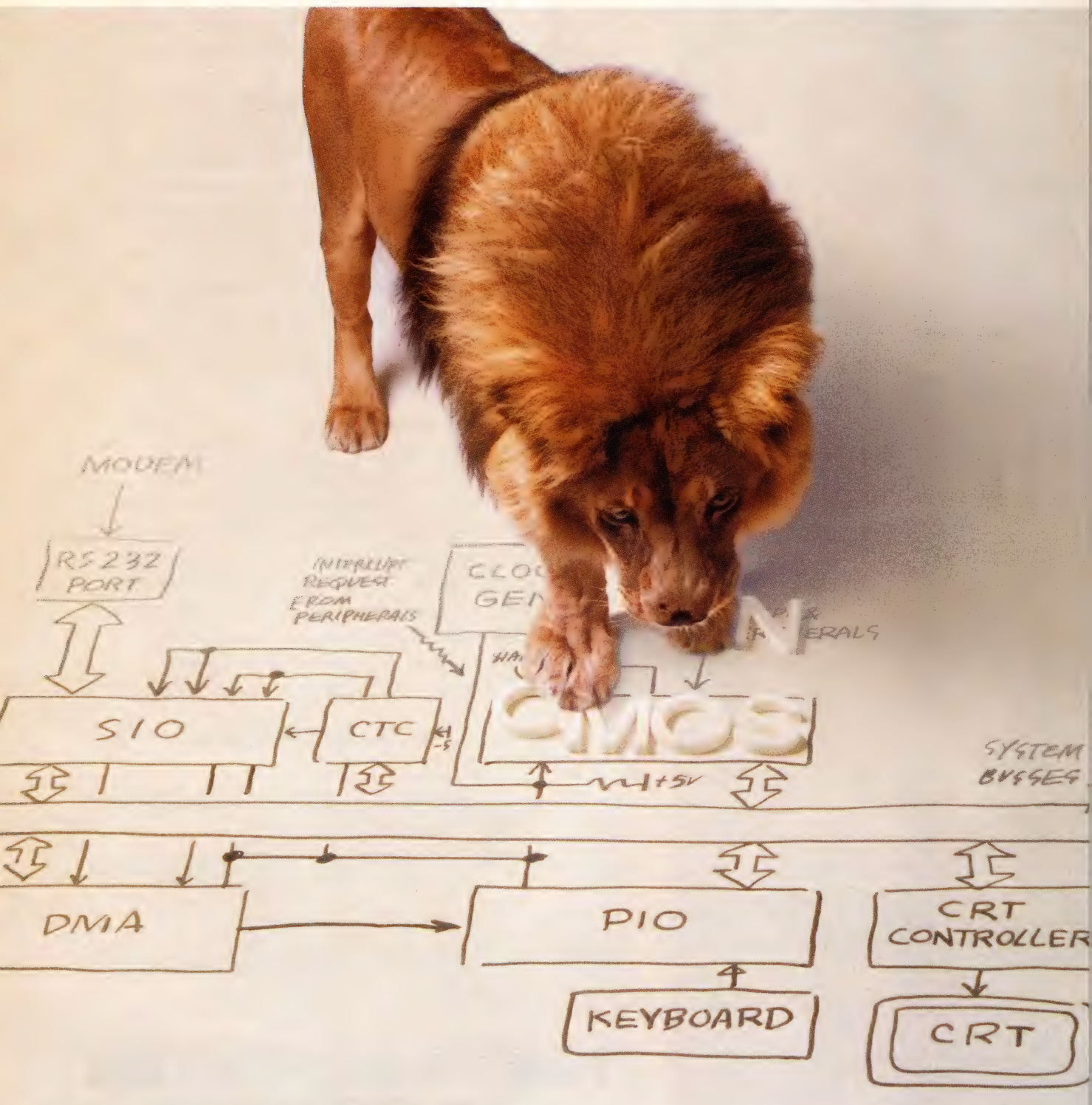

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TMPZ84C20	PIO: Parallel Input/Output Controller	CMOS	2mA	$<10\mu A$
T6497	Clock Generator/Controller	CMOS	2mA	$<10\mu A$
TMPZ84C40	SIO: Serial Input/Output Controller	CMOS	25mA	$<10\mu A$
TMPZ84C10	DMA: Direct Memory Access Controller	CMOS	25mA	$<10\mu A$

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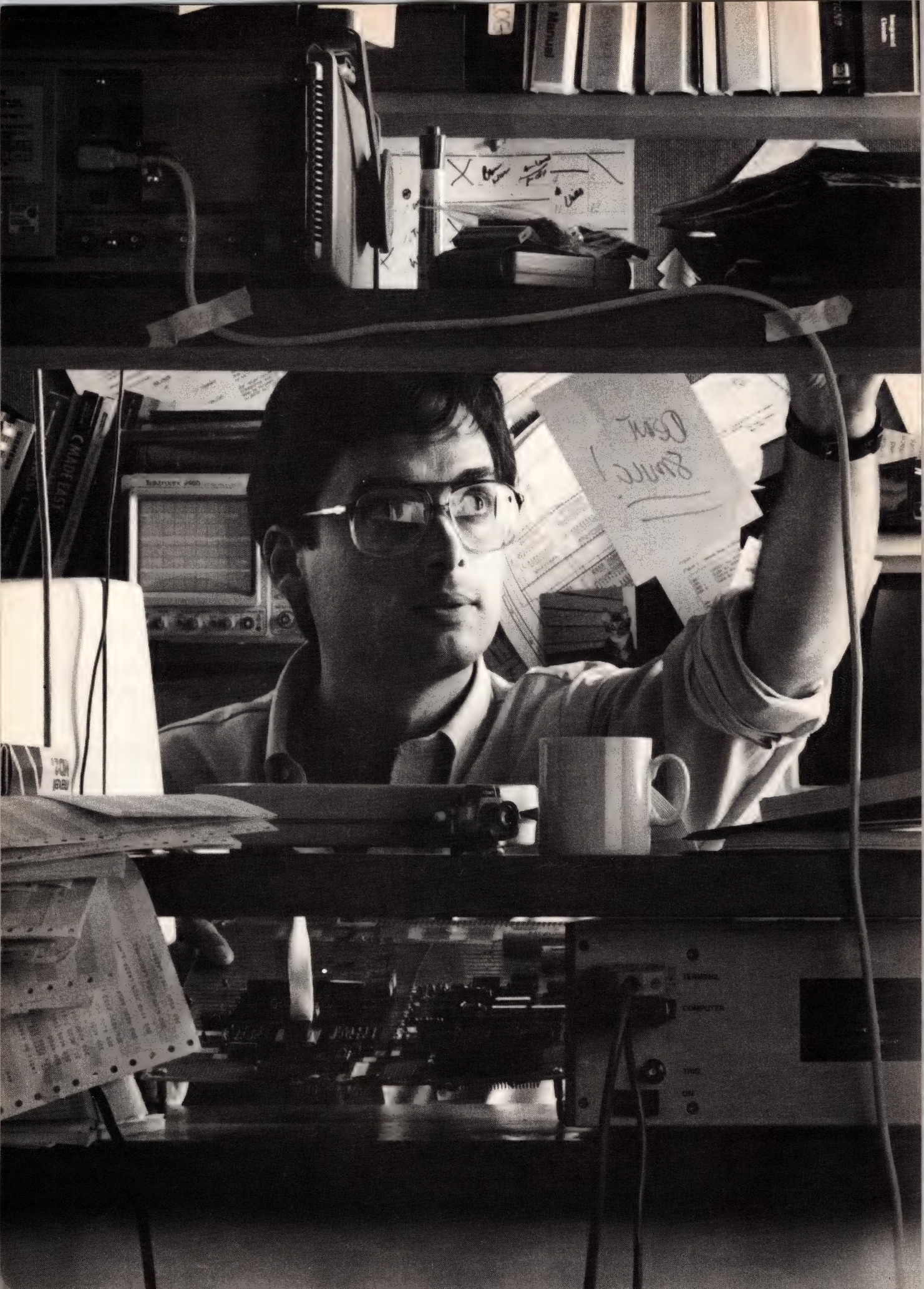
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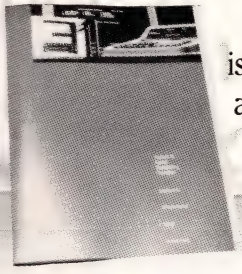

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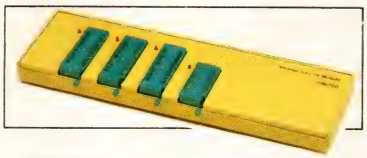

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NEWS BREAKS

EDITED BY JOAN MORROW

PRECISION OP AMP PROVIDES WIDE-BANDWIDTH PERFORMANCE

The HA-5147 monolithic operational amplifier from Harris Semiconductor (Melbourne, FL, (305) 724-7000) combines a 35V/μsec slew rate and 500-kHz full-power bandwidth with precision-op-amp specs: 3-nV/$\sqrt{\text{Hz}}$ noise, 30-μV offset voltage, and 1800V/mV open-loop gain. Built with Harris's dielectric-isolation process, the amplifier also provides a 120-dB gain-bandwidth product and a 126-dB CMRR.

For applications in which the op-amp gain is greater than 10, you can improve performance by substituting the HA-5147 for a 725, OP25, OP06, OP07, or OP37 op amp. (Internally compensated versions HA-5127 and HA-5137 will be offered later.) Commercial and military versions of the HA-5147 will be available in January; prices will range from $10.22 to $51.07 (100).—Tarlton Fleming

32-BIT MICROPROCESSOR COMES IN 20-MHz VERSION

National Semiconductor Corp (Santa Clara, CA) has begun shipments of its 20-MHz NS32332 32-bit CPU. The device is aimed at such real-time applications as laser printers, factory automation and robotics, and aerospace and military systems. For more information on this microprocessor family, as well as 50 others, turn to EDN's Thirteenth Annual μP/μC Directory, which begins on pg 102.

National also has begun shipping samples of its NS32382 memory-management unit for the 32000 Series μP family. The 32382, packaged in a 125-pin pin-grid array, operates at 15 max. It supports as much as 4G bytes of memory and page sizes of 4k bytes.—Joan Morrow

CHIP FURTHER ENHANCES IBM GRAPHICS STANDARD

The Enhanced Graphics Adapter (EGA), which has become the de facto graphics standard for IBM Personal Computers, owes much of its success to the availability of inexpensive EGA clones. (For more information on this topic, see "Boards that meet EGA spec bring flexible graphics capability to IBM PC workstations," EDN, September 18, 1986, pg 75). The majority of these non-IBM boards are based on an inexpensive 4-IC graphics controller chip set from Chips and Technologies Inc (Milpitas, CA, (408) 434-0600). The company now offers the 82C435, a single-chip enhanced graphics controller, which, when combined with the $15 (100) 82C436 bus interface IC, reduces an EGA-board chip count to 15 ICs, including 256k bytes of display memory. Resolution can be as high as 640×480 pixels.

The 82C435 provides smart autoemulation, which enables the adapter to automatically switch between EGA, IBM CGA (Color Graphics Adapter), IBM MDA (Monochrome Display Adapter), and Hercules graphics modes. This feature is similar to one incorporated in Paradise Systems Inc's (South San Francisco, CA) Autoswitch. In addition, the $50 (100) 82C435 supports the Microsoft Windows operating environment.—Margery S Conner

POWER-FAIL IC GIVES EARLY WARNING OF SUPPLY FAULTS

A CMOS-processed power-fail detector from GE/Intersil (Cupertino, CA) gives speedy warnings of any problems in a power-supply circuit. Model ICL7677 is suitable for use on either the primary or secondary side of a power supply. On the primary side, you can use it in conjunction with optoisolators that transmit fault indications to the equipment on the secondary side. On the secondary side, it has the ability to drive TTL/CMOS logic at its fault-indicating outputs. The IC's four outputs give no-fault,

undervoltage, overvoltage, and overtemperature or overcurrent indications. You can program the IC's time delays to prevent false indications that could otherwise result from spikes or noise.

The device provides an output state that indicates that a supply is turning on; the state changes when the supply voltage reaches its nominal operating range. The chip includes a bandgap reference that allows you to program the detection thresholds; alternatively, you can use an external voltage reference. The ICL7677 doesn't need an additional power supply; it operates from the supply it's monitoring. It costs $3.95 (100).—Bill Travis

NBS CERTIFIES 14 ELECTROMAGNETIC-COMPATIBILITY TEST LABS

Acting on the request of industry groups and manufacturers, the National Bureau of Standards has accredited 14 commercial laboratories to perform electromagnetic-compatibility and telecommunications-equipment testing. The laboratories are accredited to perform FCC standard tests for conducted and radiated emissions, vibration and temperature, and hearing-aid compatibility, among other tests. Industry groups and manufacturers sought the accreditation program to assist them in sales of their products to foreign agencies.

Annual accreditation fees range from $1900 to $2925. The fees cover the cost of on-site assessment once every two years, periodic proficiency testing, and program operating costs. For more information, contact Manager, Laboratory Accreditation, A531 Administration Building, National Bureau of Standards, Gaithersburg, MD 20899, or phone (301) 921-3431.—Deborah Asbrand

1G-SAMPLE/SEC WAVEFORM DIGITIZER HAS 10-BIT RESOLUTION

The Model 3000 single-channel digitizer—the first product from Sequence Inc (San Jose, CA, (408) 436-6065)—has an analog input bandwidth of 350 MHz. You can gang as many as eight digitizers together under the control of an IBM PC/XT host. To set up a measurement, you use the host's mouse to issue commands on the setup menu. You have control over the digitizer's input sensitivity, offset level, timebase value, trigger level, and trigger mode. The results can be displayed in color on a split screen. You can compare waveforms with each other or with waveforms stored on disk. Or you can display the waveform with its Fourier transform.

Sequence spent the last 2½ years developing the parallel-processing-array technology used for the analog-to-digital conversion. One of the features of the technology is its resulting low time-aperture jitter specification of less than 3 psec rms. The Model 3000 costs $30,000.—Chris Everett

SEMICONDUCTOR MANUFACTURER EXPANDS EPROM OFFERING

Signetics (Sunnyvale, CA) last month announced the availability of production quantities of its 256k-bit 27C256 CMOS EPROM, which complements the company's 64k-bit 27C64A, a 64k-bit version introduced in July. The 27C256 features a 32k×8-bit organization and costs $10 (100). The 27C256 and 27C64A are each packaged in a 28-pin quartz-windowed ceramic DIP.—Rick Nelson

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NEWS BREAKS: INTERNATIONAL

BY PETER HAROLD

VME BUS PRODUCTS HIGHLIGHTED AT SYSTEC '86

The VME Bus area at Systec '86—Munich's international trade fair for computer integration, which was held last month—was the venue for several new VME Bus product announcements.

The Focus-32 VME Bus system from Force Computers (Ottobrunn, West Germany, TLX 524190) is a 32-bit development/target system based around a 16-layer high-speed backplane. The 12-slot backplane accommodates two board stacks, each with six horizontally mounted double Eurocards positioned alongside each other in a 4U-high desktop case, which you can also position as a vertical tower cabinet. The boards plug in from the rear, leaving the front panel free for disk drives and operating controls. The unit has a double-skinned metal case to minimize EMI problems. Complete with a 450W power supply, an 80M-byte hard-disk drive, a 1M-byte floppy-disk and system controller, serial I/O, a SCSI bus controller, 1M-byte memory, and 32-bit CPU cards, the Focus-32 costs between $22,500 and $25,000.

The 68020-based GC20 VME Bus CPU card from Eltec (Mainz, West Germany, TLX 4187273), when used with the company's PIG and HRG graphics controller boards, provides high-level graphics command processing capabilities. To eliminate arbitration problems on the VME Bus, the board communicates with the graphics boards via a private bus. The board, which costs between DM 6000 and DM 8000, supports the company's HiResPac and PigPac graphics software packages. The company is developing firmware to provide a GKS interface to the graphics system. Additional onboard facilities include 1M byte of dual-ported RAM, a SCSI interface, serial I/O ports, a real-time clock, and an optional 68881 math coprocessor.

The $4400 Model 2501-4280-5 board from Microproject (Haarlem, The Netherlands, TLX 71189) is a VME Bus-compatible memory board that features 8M bytes of parity-checked dynamic RAM, a read access time of less than 200 nsec, write access time of less than 80 nsec, cycle time of less than 300 nsec, and hidden refresh. It supports 8-, 16-, and 32-bit data transfers, including unaligned and block transfers. The board recognizes 24- and 32-bit VME Bus addresses and is jumper selectable on 1M-byte address boundaries.

The SISC-16 VME Bus serial-I/O board from Stollmann (Hamburg, West Germany, Teletex (17) 403226) is an intelligent serial-I/O controller for as many as 16 full-duplex asynchronous RS-232C channels. Each channel has independent, software programmable Rx and Tx baud rates. The board can handle input data rates of greater than 16,000 cps (typically 30,000 cps). It supports software handshaking via X On/X Off protocol or hardware handshaking on the RTS and CTS signal lines. Onboard firmware is optimized for a Unix-V environment, and Unix-V software drivers are available. The SISC-16 costs DM 4000 and DM 4600, depending on the number of ports.

If you need to investigate backplane bus activity in 16-bit VME Bus systems, the $4900 VME Bus Tracer module from Vmetro (Oslo, Norway, phone 47-2-360968) provides you with a passive probe into 72 VME Bus signal lines. It has an onboard processor and firmware and interfaces via an RS-232C link to a standard ASCII terminal. Trace memory amounts to 1024 bus samples, and you can position the trigger point for pre-, post-, or mid-triggering. Synchronous sampling allows you to capture individual data-bus transfers; asynchronous sampling at a clock speed as high as 16 MHz allows you to investigate timing errors on the bus lines.

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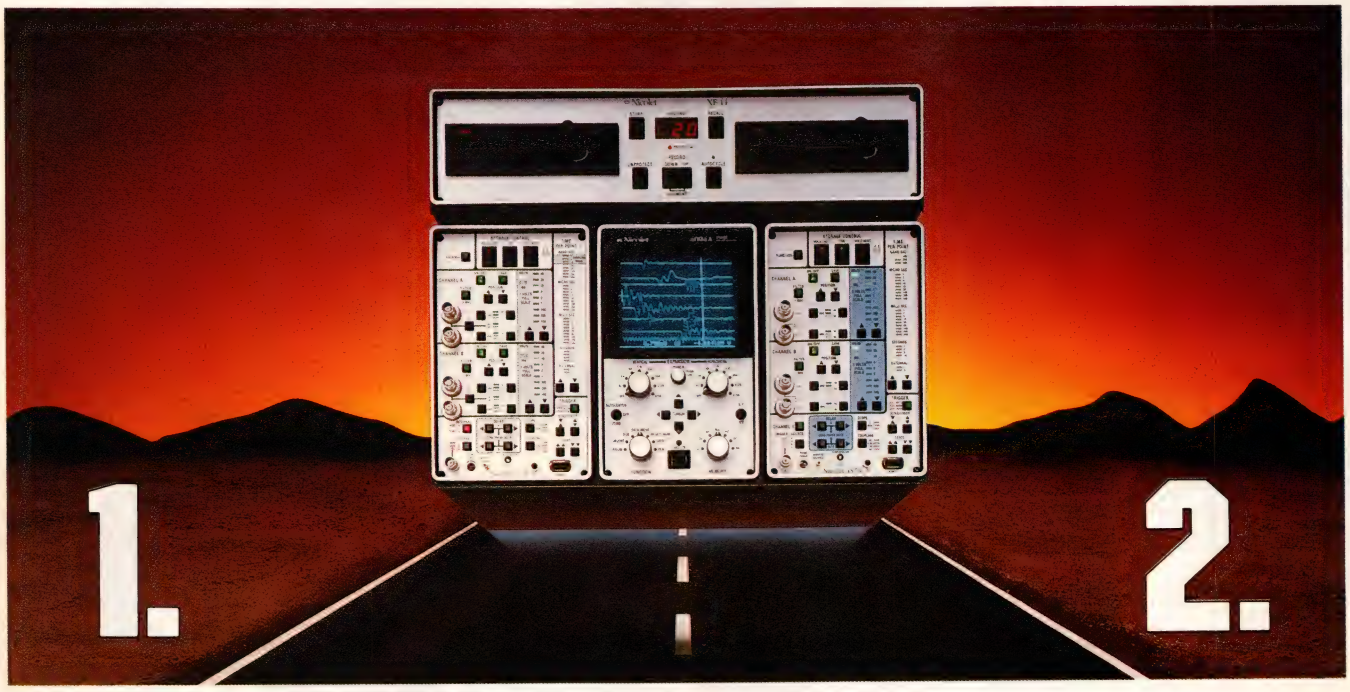

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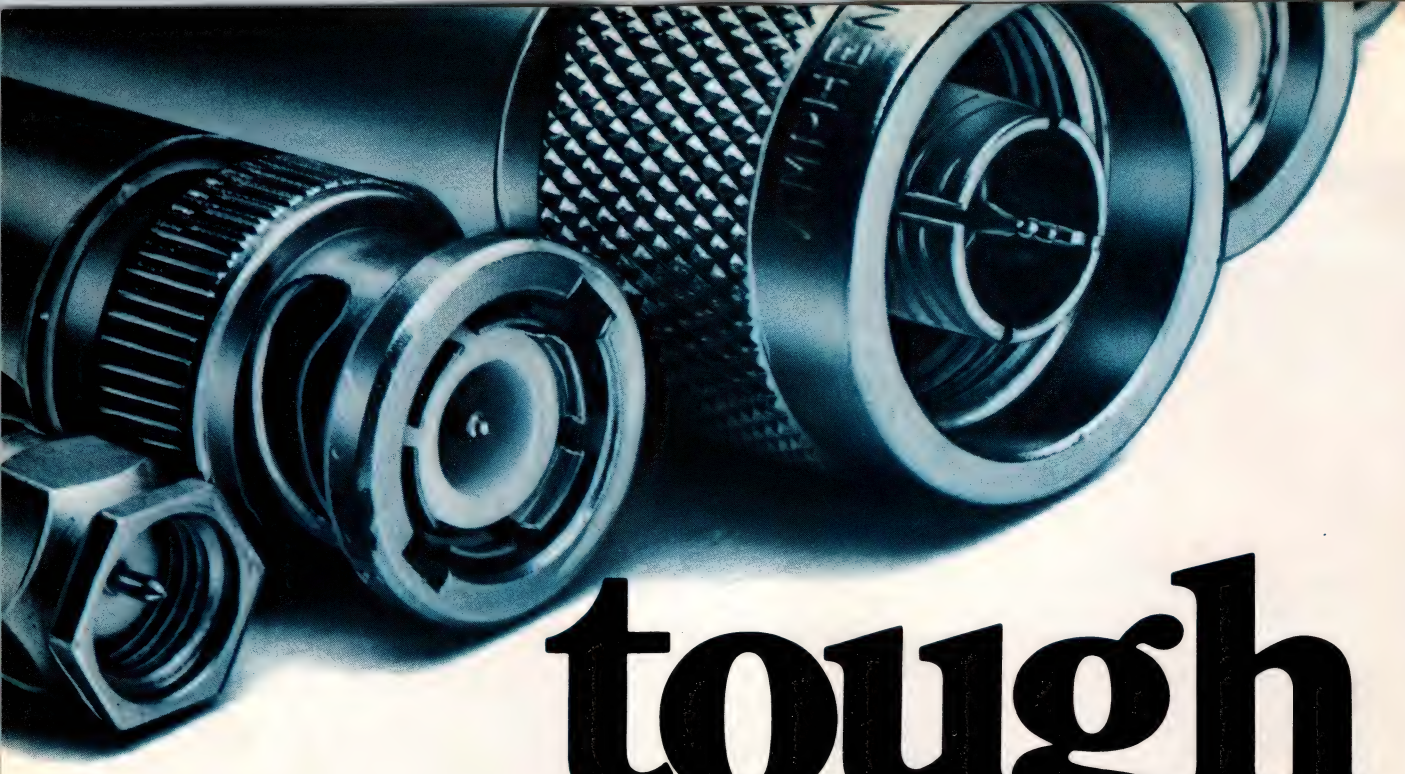

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3	●	■	●	●
4	●	●	●	●
5	●	●	●	●
6	●	■	●	●
7	●	●	●	●
8	●	●	●	●
9	●	●	●	●
10	●	■	●	●
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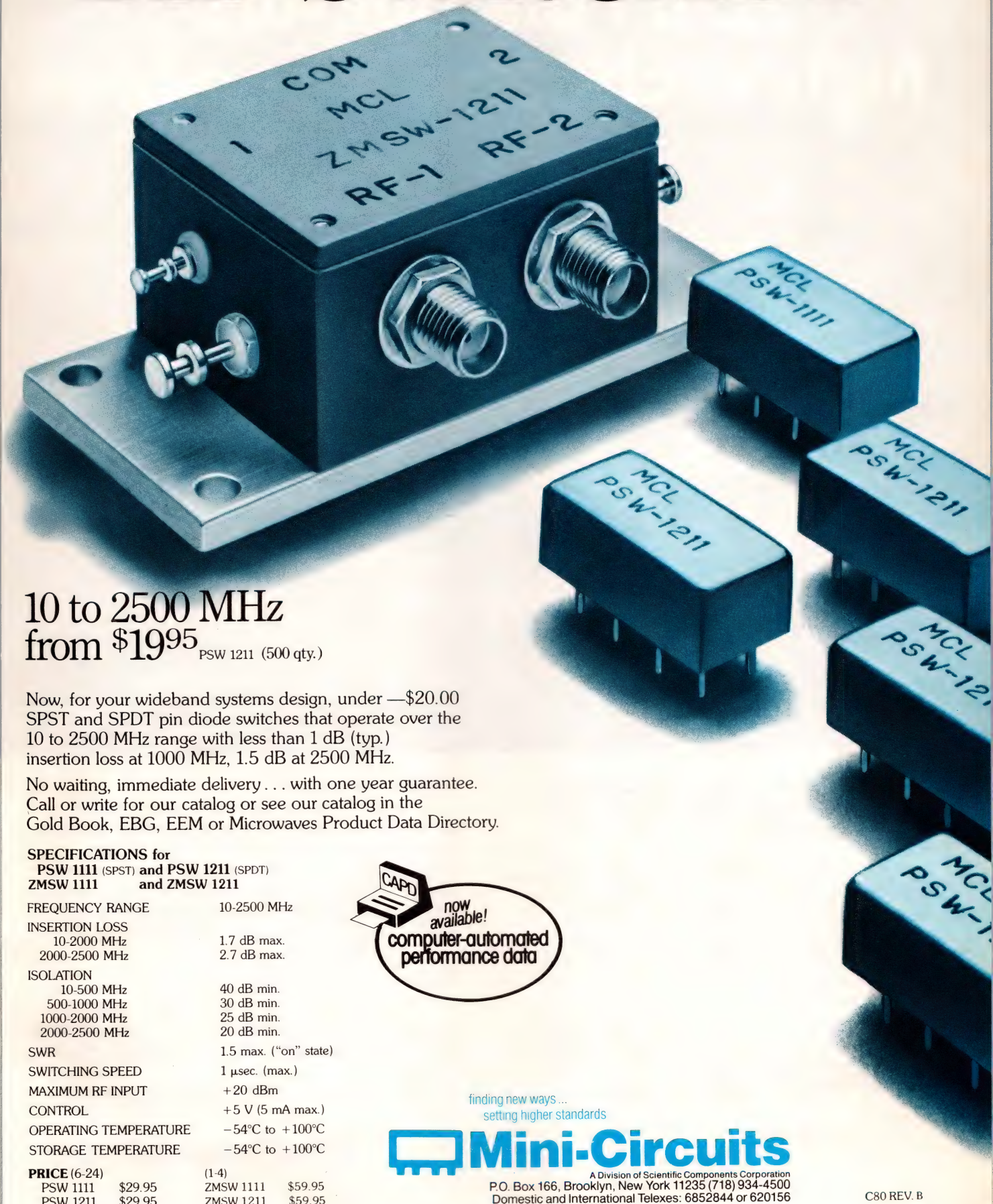

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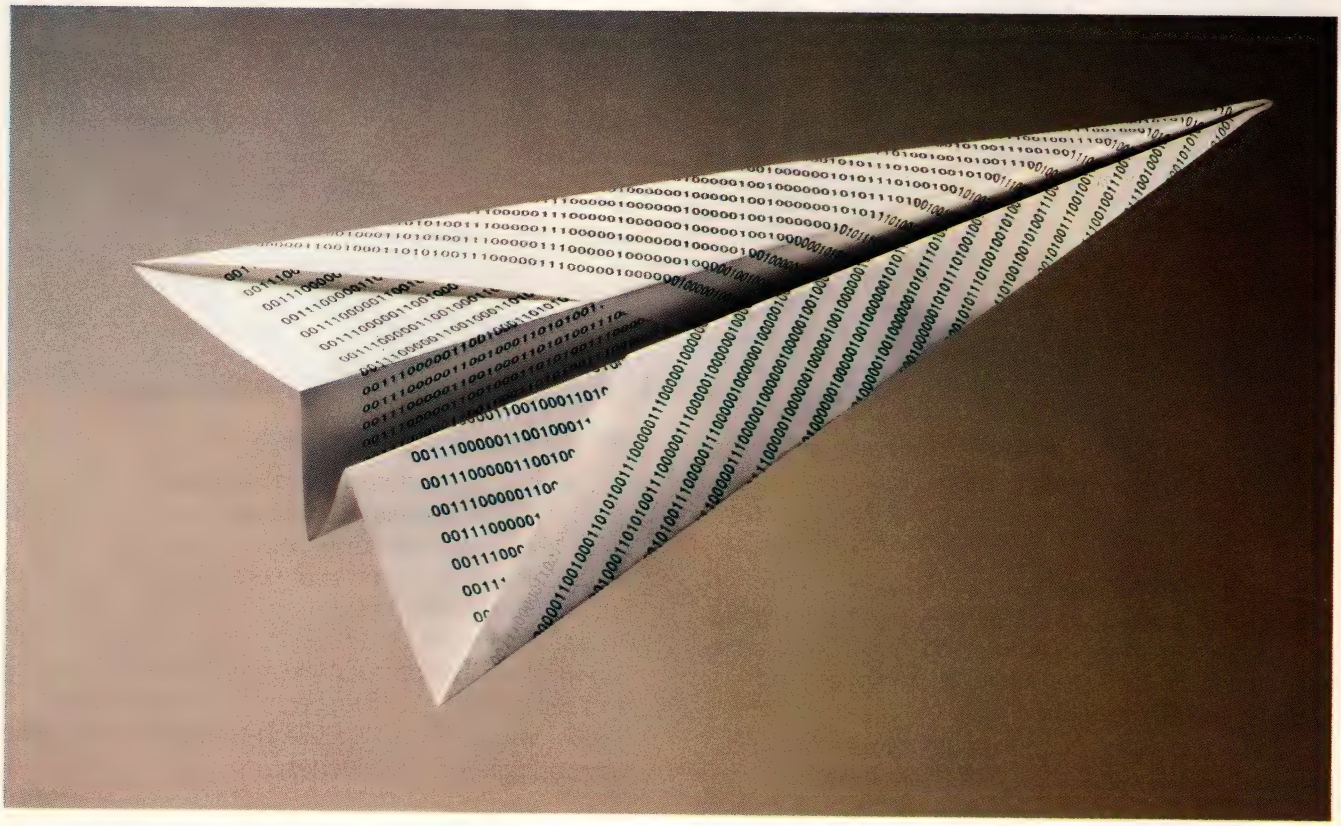

Now you can cut the cost of a PC LAN dramatically with our new 82588 LAN controller.

It's the most integrated networking solution in the 1-2 Mbps range.

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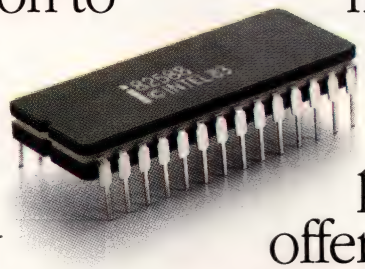

We put timing recovery, data encoding/decoding, collision detection and transmit clock generation all on a single chip. To lower your component count.

Which adds up to even more savings in areas like assembly, testing and reliability.

And we made sure that the 82588 supports emerging LAN standards like StarLAN. It also supports the IBM® PC Network. Plus many other specialized baseband and broadband LANs.

And because it snaps together with Intel's world standard 186 and 188 microprocessors, you eliminate TTL glue and save even more money. While speeding up your design.

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CIRCLE NO 178

SIGNALS & NOISE

The technician syndrome

Dear Editor:

The technician syndrome is an all-too-common disease of persons who have started as technicians, studied part time to obtain a bachelor's degree, and have been promoted to the title of Engineer. They have lost the ability to think. My observations have indicated that close to half of the persons who have gone through this sequence have succumbed.

The disease is contracted while the person is a technician. Once it's contracted, treatment is difficult. Many persons never recover.

The disease is just as debilitating to a technician as to an engineer. But the results expected of an engineer are so much greater than those expected of a technician that the net loss to his career and to his employer are correspondingly greater.

As with any disease, there must be a susceptible person and a causative agent. As with any disease, some persons are not susceptible and will tolerate the most severe causative agent without contracting the disease. As with many diseases, the genetic factor that permits an individual to resist it may be harmful in another respect.

The causative agent is a certain type of engineer for whom the technician works. This type of engineer, because of personality or because of pressure, does not encourage the technician to use his judgment. The engineer does not take the time to explain in detail the ultimate purpose of an operation. If the technician's knowledge is not sufficient for him to understand it, the engineer does not educate him. The technician is told to perform the task without questions.

Nothing ever goes as planned, however. If the technician is making a series of measurements, they will not come out as expected. Obviously, if we could predict the outcome perfectly, there would be no point in making a test. Therefore, the measurements will miss some critical points or take much longer than necessary.

There are three losers: the technician, who does not learn how to feed back test data to modify a test plan in real time; the engineer, who will have to revise the test plan after the

Continued on pg 32

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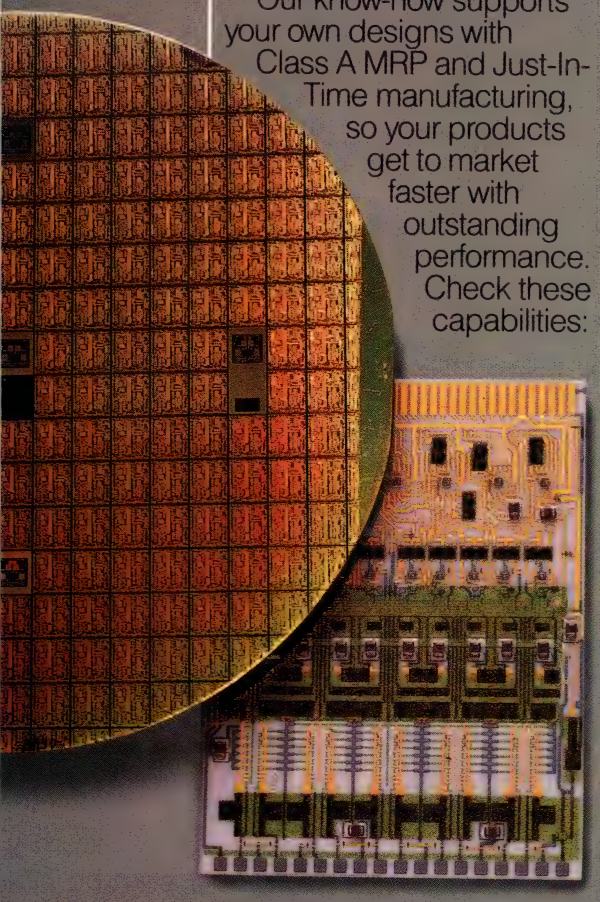

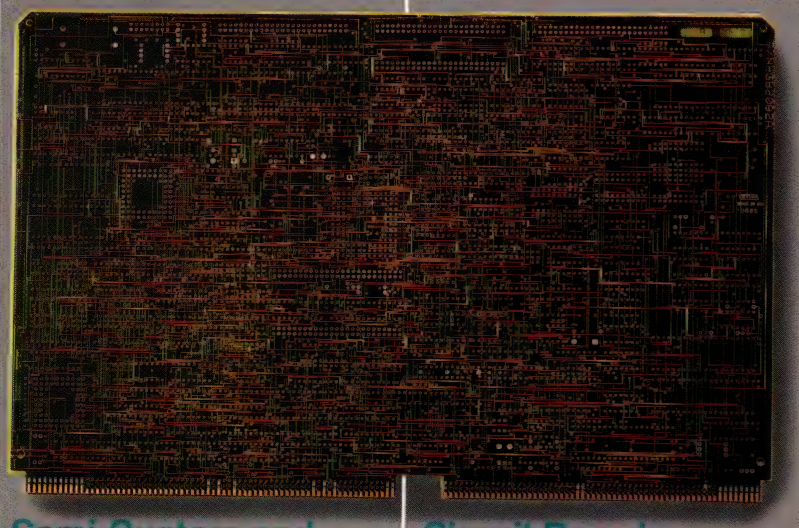

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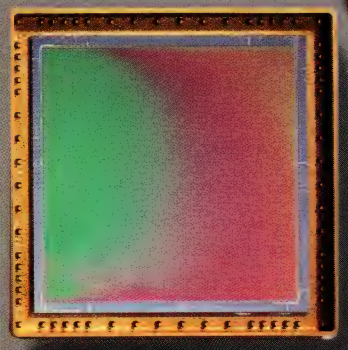

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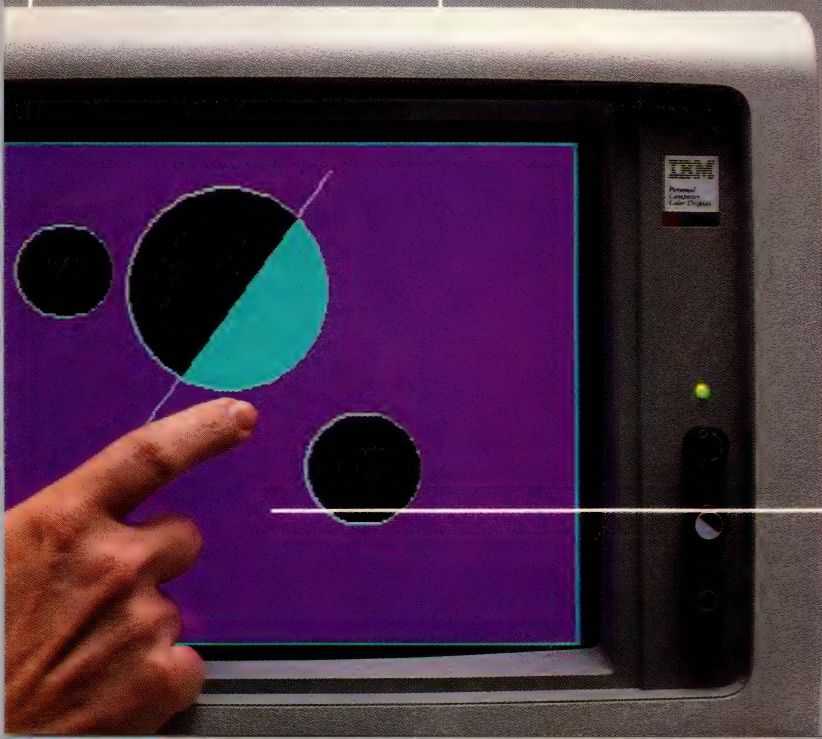

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wasted effort; and the company, which pays for it all.

Most technicians, if they have a little knowledge, will recognize the weakness of the plan, and will suggest a change. The type of engineer that causes the problem will ignore their suggestions. After a few such experiences, the technician will feel defeated and will cease to offer suggestions. He will do exactly what he is told and will even stop thinking about improvements. He now has succumbed.

A few technicians have the emotional strength to persevere. Unfortunately, they will antagonize the engineer, who is their immediate superior. If the engineer were the type who would listen, he never would have caused the problem. The technician's only solution is another supervisor, department, or company.

Unfortunately, few schools teach students how to think. Most teach "facts." The poor victim may complete the work for a bachelor's or even an advanced degree, and still have no concept of how to handle the unexpected or the new.

If a victim is lucky, he may come under the tutelage of someone with sufficient patience and time to make him think. Then, recovery is possible. Unfortunately, as with most deadly diseases, contracting the technician syndrome is easier than curing it.

Sincerely yours,
Matthew W Slate
H&M Associates
Sudbury, MA

A different display technology

Dear Editor:

In the article "Advances in flat-panel-display technology improve display features and cut prices" (EDN, September 4, pg 79), Sigmatron Nova's application-specific-device approach was covered quite nicely and accurately. There was an error, however, in the type of technology we manufacture. The article states that we work with dc EL (powdered phosphor) technology. In fact, we work with ac thin-film EL, and are the original inventors of the ac thin-film technology.

Sincerely yours,
Bill J Van Ollefen
Sigmatron Nova Inc
Thousand Oaks, CA

WRITE IN

Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

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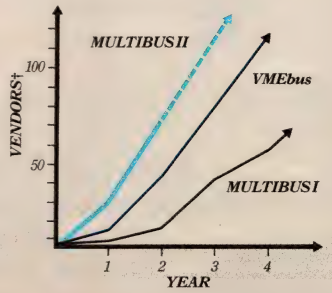

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† SOURCE: Technical Publishing Co. buyer's guides. and various VME directories.

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Armed Forces Communications and Electronics Association/Kansas Chapter Symposium and Exhibition: The Role of Modeling and Simulation in Command and Control, Kansas City, MO. Rich Mullen, Attendance Chairman, c/o Northrop Wilcox, 2001 NE 46th St, Kansas City, MO 64116. (816) 453-2600. December 2 to 4.

Real-Time Operating Systems: A Hands-On Workshop, Washington, DC. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. December 2 to 5.

Electromagnetic Interference—Characteristics and Control, Milwaukee, WI. Center for Continuing Engineering Education, University of Wisconsin-Milwaukee, 929 N 6th St, Milwaukee, WI 53203. (414) 224-3952. December 3 to 5.

International Electron Devices Meeting, Los Angeles, CA. Melissa Widerkehr, Courtesy Associates, 655 15th St NW, Suite 300, Washington, DC 20005. (202) 347-5900. December 7 to 10.

International Thermal Expansion Symposium and Exhibit, Pittsburgh, PA. P S Gaal, ITES General Chairman, Anter Laboratories, 1700 Universal Rd, Pittsburgh, PA 15235. (412) 795-6410. December 8 to 10.

International Original Equipment Design Show and **Integrated Manufacturing Expo,** New York, NY. Penton Expositions, 122 E 42nd St, Suite 900, New York, NY 10168. (800) 634-4639; in NY, (212) 867-9191. December 9 to 11.

Principles of RF and Microwave Circuit Design, Santa Clara, CA. Besser Associates, 3975 E Bayshore Rd, Palo Alto, CA 94303. (415) 969-3400. December 15 to 17.

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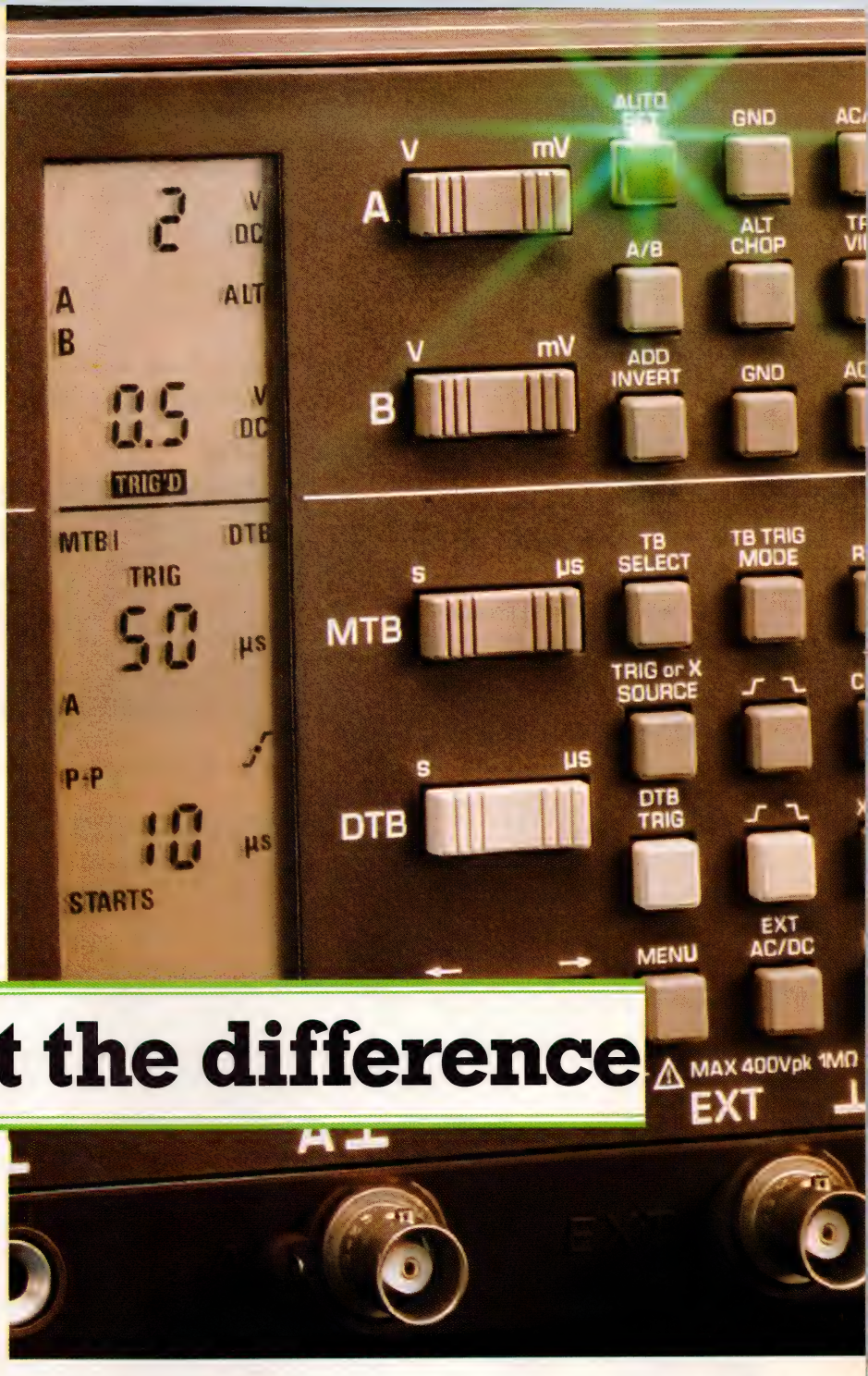

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CALENDAR

Survey of Computer-Communications Standards (seminar), College Park, MD. Professional and Career Development Program, University of Maryland, University College, College Park, MD 20742. (301) 985-7122. December 15 to 17.

Dexpo East (DEC-Compatible Exposition and Conference), New York, NY. Expoconsul International, 3 Independence Way, Princeton, NJ 08540. (800) 628-8185; in NJ, (609) 987-9400. December 17 to 19.

Microcomputer Graphics Show and Conference, New York City, NY. Expoconsul International, 3 Independence Way, Princeton, NJ 08540. (609) 987-9400. December 17 to 19.

Invitational Computer Conference, Irvine, CA. B J Johnson & Associates, 3151 Airway Ave, #C-2, Costa Mesa, CA 92626. (714) 957-0171. January 8.

American Society of Test Engineers Annual Conference, Anaheim, CA. ASTE, 114 N Hale St, Suite 2B, Wheaton, IL 60187. (312) 260-1055. January 8 to 9.

Annual Battery Conference on Applications and Advances, Long Beach, CA. Roseann Schaff-Matheny, Dept of Electrical Engineering, California State University, 1250 Bellflower Blvd, Long Beach, CA 90840. (213) 498-4605. January 13 to 15.

Buscon West (Bus/Board Users Show and Conference), Los Angeles, CA. Buscon, 17100 Norwalk Blvd, #116, Cerritos, CA 90701. (213) 402-1610. January 20 to 21.

Syscon (Subsystems Conference and Exposition), Los Angeles, CA. Syscon, 17100 Norwalk Blvd, #116, Cerritos, CA 90701. (213) 402-1610; (714) 552-4617. January 20 to 21.

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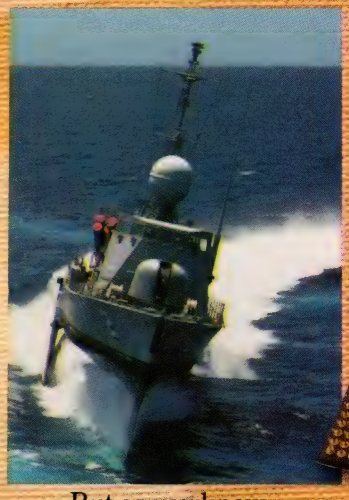

Today we're adding to our list—and recording firsts—faster than ever in our military history. For example, our AD7541 recently became the first 12-bit D/A converter to pass QPL muster.

But as you know, a long list of QPL parts is only half the battle. You've also got to be able to deliver them on time, in volume.

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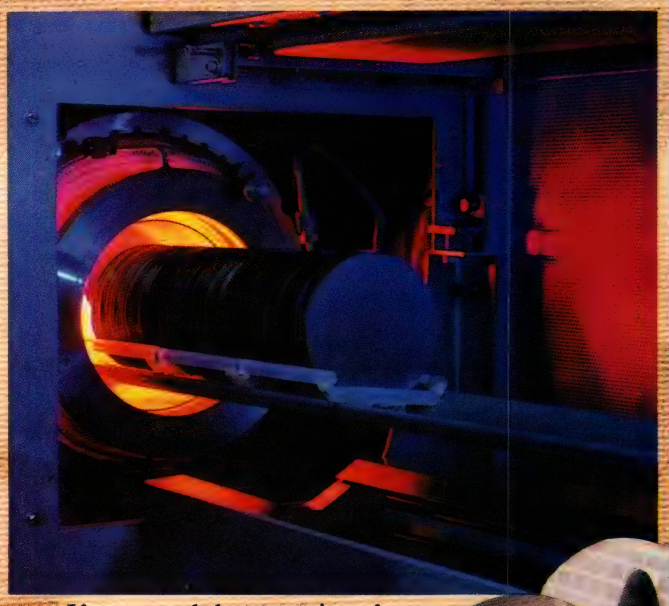

If you need the security of a bonded inventory, you've got it. Do you want off-the-shelf inventory at any of our military distributors? No problem.

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11101BIC	DG181AA
11101BCA	DG181AP
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11106BCA	DG188AP
11107BAC	DG190AL
11107BEC	DG190AP
11107BEA	DG190AP
11108BAC	DG191AL
11108BEC	DG191AP
11108BEA	DG191AP
12302BEA	DG201AP
12302BEC	DG201AP

New JM38510 QPL's Forthcoming
Analog Switch

10505BEC	IH5044
10505BEA	IH5044
10506BEA	IH5045
10506BEC	IH5045
11101BIA	DG181
11102BIA	DG182
11105BIA	DG184
11106BIA	DG185
11601BCC	DG300A
11601BCA	DG300A
11602BCC	DG301A
11602BCA	DG301A
11603BCA	DG302A
11603BCC	DG302A
11604BCA	DG303A
11604BCC	DG303A
19001BXC	IH6116
19003BXC	IH6216
19007BEA	IH6108
19007BEC	IH6108
19008BEA	IH6208
19008BEC	IH6208

Military DWG. No.

DESC77052-01EA	IH6108MJE
DESC77052-01EC	IH6108MDE
DESC77052-01EA	IH6108MDE
DESC77053-01EA	DG201AK
DESC77053-01EC	DG201AP
DESC77053-01EA	DG201AP
DESC78014-01CA	DG129AK
DESC78014-01CC	DG129AP
DESC78014-01CA	DG129AP
DESC81006-01AC	IH5040MFD
DESC81006-01EC	IH5040MDE
DESC81006-01EA	IH5040MDE
DESC81006-02AC	IH5041MFD
DESC81006-02EC	IH5041MDE
DESC81006-02EA	IH5041MDE
DESC81006-02IA	IH5041MTW
DESC81006-02IC	IH5041MTW
DESC81006-02IB	IH5041MTW
DESC81006-03AC	IH5042MFD
DESC81006-03EC	IH5042MDE
DESC81006-03EA	IH5042MDE
DESC81006-03IA	IH5042MTW
DESC81006-03IC	IH5042MTW
DESC81006-03IB	IH5042MTW
DESC81006-04AC	IH5043MFD
DESC81006-04EA	IH5043MJE
DESC81006-04EC	IH5043MDE
DESC81006-04EA	IH5043MDE
DESC81006-05AC	IH5044MFD
DESC81006-05EA	IH5044MJE
DESC81006-05EC	IH5044MDE
DESC81006-05EA	IH5044MDE
DESC81006-05IA	IH5044MTW
DESC81006-05IC	IH5044MTW
DESC81006-05IB	IH5044MTW
DESC81006-06AC	IH5045MFD
DESC81006-06EA	IH5045MJE
DESC81006-06EC	IH5045MDE
DESC81006-06EA	IH5045MDE
DESC81006-06IA	IH5045MTW
DESC81006-06IC	IH5045MTW
DESC81006-06IB	IH5045MTW
DESC81006-07AC	IH5046MFD
DESC81006-07EA	IH5046MJE
DESC81006-07EC	IH5046MDE
DESC81006-07EA	IH5046MDE
DESC81006-08AC	IH5047MFD
DESC81006-08EA	IH5047MJE
DESC81006-08EC	IH5047MDE
DESC81006-08EA	IH5047MDE
596285131-04XA	IH5116MJI
596285131-04XA	IH5116MDI
596285131-04XC	IH5116MDI
596285131-05XA	IH5216MJI
596285131-05XA	IH5216MDI
596285131-05XC	IH5216MDI
596285131-06EA	IH5208MJE
596285131-06EA	IH5208MDE
596285131-06EC	IH5208MDE

MIL-S-19500 Transistors

2N3821JAN	2N4858JAN
2N3821JTX	2N4858JTX
2N3821JTXV	2N4858JTXV
2N3823JAN	2N4859JAN
2N3823JTX	2N4859JTX
2N3823JTXV	2N4859JTXV
2N4091JAN	2N4860JAN
2N4091JTX	2N4860JTX
2N4091JTXV	2N4860JTXV
2N4092JAN	2N4861JAN
2N4092JTX	2N4861JTX
2N4092JTXV	2N4861JTXV
2N4093JAN	2N5114JAN
2N4093JTX	2N5114JTX
2N4093JTXV	2N5114JTXV
2N4856JAN	2N5115JAN
2N4856JTX	2N5115JTX
2N4856JTXV	2N5115JTXV
2N4857JAN	2N5116JAN
2N4857JTX	2N5116JTX
2N4857JTXV	2N5116JTXV

Latest List of MIL-STD-883B Rev. C Compliant Devices
Data Acquisition Products

883B Rev C.

AD7520SD/883B	DG151AL/883B
AD7320TD/883B	DG152AK/883B
AD7520UD/883B	DG152AL/883B
AD7521SD/883B	DG153AL/883B
AD7521TD/883B	DG153AP/883B
AD7533SD/883B	DG154AK/883B
AD7533TD/883B	DG154AL/883B
AD7533UD/883B	DG161AL/883B
AD7541SD/883B	DG161AP/883B
AD7541TD/883B	DG162AK/883B
ICL7134UJMJ1/883B	DG162AL/883B
ICL7134UKMJI/883B	DG163AL/883B
ICL7134ULMJI/883B	DG163AP/883B
ICL7662MTV/883B	DG164AK/883B
ICL8038AMJD/883B	DG164AL/883B
ICL8038BMJD/883B	DG180AA/883B
ICL8069DMSQ/883B	DG180AK/883B
ICL8212MTY/883B	DG180AL/883B

Timer/Counter Circuits
883B Rev C.

ICM7555MTV/883B	DG181AA/883B
ICM7556MJD/883B	DG181AK/883B

Amplifiers-Operational
883B Rev C.

ICL8023MJE/883B	DG181AL/883B
	DG182AA/883B
	DG182AK/883B
	DG182AL/883B
	DG183AL/883B
	DG183AP/883B
	DG184AK/883B
	DG184AL/883B
	DG185AK/883B
	DG185AL/883B
	DG186AA/883B
	DG186AL/883B
	DG186AP/883B
	DG187AA/883B
	DG187AK/883B
	DG187AL/883B
	DG188AA/883B
	DG188AK/883B
	DG188AL/883B
	DG189AP/883B
	DG190AK/883B
	DG190AL/883B
	DG191AK/883B
	DG191AL/883B
	DG200AA/883B
	DG200AK/883B
	DG201AK/883B
	DGM181AA/883B
	DGM181AK/883B
	DGM182AA/883B
	DGM182AL/883B
	DGM184AK/883B
	DGM184AL/883B
	DGM185AK/883B
	DGM185AL/883B
	DGM190AK/883B
	DGM190AL/883B
	DGM191AK/883B
	DGM191AL/883B
	IH5009MJD/883B
	IH5010MJD/883B
	IH5011MJE/883B

Analog Switch Products
883B Rev C.

D123AK/883B	IH5012MJE/883B
D123AL/883B	IH5013MJD/883B
D125AK/883B	IH5014MJD/883B
D125AL/883B	IH5015MJE/883B
D129AK/883B	IH5016MJE/883B
D129AL/883B	IH5017MDD/883B
DG126AK/883B	IH5018MDD/883B
DG126AL/883B	IH5019MDE/883B
DG129AK/883B	IH5020MDE/883B
DG129AL/883B	IH5021MDD/883B
DG133AK/883B	IH5023MDE/883B
DG133AL/883B	IH5024MDE/883B
DG134AK/883B	IH5040MFD/883B
DG134AL/883B	IH5040MJE/883B
DG139AK/883B	IH5041MFD/883B
DG139AL/883B	IH5041MJE/883B
DG140AL/883B	IH5041MTW/883B
DG140AP/883B	IH5042MFD/883B
DG141AL/883B	IH5042MJE/883B
DG141AP/883B	IH5042MTW/883B
DG142AK/883B	IH5043MFD/883B
DG142AL/883B	IH5043MJE/883B
DG143AK/883B	IH5044MFD/883B
DG143AL/883B	IH5044MJE/883B
DG144AK/883B	IH5045MFD/883B
DG144AL/883B	IH5045MJE/883B
DG145AL/883B	IH5046MFD/883B
DG145AP/883B	IH5046MJE/883B
DG146AL/883B	IH5047MFD/883B
DG146AP/883B	IH5047MJE/883B
DG151AK/883B	IH5052MJE/883B
	IH5053MJE/883B
	IH5108MJE/883B
	IH5116MJI/883B
	IH5140MFD/883B
	IH5140MJE/883B
	IH5141MFD/883B
	IH5141MJE/883B
	IH5142MFD/883B
	IH5142MJE/883B
	IH5143MFD/883B
	IH5143MJE/883B
	IH5144MFD/883B
	IH5144MJE/883B
	IH5144MTW/883B
	IH5145MFD/883B
	IH5145MJE/883B
	IH5148MFD/883B
	IH5148MJE/883B
	IH5148MTW/883B
	IH5149MFD/883B
	IH5149MJE/883B
	IH5150MFD/883B
	IH5150MJE/883B
	IH5150MTW/883B
	IH5151MFD/883B
	IH5151MJE/883B
	IH5208MJE/883B
	IH5216MJI/883B
	IH5341MTW/883B
	IH5352MJE/883B
	IH6108MJE/883B
	IH6116MJI/883B
	IH6201MJE/883B
	IH6208MJE/883B
	IH6216MJI/883B

Microcontrollers, Microperipherals, Memory
883B Rev C.

IM6402-1MJL/883B	
IM6402AIJL/883B	
IM6402AMJL/883B	
IM6402IJL/883B	
IM6653AMJG/883B	
IM6653MJG/883B	
IM6654-1IJG/883B	
IM6654AMJG/883B	
IM6654MJG/883B	

New 883B Rev C. Devices Forthcomin

ICL8013	
ICL8021	
ICL7667	
ICL7115	
ICL7109	
ICM7170	

On-Line Instructions

Dial 1-800-345-7335 (in CT 203-852-9201). On any ASCI terminal or PC with a 300 or 1200-baud modem (EVEN or IGNORE parity, 7 data bits, 1 stop bit). At "Enter Response Code," type GEIHIREL.

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CIRCLE NO 165

GEI

ZAX INTRODUCES 8051 EMULATION WITH...U.S.*

If you're engaged in microprocessor development using an 8051 microcontroller, then you need the ZAX ICD-378 8051 Emulator with U.S.*Host computer controlled, the ZAX 8051 Emulator supports the complete family of Intel's 8051/8052 microcontrollers and contains a menu-driven user interface with on-line help facility.

Our 8051 emulator features everything you need to meet your development deadlines. Features like: symbolic debugging, 64,000 hardware breakpoints, software driven chip reset, single-step instruction trace, logic state analyzer interface and U.S.*

The ZAX 8051 Emulator has 128K bytes of static RAM emulation memory (64K of code, 64K of data) and may be mapped with 16 byte resolution. Included is a 4K bytes deep × 48 bits wide real-time trace buffer for capturing program execution.

Software support for the ZAX 8051 is provided by our ZLINK user-convenient communications software package. ZLINK enhances the performance of the 8051 by utilizing the power of the host computer. It provides necessary features for real-time debugging like extensive breakpoint capability employing Boolean expressions and symbolic debugging.

For development software access, we offer a broad range of manufacturer-compatible software including PL/M 51 compilers, cross assemblers/loaders and object module librarians.

*For more information on ZAX's unique U.S., call our TOLL FREE number.

And should you need a wholly-supported host computer, look no farther than ZAX. The ZAX BOX-ER is an economical host computer that's easy to use, delivers abundant processing power, possesses superior memory capacity and supports high resolution graphics for engineering applications. The perfect complement to our 8051 emulator.

At ZAX, we're committed to providing you with the tools you need to meet your microprocessor-design deadlines. All of our products are backed by a full, one-year warranty which protects you from unnecessary delays. So, whether you're engaged in development using an 8051 microcontroller or a variety of microprocessors, call us and we'll show you how to beat your deadlines.

To order the ZAX ICD-378 8051 Emulator with U.S.* or for additional information, call us TOLL FREE at 800-421-0982 (in California phone 800-233-9817) or write to ZAX CORPORATION, 2572 White Road, Irvine, CA 92714. In Europe, call (49) 2162-32034.

ZAX

Zax Corporation

CIRCLE NO 166

SIEMENS

Stacked capacitors – technology from Siemens

10,000,000,000 stacked capacitors sold speak for themselves

Siemens was first to decide for film capacitors in stacked technology.

More than 30 years ago the world's first mass-produced self-healing film capacitors appeared from Siemens – leading to the development of stacked film technology.

Licences and know-how from Siemens went to manufacturers around the world.

Another stacked capacitor technology is used worldwide – ceramic multilayer capacitor MLC.

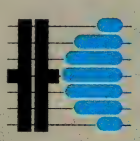
So that the customer gets all the benefits, Siemens offers
- stacked capacitors with anorganic dielectric material – ceramic multilayer capacitors MLC and
- stacked capacitors with organic dielectric material – metallized stacked film capacitors MKT.

Production facilities for stacked capacitors are located in West Germany, Austria, Spain and Brazil – which means fast and competent service for our customers.

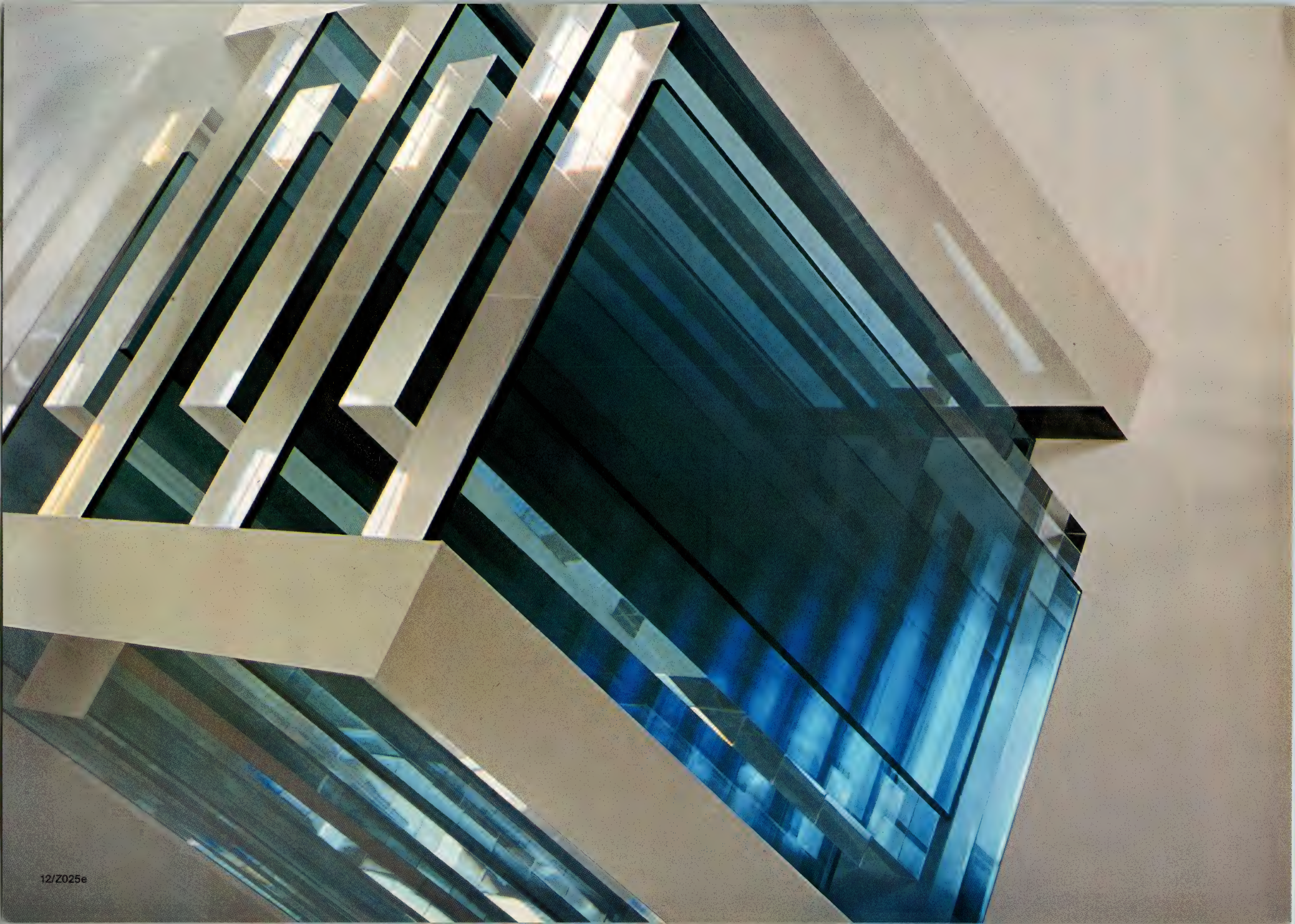
Ceramic multilayer capacitors
are notable for their
- extremely small dimensions
- excellent suitability as SMDs
- very good RF characteristics, especially with COG material
- wide ranges of operating temperature
- attractive prices

Metallized film capacitors
offer the user advantages like
- excellent for automatic insertion either as radial leaded boxes or SMDs
- high pulse-loading capacity
- very stable capacitance
- extremely high longterm reliability
- good price/performance ratio

If you need further information contact your nearest Siemens office or Siemens AG, Infoservice 12/Z025, Postfach 2348, D-8510 Fürth, West Germany quoting "Stacked capacitors".



CIRCLE NO 168



12/Z025e

Count on OKI to expand your options in CMOS Gate Arrays.

1.5-micron & 2-micron				3-micron	
70V000 Series VERY HIGH SPEED		*70H000 Series* HIGH SPEED		*70000 Series*	
# Gates	# I/Os	# Gates	# I/Os	# Gates	# I/Os
700	66	3289	86	387	44
1000	66	4290	104	720	62
1500	66	6000	130	1445	88
2000	80	8024	148	2000	106
2500	80	10008	172	4205	120

Expanded product families and packaging. For more cost-effective, more flexible single-chip logic integration, OKI supplies more pre-designed Gate Array options, in the most advanced package types: plastic or ceramic through-hole DIPs or pin grid arrays; or plastic surface-mount PLCC or flatpack.

Expanded services, plus world-leading production automation. OKI CSIC* design expertise is accessible at any development stage. And OKI's CSIC manufacturing/testing facilities—among the world's most highly automated—assure high quality, high volume fabrication.

RFQ OKI CMOS Gate Arrays

REQUEST FOR QUOTE

For prompt response to your Request for Quote (returned with complete technical data), please fill out the brief specs needed below:

Name/Title _____

Company _____

Address _____

City _____ State _____ Zip _____

Tel: (_____) _____

EDN112786

My application requires:

1. Gate count: _____ 2. Pin count: _____
3. **CMOS process:**
   ( ) 1.5 micron ( ) 2 micron ( ) 3 micron
4. **Packaging preferred:**
   Surface-mount ( ) PLCC ( ) Flatpack
   Through-hole ( ) Pin Grid Array ( ) DIP
5. **Anticipated volume:** _____ pieces/month

☐ Please call me for immediate consultation.

Request for Data

Please rush complete technical input on:

( ) CMOS Gate Arrays
( ) CMOS Standard Cells
( ) CMOS Custom VLSI Logic

To return your RFQ to OKI: Remove entire page and fold into thirds. Staple or tape together and mail to: OKI Semiconductor, 650 N. Mary Ave., Sunnyvale, CA 94086. Tel: (408) 720-1900.

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*Customer-Specific Integrated Circuit

SDI, national security, and opportunity

Back in the '50s, when the Committee on the Present Danger was urging that the United States arm and protect Western European nations from the Soviet menace, much criticism of this apparently hard-line containment policy came from the far right. The communists might welcome such a costly policy, the critics argued, as the kind of spending paroxysm that augurs the twilight of capitalism. Yet today, when deployment of any currently conceivable version of the Strategic Defense Initiative demands astounding levels of spending that threaten to bankrupt this nation, opponents of SDI are painted into a liberal-left corner, and no one publicly imagines the respective twinkles in the eyes of Marx, Lenin, and Stalin.

One argument for vigorous SDI R&D is unassailable: Nuclear arms are here to stay. We can't divest ourselves of the knowledge of how to make them, and no treaty restraining their proliferation is backed by the force that can compel maverick nations to comply. We must find a way to render them useless.

As to the arguments against SDI, forget for the moment that the software for a space-based defense system may be far too complex, that testing may be impossible—that "it can't be done." This criticism may be correct, but underestimating engineering ingenuity so often proves to be myopic. Forget also for the moment that the system must be virtually 100% impervious, that it can be overwhelmed by missiles, that it constitutes an additional trip-wire for a nuclear exchange, or even that it can serve as an offensive weapon. Let's consider simply the potential costs.

There is a growing awareness that national security encompasses more than just defense against belligerent governments. Environmental concerns—soil erosion, deforestation, depletion and pollution of the aquifer—are great threats globally, and infrastructure worries—deteriorating highways and bridges, cities choked with cars, waste and depletion of energy resources—are all too familiar problems here at home. These problems threaten our very standard of living, and that constitutes a threat to national security.

One familiar myth, summoned again in support of SDI, is that defense spending is good for the economy. The more we are locked into this way of thinking, the more it seems as though defense projects are the *only* way to employ large numbers of civilians. Yet Bureau of Labor statistics show that the job-to-government-dollar ratio is higher in the health, education, and civil engineering sectors than in the defense sector. Unquestionably, defense spending has been good to the engineer, but might not government spending on other projects—mass-transit systems, alternative energy resources, energy-management and -distribution systems, to name a few—create equally challenging opportunities for engineers?

The correlative question is, can we afford to concentrate large amounts of our wealth on SDI to the exclusion of other important national-security concerns? We must expand the terms of the debate, and in doing so, we needn't be threatening engineers' livelihoods. There are lots of security problems to be solved, and if they're allowed to, engineers will find myriad possible solutions. And they can meet these challenges without ideological and politically partisan sidetracks.

George C. Stubbs

George Stubbs
Staff Editor

Our brains hav

The reliable side.

At Quantum, we put at least half our thinking into making disk drives reliable.

Our Q200 Series™ of 5¼" intelligent disk drives is the perfect example of achieving near-perfection.

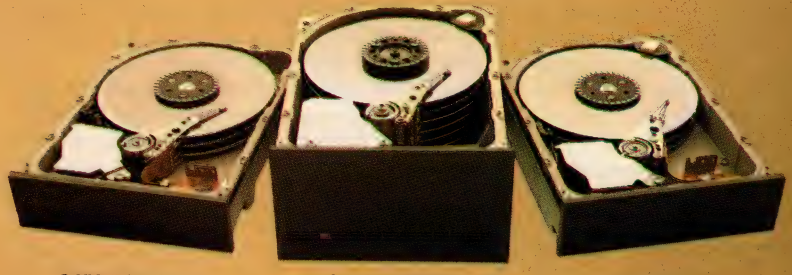
The mean time between failure for our Q200 Series products is 25,000 operating hours. Our customers' incoming acceptance rate is over 99%. And the many ship-to-stock programs with our customers underscore a confidence level that's even higher.

The extraordinary reliability of our Q200 Series drives is the result of the out-of-the-ordinary things we do to make them that way.

Because we were the first to make intelligent disk drives, we have more field-proven experience in making them to last. And because we designed both the SCSI controller electronics and the drive, they truly perform as if they were made for each other.

The Q200 Series drives are available in 53MB, 80MB and 160MB (formatted) capacity models. And our new custom-designed, semi-automatic manufacturing line in Milpitas enables us to make these high quality drives at the rate of one every 30 seconds. So availability is one more thing you can rely on—from Quantum.

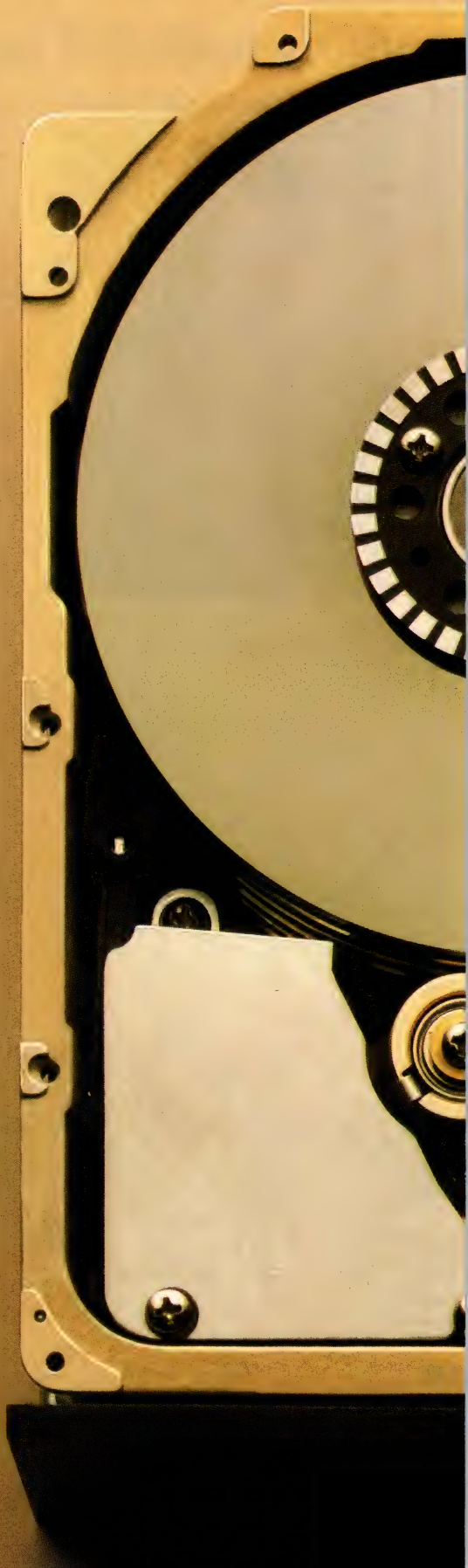
Quantum Corporation, 1804 McCarthy Blvd., Milpitas, CA 95035 (408) 262-1100. TWX 910-338-2203. Eastern Regional Sales: Salem, NH (603) 893-2672. Western Regional Sales: Santa Clara, CA (408) 980-8555. European Sales: Frankfurt, West Germany 069-6666-6167. Quantum products are distributed in the United States and Canada by Arrow Electronics.



Q250 (53MB) Q160 (160MB) Q280 (80MB)

Quantum

First In Intelligent Disk Drives



e two sides, too.

The innovative side.

At Quantum, we put at least half our thinking into making disk drives innovative.

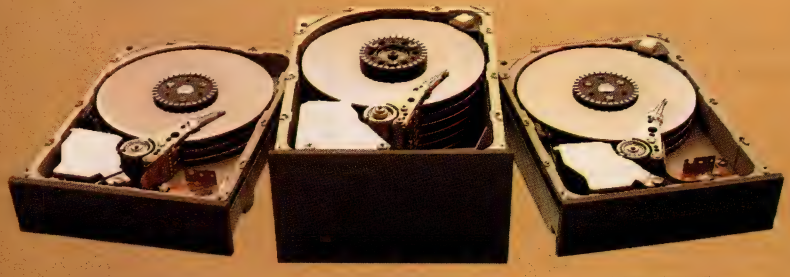
Our Q200 Series™ of intelligent disk drives is the best example of doing things ever better.

The half-height 53MB and 80MB (formatted) capacity models were the very first intelligent drives introduced — a major advancement in disk drive architecture, integrating a custom SCSI controller into the drive itself.

Soon thereafter, we introduced our full-height 160MB (formatted) capacity intelligent disk drive. This new model in the Q200 family incorporates yet another major advance — DisCache,™ a look-ahead, high-speed memory to significantly increase data throughput, with programmable options for individual application needs.

All three models in the Q200 Series use the same heads, the same media, and the same integrated controller design. They also use the same SCSI interface and support the same software commands, utilizing the industry standard common command set. That's why we can guarantee compatibility among the family, making it easier than ever to upgrade and enhance your systems — now and with future products. So if you're looking for future innovations, Quantum is where to look first.

Quantum Corporation, 1804 McCarthy Blvd., Milpitas, CA 95035 (408) 262-1100. TWX 910-338-2203. Eastern Regional Sales: Salem, NH (603) 893-2672. Western Regional Sales: Santa Clara, CA (408) 980-8555. European Sales: Frankfurt, West Germany 069-6666-6167. Quantum products are distributed in the United States and Canada by Arrow Electronics.



Q250 (53MB) Q160 (160MB) Q280 (80MB)

Quantum

First In Intelligent Disk Drives

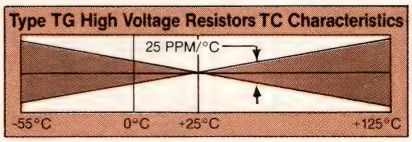
Precision High Voltage Resistors and Resistor Networks from CADDOCK for high performance, high voltage systems.

Type TG Low TC Precision High Voltage Resistors with a TC of 25 PPM/°C from -55°C to +125°C and resistance values to 1,000 Meg.

Constructed with Caddock's Tetrinox® resistance films to achieve exceptional temperature and loadlife stability, the Type TG high voltage resistors are ideal for the precision circuitry of TWT power supplies, electron microscopes, X-ray systems, high resolution CRT displays and geophysical instruments.

The Type TG resistors deliver this outstanding combination of performance specifications:

- Temperature Coefficient of 25 PPM/°C from -55°C to +125°C.



- Resistance range from 1 Meg. to 1000 Meg.
- Resistance Tolerances from 1.0% to 0.1%.
- Loadlife Stability of 0.25% per 1000 hours.
- Voltage ratings up to 48,000 volts.
- Max. Continuous Operating Temp. of +225°C.
- Exclusive Non-Inductive Performance.

plus - Matched Resistor Sets with Low Ratio Temperature Coefficient Tracking Performance.

The Type TG resistors can be used in combination with the low TC of Caddock's Type TK Low TC Precision Radial-Lead Resistors to achieve 30 PPM/°C Ratio TC without special matching.

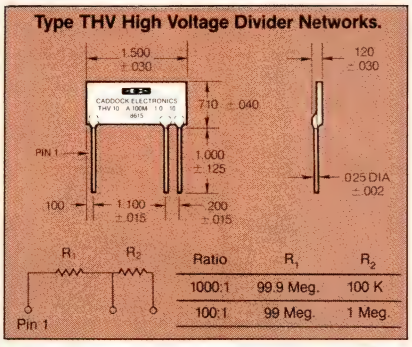
With special matching, a Ratio TC of 10 PPM/°C can be achieved.

Type THV Thin-Profile 10 KVDC Precision Resistor Voltage Divider Networks with Ratio TCs to 10 PPM/°C from -55°C to +125°C.

Caddock's advanced high voltage resistor technology combines our high stability Tetrinox® resistance films with laser-generated V-Notch Geometry (Pat. Pend.) to produce this compact high voltage divider network.

The performance of these high stability networks includes these special features:

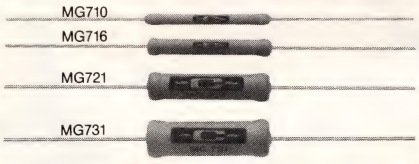
- Standard Input Resistance of 100 Megohm with custom resistances available.
- Standard Voltage Division Ratios of 1,000:1 or 100:1 with custom ratios available.
- Ratio Tolerances of 0.25%, 0.5%, 1.0% or 2.0% at 10 KVDC.
- Ratio Temperature Coefficients of either 10 PPM/°C or 25 PPM/°C from -55°C to +125°C.
- Non-Inductive Performance.
- Thermal coupling between the resistors in this single-substrate network provides excellent Ratio Temperature Coefficient stability.



- The thin-profile and 1.5 inch body length provides for easy packaging in space-sensitive designs.

Type MG Precision High Voltage Resistors with extended resistance range to 10,000 Megohm and a TC of 80 PPM/°C.

For greater **design flexibility**, Caddock's 'family' of Type MG resistors has been expanded with additional models and now includes 23 models that permit designers to select the optimum resistor size, power rating and voltage rating for each application, as illustrated by the four models of 4,000 volt, 1-inch long resistors shown here:



The Type MG high voltage, high stability resistors include all of these performance specifications:

- Standard Temperature Coefficient of 80 PPM/°C.
- Resistance values to 10,000 Megohm.
- Resistance Tolerances from 1.0% to 0.1%.
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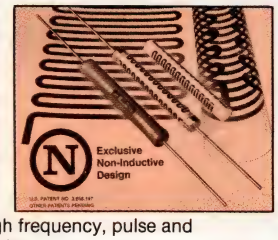
- Exclusive Non-Inductive Performance.

Most models of these high voltage resistors are manufactured with Caddock's Exclusive Non-Inductive Design for improved performance in high frequency, pulse and wide-band circuits.



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CIRCLE NO 170

ASIC-verification systems speed prototype testing, but system capabilities vary

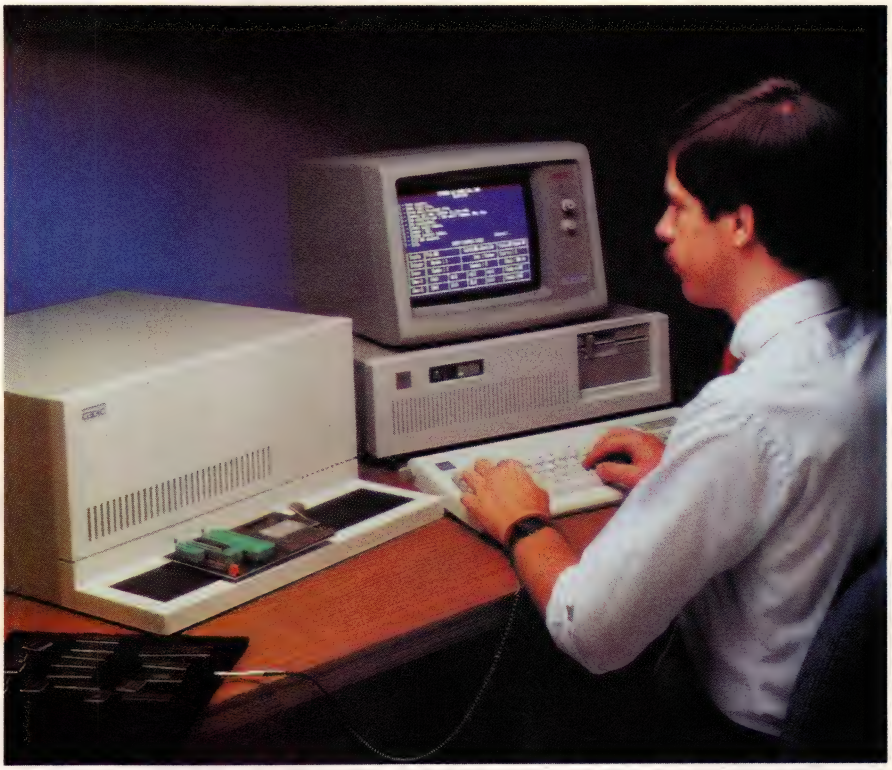
Chris Everett, *Regional Editor*

Today's design-verification systems test a prototype in much the same way that a production ATE system tests production parts. Unlike production testers, however, which are extremely difficult both to program and to use interactively, a verification (or prototype) tester makes it easy for you to set up test parameters, write a test program, and run the test by yourself. Because you can write your own test program for a verification system, the system gives you more control over the test than you'd have if you used an ATE system to test your protoype. Prototype testing will probably take much less time on a verification system than on an ATE system, therefore.

Design-verification systems originally consisted of just a pattern generator and a logic analyzer with a controller to coordinate the two. Now, however, they also provide ac parametric-measurement capabilities. Furthermore, in the past six months, several companies have added dc parametric-measurement capabilities to their systems. And vendors are incorporating still other measurement instruments—such as digitizers and arbitrary-waveform synthesizers—in their verification systems.

The primary purpose of a verification system is to tell you whether you've designed a device correctly. All verification systems can at least fulfill that objective. All the systems let you run a functional go/no go test on a device, and all let you display the expected-result vectors and the acquired-result vectors simultaneously.

Furthermore, the verification testers all have logic-analyzer-like analysis capabilities to varying degrees of sophistication. The Topaz analyzer from Hilevel, for instance, has a multiple-level trace control. You can selectively save only relevant data for analysis. Hewlett-Packard's 81800S analyzer includes 5-nsec glitch detection. The Hewlett-Packard 81800S, Hilevel Topaz-50, Integrated Measurement Systems (IMS) Logic Master 2000, and Tektronix Delta have real-time-compare capabilities, which speed your analysis.



Instead of hard-wiring the DUT socket board, *you can soft-wire the DUT socket on the 256-pin STM5100 verification system from Cadic. The system provides a menu that you use to control a switching matrix.*

Although all verification systems have the same basic functions—they can all basically generate a stimulus to a device under test (DUT), acquire the response, and display the results for you to analyze—the systems vary widely in their measurement and data-analysis capabilities.

When you're choosing a verification system, you'll probably base your choice on the number of pins (or channels), the speed, and the timing resolution it offers. The price of a verification tester, which ranges from about $30,000 to approximately $250,000, depends primarily on these three factors. The testers listed in the **table** on pg 62 are typical configurations; other configurations are available to suit a wide range of prototype devices.

Verification testers also differ in the user-interface features, test fixtures, test-pattern-generation tools, and data-analysis tools they offer, although in every case these features are relatively easy for a designer to use. The user interface on

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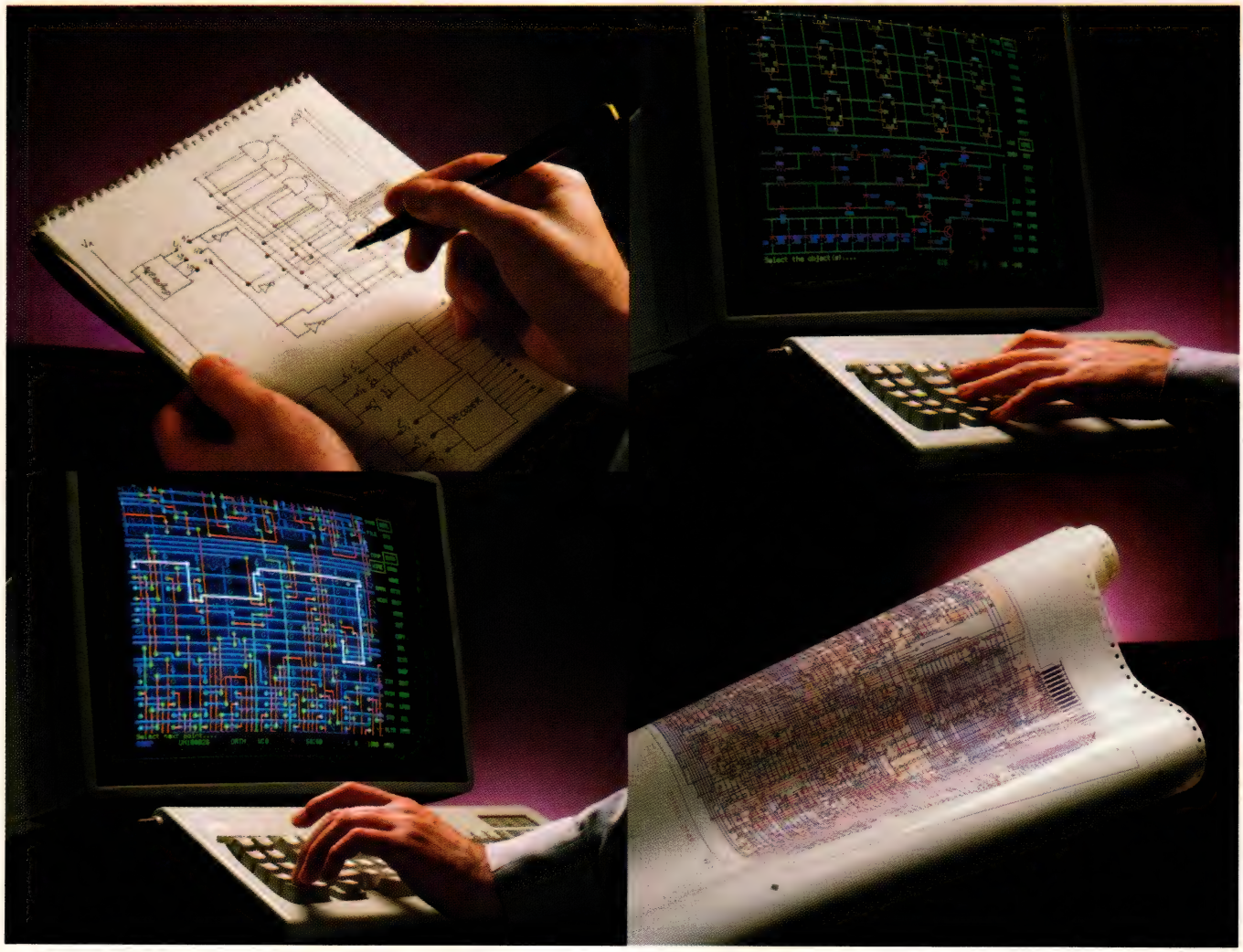

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the Cadic STM5100 verification tester, for example, is a series of menus. You use the main menu to select the task you want to perform: writing a test program, editing test vectors, running a test, or analyzing results.

If you choose to write a test program, the main menu will direct you to a series of setup menus. You don't need to learn a tester-programming language to write a program. Instead, you simply step through the setup menus.

Using the voltage-select menu, you set the supply voltage, the logic levels of the device under test, and the output threshold levels, all with 20-mV resolution. Using the system-timing table (a menu), you set clock speeds (to 10 MHz) and output strobe timing (to 1-nsec resolution) and assign the output pins to be sampled by each strobe.

The test vectors are stored in a separate file in the tester's host computer. You use the main menu again to read the vector file into the tester, and you call up the view-and-edit menu to review, change, or reformat your test vectors. The Cadic system requires a PC/AT host.

Recently, Tektronix added an interactive, window-based user interface to its Delta Series verification systems. Users of the Delta Series previously had to program a test sequence in C and then compile it and run it in batch mode. With Via, the new interactive user interface, you can now use a mouse and a series of pull-down menus to create and edit test sequences on the Delta Series systems. To use Via, you need an IBM PC/AT.

Interactive user interface

Fig 1 shows the pull-down menu you use to specify the voltage levels of the Delta's power supplies and to assign the tester channels to power rails. If you make an invalid entry, a help menu will pop up with status information or instructions. After you've developed a program, you send the complete test definition from the IBM PC/AT host to the Delta tester for execution. Three systems—Tektronix's DAS 92DV (the verification-system configuration of the company's DAS 9200 logic-analysis system), IMS's Logic Master 2000, and Hilevel Technology's Topaz—also use a menu-programming format to speed the development of test programs.

Verification systems have also made timesaving improvements in test fixtures. For example, when you use a production tester, you normally bolt the DUT socket board to the test head. When you use Hilevel's Topaz verification system, however, you simply clamp a test head over the edges of the DUT socket board.

A more time-consuming task, of course, is the wiring of the DUT socket board itself. With most testers, you must hard-wire the last two or three inches of the test paths between the tester and the socket that holds the DUT.

With the Cadic STM5100 tester, however, you use a setup menu on the host's screen to soft-wire the DUT socket board. The Cadic STM5100 is based on a tester-per-pin architecture. Each of the system's 256 pins has a driver and a receiver, and each can be programmed as an input, output, or bidirectional pin. The setup menu you used to soft-wire the tester controls a switching matrix that automatically wires the correct electronics to each pin. The wiring diagram—or, more correctly, the resource-allocation table—also becomes a part of the test program. When you want to test a different device, you read its test program into the Cadic tester, and the system automatically configures the DUT socket for the new part.

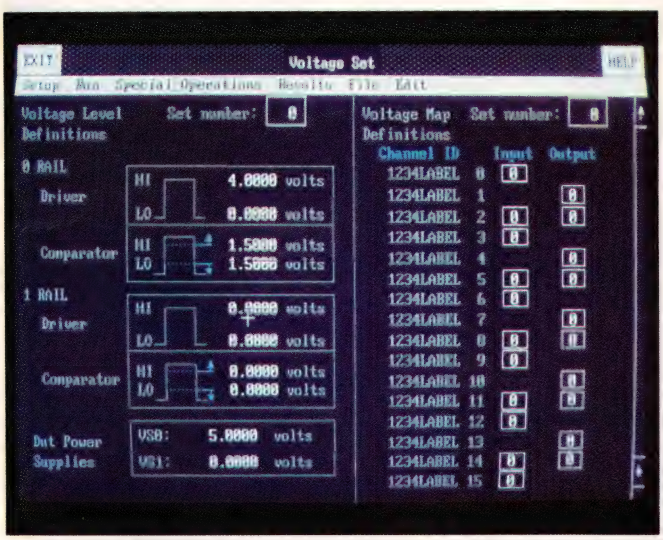


Fig 1—You use menus to enter test parameters *in a verification system, instead of writing your test program in a high-level language. This menu, the voltage-set menu on Tektronix's Delta system, lets you specify voltage levels.*

A CAE-to-verification link passes simulation vectors *to the test system's host, an IBM PC/AT, where the vectors are reformatted and debugged before being incorporated in the test program. The host also controls the operation of Tektronix's Delta system, a 192-pin tester with 100-psec timing resolution.*

After the tester has been configured, you can go to the calibration-select table and choose either an automatic or a manual calibration routine. In automatic mode, the tester selects the fastest data-acquisition strobe and the slowest channel and calibrates the system. If you use manual mode, you select the strobe and data channel the tester will use to calibrate itself.

Because of the STM5100's tester-per-pin architecture, the pins in each of its 16-pin add-on modules can be programmed, in any combination, as input, output, or bidirectional pins. Other verification systems use a different type of architecture. Hewlett-Packard's 81800S, IMS's Logic Master 2000, Step Engineering's Step-DAS, and Tektronix's DAS 92DV each have two types of modules: a stimulus (or input) module and a response (or output) module. The stimulus section is a data or pattern generator; the response section is a logic analyzer. Software and specialized buses tie the two sections together.

When you configure your tester to verify a specific device, therefore, you must have enough stimulus channels to support all the device's input-pin needs and enough response channels to support all the device's output-pin needs. You also need both an input and an output channel to support each bidirectional pin on your device.

The architectures of Hilevel's Topaz and Tektronix's Delta systems fall between the Cadic STM5100's flexible tester-per-pin architecture and the strict pattern-generator/logic-analyzer architectures of the other manufacturers' systems. The pins in each 16-pin module that you add to the Topaz can be either input or output pins. You can use all 16 as either input or output pins or eight as input pins and the other eight as output pins. All 16 pins can also be bidirectional; they operate together and are controlled by the data fed to the module's two strobe pins.

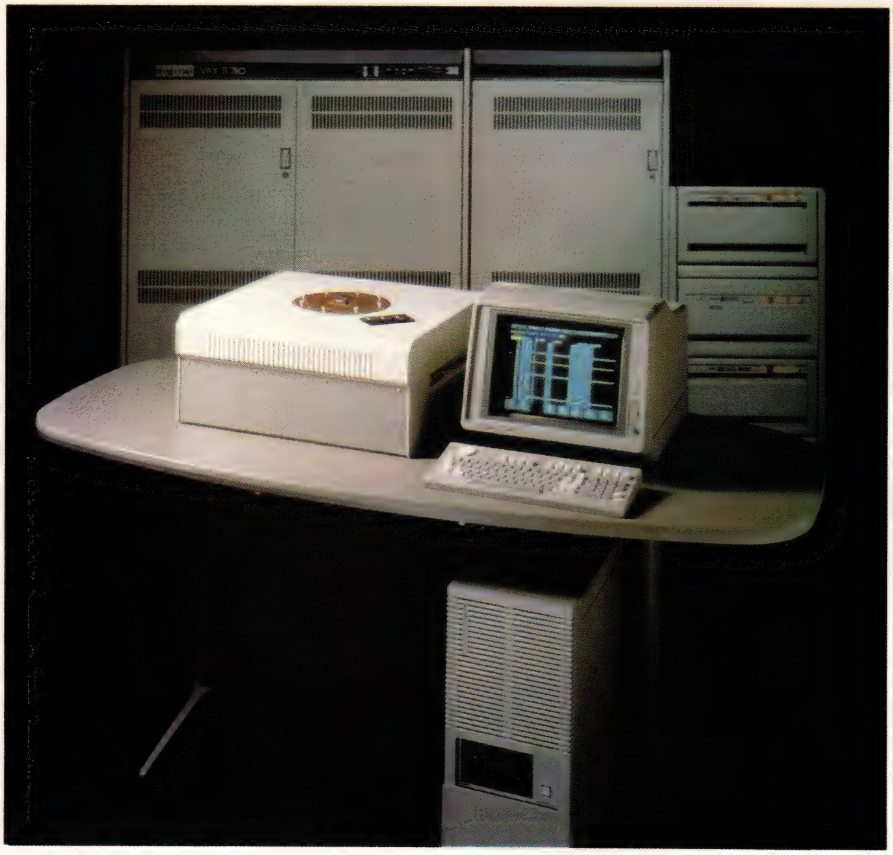
With each of the 24 I/O-channel modules for the Tektronix Delta, you get 24 input drivers and 24 output receivers, for a total of 48 pins. Although it's not immediately apparent from the Delta's data sheet, you can use the output receivers independently from the input driver pins.

CAE-to-tester links

Verification systems offer several different types of aids that speed test-pattern generation. The most common of these is a link between the verification system and a CAE system. In its basic form, this link serves simply to pass simulation vectors from the CAE workstation to the tester. Recently, verification systems have begun to offer vector-formatting and -verification tools as well.

With Tektronix's CAE link, for example, you can pass simulation vectors from Tektronix's Ideal, Gen-Rad's Hilo, Teradyne's Lasar6, Mentor Graphics' Quicksim, or Daisy's Megafault to an intermediate event-driven file format. The vectors are then translated to a Tek-

You can fit devices having as many as 512 pins into *one of the socket boards available for Hilevel's Topaz verification system. The Topaz-50 tests to 50 MHz and offers 500-psec timing resolution.*



A test fixture and specialized software *turn the Tektronix DAS 9200 logic-analysis system into the DAS 92DV verification system. The DAS 92DV has 179 input pins and 96 output pins; its timing resolution is 1 nsec.*

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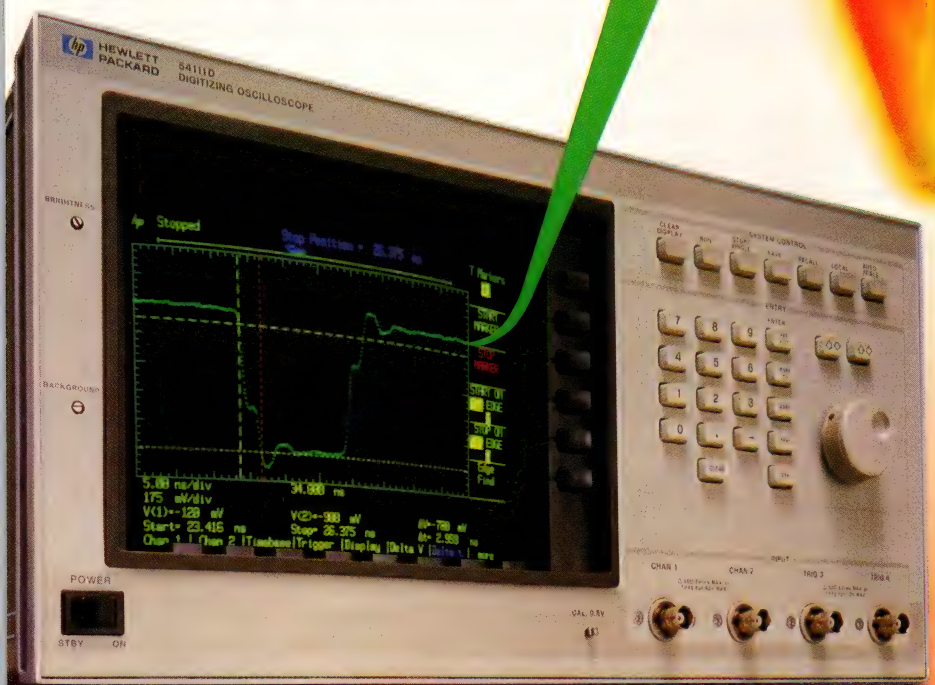

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tronix-defined state-wave format. At this point, any of the three Tektronix tester families—the DAS 9200, the Delta, or the LT-1000—can access the files. During the translation, the link reports to you any tester timing-violation problems, which would cause setup- and hold-time violations in the tester.

Cadic, Hilevel, IMS, and Step Engineering provide CAE system/verification tester links as well. IMS also offers a link between its Logic Master 2000 and an ATE system, Sentry from Schlumberger. After you complete your testing on the Logic Master 2000, you can convert your final vector set to Sentry-compatible vector files. If you don't have test vectors available to transfer, you can use the algorithmic pattern-generation tools on the Logic Master 2000 and Tektronix DAS 92DV systems to generate vectors.

50-MHz testing and 100-psec resolution characterize *Hewlett-Packard's 81800S verification system. For VLSI-device testing, you can operate two of the systems in parallel; together they provide 128 input pins and 64 output pins.*

Mnemonics generate vectors

Another pattern-generation aid is available from Step Engineering. The company offers tools that let you write test vectors and analyze test results in mnemonics instead of in binary or hexadecimal code. You use your own symbols and mnemonics to define the device architecture. You then write the vector pattern in a high-order language, using C-like constructs. You can mix bit-level coding with statements whenever and wherever necessary. After running the test, you use Step's disassembler to translate the binary results into your symbols and mnemonics for analysis. The Step-DAS, which ordinarily requires just a terminal, needs a PC/AT host to run the assembly-language development tool. Hilevel's Topaz, which provides a similar assembly-language pattern-development tool, also requires a PC/AT host.

Hilevel also offers two other test-pattern-generation aids. One of these, Wave-gen, lets you draw the test patterns on an IBM PC/AT. The Topaz test system converts the patterns to test vectors and runs the test. Wave-gen can speed setup-and-hold time studies, because you can easily vary pattern edges on the host's screen.

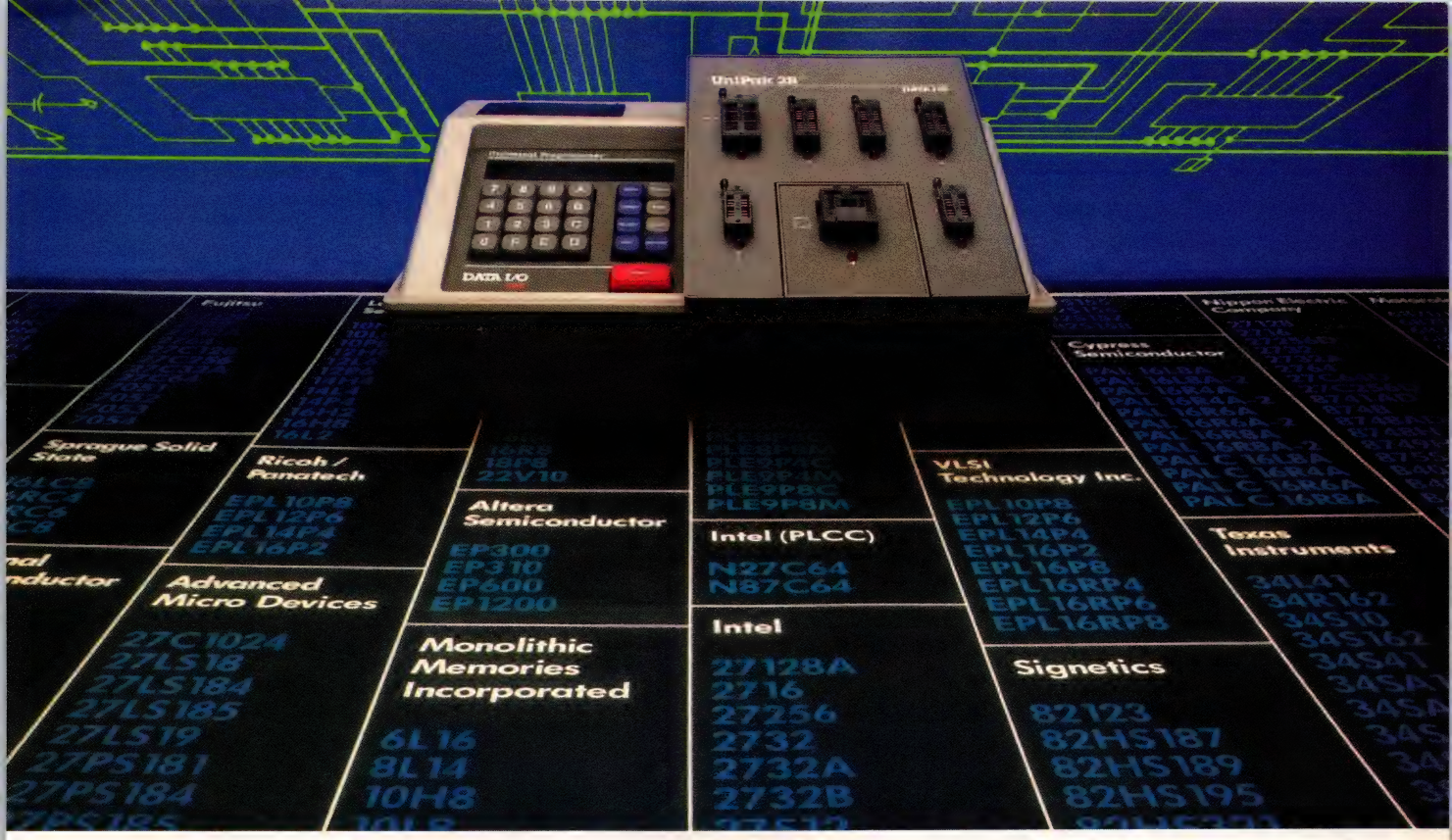
The company's other test-pattern-generation aid is a firmware-based vector generator. You define the width and depth of the vector

Specs can be confusing

Data-sheet specs for the different verification systems can sometimes be confusing: Some manufacturers use specifications similar to those for logic analyzers; others employ specs like those for ATE systems. IMS, for example, uses the term "data channels" to describe the stimulus and response channels in its system. Hilevel, on the other hand, uses the term "signal pins," a term familiar in ATE. Some manufacturers call a channel an I/O pin, which can mean a stimulus channel, a response channel, or a combination stimulus/response (bidirectional) channel.

Tektronix's Computer-Based Instrumentation Div uses the term "I/O channel" to describe the electronics of one stimulus channel and one response channel (or one input driver and one output receiver).

Another specification that goes by several different names is the spec for the number of timing generators that set the starting and trailing edges of the data patterns relative to the start of a test cycle. The data sheet for the Tektronix Delta uses the term "phases (start/stop pairs)"; the sheet for the same company's DAS 92DV data sheet calls them strobes. Step Engineering refers to them as pattern clocks. In the **table** on pg 62, they're labeled "timing-edge generators." A number of other verification-system parameters are also labeled differently on different products' data sheets.



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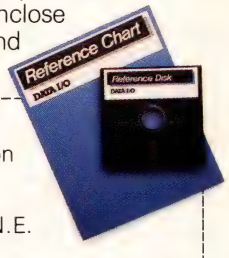

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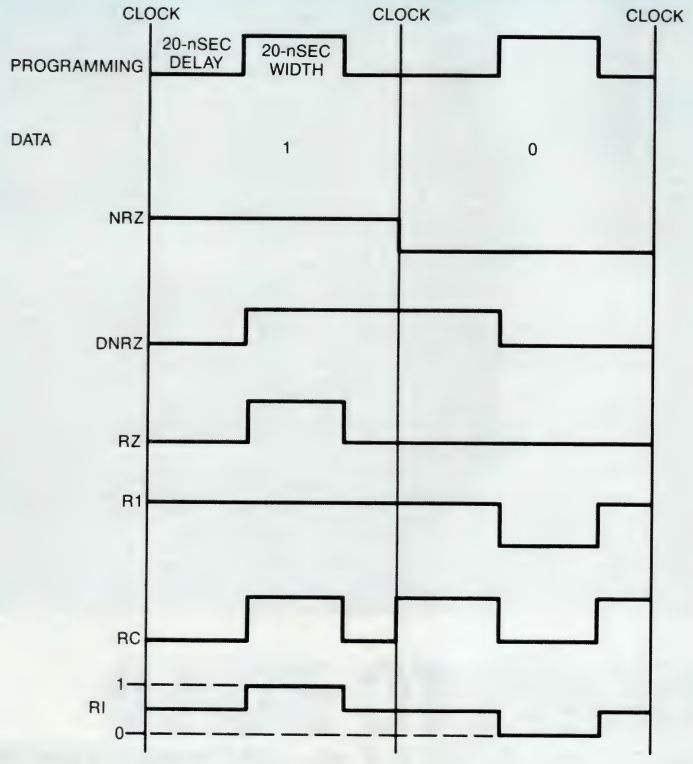

DATA FORMAT	DELAY (nSEC)	WIDTH
NRZ (NONRETURN TO ZERO)	0	CYCLE
DNRZ (DELAYED NRZ)	20	CYCLE
RZ (RETURN TO ZERO)	20	20 nSEC
R1 (RETURN TO ONE)	20	20 nSEC
RC (RETURN TO COMPLEMENT)	20	20 nSEC
RI (RETURN TO INHIBIT)	20	20 nSEC

Fig 2—To make high-resolution timing measurements, *you'll need a verification system that provides for a variety of data formats.*

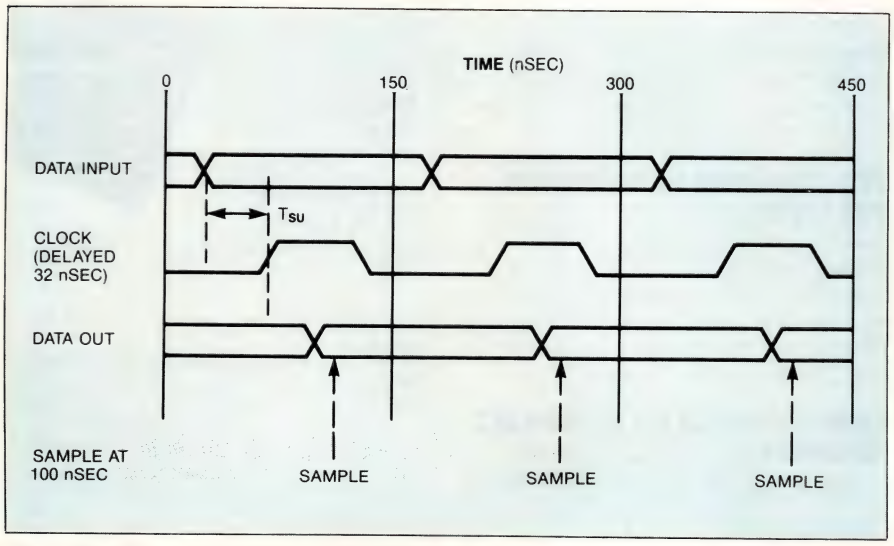

Fig 3—By using a combination of RC and RZ data formats, *you can make setup-time (T_{SU}) measurements on each of your device's input pins.*

pattern to be filled. The generator then fills the memory with walking ones, walking zeros, a sequential binary pattern, a checkerboard pattern, or random generated patterns.

Beyond functional testing

Several of these recent verification systems let you do more than just ensure that your device functions as intended: They can also help you find out whether your device is manufacturable—that is, whether it will function under a variety of operating conditions.

Several verification systems let you make ac parametric measurements, and three of the systems offer an option that lets you make dc parametric measurements. Unlike a timer/counter or a logic analyzer, which measure timing directly, a verification system makes ac parametric or timing measurements indirectly, by precisely setting and incrementing the edges of input patterns and then detecting the effects on the outputs.

To set up a timing measurement on a verification tester, you must control the shape and timing of data patterns on individual input pins and on the DUT's clock. Normally, a clock's waveform will have the shape of the top waveform in **Fig 2.** The clock's waveform format is a return-to-zero (RZ) format. Data normally enters a device under test in a nonreturn-to-zero (NRZ) format. To use your system to make timing measurements, you need to employ one of the other data formats—DNRZ, R1, RC, and RI—because they let you make discrete pulses within a test cycle.

To verify your device's setup time (T_{SU}), you would use an RC format for the data inputs. (**Fig 3** shows the test conditions for a verification of setup time.) You specify the start of the RC signal by setting the delay from the start of the test cycle to the signal's leading edge. You set the trailing edge in terms of the width of the pulse.

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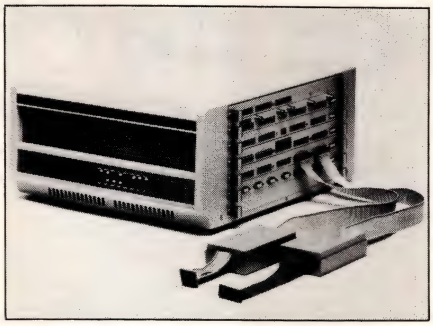
setup time on each pin individually, you must make sure that the data on the other input pins doesn't interfere with your measurement. Therefore, you need to set the delay on the RC data supplied to the pin under test so that it's long enough that the setup times of the other input pins won't affect the results.

You set the delay controlling the leading edge of the DUT's clock to be long enough so that the clock will trigger after the period comprising the delay on the RC data channel and the minimum setup time for the pin being tested.

You run the test several times. After each run, the RC delay increases by 1 nsec, thus decreasing the setup time by 1 nsec. When the test fails, the difference between the RC delay and the DUT's clock delay is the minimum setup time for that pin.

Setup-time measurement can also be made with DNRZ-format signals; hold-time measurements can be made with RC-format signals. Hilevel's Topaz, IMS's Logic Master 2000, and Tektronix's Delta Series provide six different data formats. Cadic's STM5100 provides 10; four of these formats are particularly suitable for bidirectional-pin applications.



You can add as many as 512 input and 512 output pins *to Step Engineering's Step-DAS verification system. The system simplifies test-pattern generation by letting you write programs in C-like constructs, using mnemonics and symbols that you define.*

DC measurement capabilities

For dc measurements, Hewlett-Packard, Hilevel, and IMS offer dc PMU (parametric measurement unit) options for their verification unit systems. IMS's PMU is integrated in the tester's architecture; it lets you make dc measurements on any DUT pin.

The Logic Master 2000 uses pop-up menus and canned measurement programs to speed the measurement process. If you want to make a gross leakage test, for example, you call up the gross-leakage-test menu and set the measurement values.

Traditionally, if you wanted to measure the input-pin loading and the output-pin drive levels into a load, you had to write a test program that sequenced the switching matrix and PMU through the hundreds of I/O pins on your DUT. With IMS's system, however, you can use special software that automatically develops a test program to measure the appropriate dc parameters at each of the I/O pins. The company supplies this software with the dc parametric option for the Logic Master 2000.

After you run the dc parametric test, the system gives you the measurement results. If a pin tests out of limits or if it isn't completely tested because the test pattern supplied to it does not change, the pin is flagged.

System can verify DSPs

To verify a mixed-signal device like a codec or a DSP, you can use two of the measurement capabilities of Tektronix's Delta verification system: a 2-channel, 25-MHz arbitrary-waveform synthesizer and a 2-channel, 400-MHz equivalent-bandwidth digitizer. You can trigger the digitizer anywhere within the test pattern and make timing measurements with 50-psec resolution. Voltage levels are resolved to 10 or 12 bits, depending on which sampling speed you use. **EDN**

For more information . . .

For more information on the verification systems described in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

Cadic Inc
7874 SW Nimbus Ave
Beaverton, OR 97005
(503) 626-7902
Circle No 701

Hewlett-Packard Co
1820 Embarcadero Rd
Palo Alto, CA 94303
Phone local office
Circle No 702

Hilevel Technology Inc
18902 Bardeen
Irvine, CA 92715
(714) 752-5215
Circle No 703

Integrated Measurement Systems Inc
9525 SW Gemini Dr
Beaverton, OR 97005
(503) 626-7117
Circle No 704

Step Engineering Inc
661 E Arques Ave
Sunnyvale, CA 94086
(408) 733-7837
Circle No 705

Tektronix Inc
(Delta Series)
Computer-Based Instrumentation Div
Box 500
Beaverton, OR 97077
(503) 627-7263
Circle No 706

Tektronix Inc
(DAS 92DV)
Logic Analyzer Div
Box 12132
Portland, OR 97212
(503) 231-1220
Circle No 707

Reference

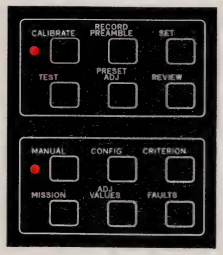
Verification Solutions, A Guide to ASIC Design Verification, Part Number 910-0061-002, Integrated Measurement Systems Inc, Beaverton, OR, 1986.

Article Interest Quotient
(Circle One)
High 503 Medium 504 Low 505

The technology of the future is recording data today.

No magnetic tape system made today measures up to the Honeywell Model 97.

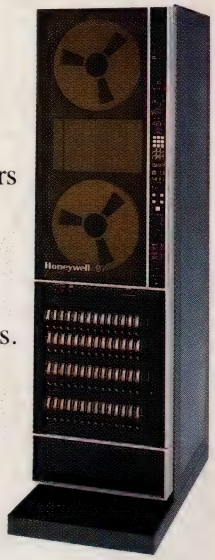
It's the only recorder with a transport that combines double vacuum buffering with a dual capstan drive system. This technology provides incredibly gentle tape handling and minimizes mechanically-induced artifacts with a 1000 Hz servo bandwidth for maximum flutter rejection and minimum TBE.



Auto calibration and test panel

The Model 97 has a computer-controlled feature set that includes:

- Direct electronics to 4.0 MHz, FM to 1 MHz and serial digital to 8 Mbps per track
- Integral time code generator/reader/search and control system
- Programmable tape management functions—search, shuttle and selective track recording
- Built-in record and separate reproduce meter monitors



The solid-ferrite heads of the Model 97 are so dependable that they're warranted for 5 years or 200 million feet of tape.

The Model 97 data system also has fully automatic calibration and test of its record and reproduce electronics. This eliminates the potential loss of data due to faulty manual calibration and setup.

The future is yours with the Model 97. For more information, contact Ed Haines, Honeywell Test Instruments Division, Box 5227, Denver, CO 80217. (303) 773-4834.

Together, we can find the answers.

Honeywell

CIRCLE NO 175

DESIGN-VERIFICATION SYSTEMS

COMPANY	MODEL	PINS	CONFIGURATION	TEST-CYCLE RATE (MHz)	VECTOR MEMORY DEPTH	STIMULUS			
						PROGRAMMABLE LOGIC LEVELS	LOGIC-LEVEL RESOLUTION	TIMING-EDGE GENERATORS	
CADIC	STM5100	AS MANY AS 256 (PROGRAMMABLE AS INPUT, OUTPUT, OR BIDIRECTIONAL PINS)	BASIC SYSTEM HAS 64 PINS; YOU ADD 16-PIN MODULES	10	32k BITS (PATTERN), 64k BITS (ACQUISITION)	YES	20 mV	8	
HEWLETT-PACKARD	81800S	AS MANY AS 128 INPUT, 4 CLOCK, AND 64 OUTPUT PINS IN TWO SYSTEMS OPERATING IN PARALLEL	BASIC SYSTEM HAS 2 CLOCK AND 8 OUTPUT CHANNELS	50	1k BIT	YES	10 mV	AS MANY AS 16	
HILEVEL	TOPAZ-50	AS MANY AS 256 (PROGRAMMABLE AS INPUT, OUTPUT, OR BIDIRECTIONAL PINS)	YOU ADD AS MANY AS 16 16-PIN MODULES PLUS LOGIC-ANALYSIS MODULES	50	4k OR 16k BITS (64k BITS WITH 25-MHz SYSTEM ONLY)	YES	10 mV	16	
IMS	LOGIC MASTER 2000	AS MANY AS 480 CHANNELS, WHICH CAN EITHER BE ALL INPUT OR OUTPUT, OR ANY COMBINATION IN 16-CHANNEL INCREMENTS	BASIC SYSTEM HAS 128 INPUT CHANNELS AND 128 OUTPUT CHANNELS. YOU ADD 16-CHANNEL INPUT OR OUTPUT MODULES	20	16k BITS	YES	10 mV	2 PER 16 CHANNEL INCREMENTS	
STEP ENGINEERING	STEP-DAS	AS MANY AS 512 INPUT AND 512 OUTPUT CHANNELS, 1 USER CLOCK INPUT, 1 INPUT AND 1 OUTPUT CONTROL LINE	YOU ADD AS MANY AS 8 64-CHANNEL INPUT MODULES AND AS MANY AS 8 64-CHANNEL OUTPUT MODULES	50	AS MANY AS 64k BITS PER INPUT CHANNEL AND AS MANY AS 32k BITS PER OUTPUT CHANNEL	ECL, TTL, OR CMOS LEVELS ONLY	N/A	1	
TEKTRONIX	DAS 92DV	AS MANY AS 179 INPUT CHANNELS AND AS MANY AS 96 OUTPUT CHANNELS	YOU ADD AS MANY AS 5 36-CHANNEL INPUT MODULES AND AS MANY AS 6 16-CHANNEL OUTPUT MODULES	50	1k BIT	TTL, ECL, USER-SUPPLIED VOLTAGES	N/A	1 FOR EACH RZ/R1 CHANNEL (PLUS 1 FOR EACH NRZ CHANNEL IF YOU USE DAS 9200 OPERATING SOFTWARE)	
	DELTA	AS MANY AS 192 (PROGRAMMABLE AS INPUT OR OUTPUT PINS) AND AS MANY AS 4 CLOCKS	BASIC SYSTEM IS 48 PINS; YOU ADD 48-PIN MODULES	20	16k BITS	YES	4 mV	3 START/STOP PAIRS PER 48 PINS	

					ACQUISITION				DATA ANALYSIS				
PATTERN-EDGE PLACEMENT RESOLUTION (nSEC)	PATTERN-EDGE PLACEMENT ACCURACY (nSEC)	CHANNEL-TO-CHANNEL SKEW (nSEC)	DATA FORMATS	PROGRAMMABLE THRESHOLD LEVELS	THRESHOLD-LEVEL RESOLUTION (mV)	DATA-ACQUISITION STROBES	STROBE-PLACEMENT RESOLUTION (nSEC)	REAL-TIME COMPARE	COMPARES EXPECTED RESULTS WITH ACQUIRED RESULTS	LOGIC-ANALYSIS MODE	DC PARAMETRIC MEASUREMENTS	PRICE
1	N/A	4	RTZ, R1, NR, DNR, DRTZ, DRT1 RTD, RTT, TTD, AND DTT	YES	20	2	1	NO	YES	YES	NO	$60,000 (64 PINS) TO $175,000 (256 PINS)
0.1	±1 nSEC ±5% OF PROGRAMMED VALUE	2	RZ AND NRZ	YES	10	1	0.1	YES	YES	YES	OPTIONAL	$64,000 (64 PINS)
0.5	±2 ±0.1% OF PROGRAMMED VALUE	1	NRZ, DNRZ, RZ, R1, XR1, AND XRZ	YES	10	1 PER 8 PINS	0.5	YES	YES	YES	OPTIONAL	$195,000 (192 PINS)
0.1	±1.5 (INCLUDES CHANNEL-TO-CHANNEL SKEW)	<1.5	NRZ, DNRZ, RC, R1, RZ, AND RI	YES	10	2 PER 16 CHANNEL INCREMENTS	0.1	YES	YES	YES	OPTIONAL	$185,000 (256 CHANNELS)
0.2	±1	2	NRZ IS STANDARD; DNRZ AND RZ FORMATS OPTIONAL	ECL, TTL, OR CMOS LEVELS ONLY	N/A	1	0.1	NO	YES	YES	NO	$30,000 (128 CHANNELS) TO $60,000
1	±1	<1	32 NRZ AND 4 RZ/R1 CHANNELS PER MODULE	YES	50	1	1	NO	YES	YES	NO	$100,000 (WITH 96 NRZ INPUT AND 96 OUTPUT CHANNELS
0.1	±0.5	±0.5	NRZ, RZ RZI, DNRZ R1, R1I	YES	4	1 PER 48 PINS	0.1	YES	YES	YES	NO	$60,000 TO $150,000

14 ways to change your mind, not your inventory:

CY7C291L
2048 × 8 PROM
35ns 60 mA

CY7C245L
2048 × 8
Registered PROM
25ns 60 mA

CY7C261
8192 × 8
Power Down PROM
35ns 100 mA
(I_{SB} = 30mA)

CY7C268
8192 × 8 32-Pin
Diagnostic PROM
40ns 100 mA

CY7C269
8192 × 8 28-Pin
Diagnostic PROM
40ns 100 mA

CY7C251*
16,384 × 8
Power Down PROM
45ns 100 mA
(I_{SB} = 30mA)

PALC16L8L
20-Pin CMOS
PAL® Device
25ns 45 mA

PALC16R8L
20-Pin CMOS
PAL Device
25ns 45 mA

PALC16R6L
20-Pin CMOS
PAL Device
25ns 45 mA

PALC22V10
24-Pin CMOS
PAL Device
25ns 90 mA

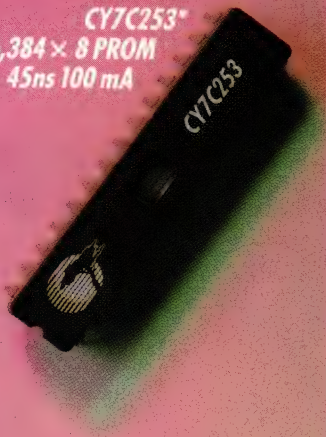
PLDC20G10
24-Pin Generic
Programmable
Logic Device
25ns 55 mA

FFFFAASS EPLD &

*available December, 1986

CY7C263
8192 × 8 PROM
35ns 100 mA

CY7C253*
16,384 × 8 PROM
45ns 100 mA



PALC16R4L
20-Pin CMOS
PAL Device
25ns 45 mA

ST CMOS RPROM.

The speed and power specs at the left are an indication of the *high performance* and *low power* you get with our CMOS PROM and PLD parts.

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All our parts work with industry standard programming tools, too.

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In addition to the world's fastest 16-bit slice (30ns) and our 4-bit slice (23ns) microprocessors, we offer the world's fastest 12-bit controllers, fast sequencers, 16 × 16 multipliers and multiplier/accumulators, plus many more high-speed CMOS circuits. Also, the fastest 64 × 4-bit and 64 × 5-bit cascadeable FIFOs (25 MHz commercial AND military performance). All very low power.

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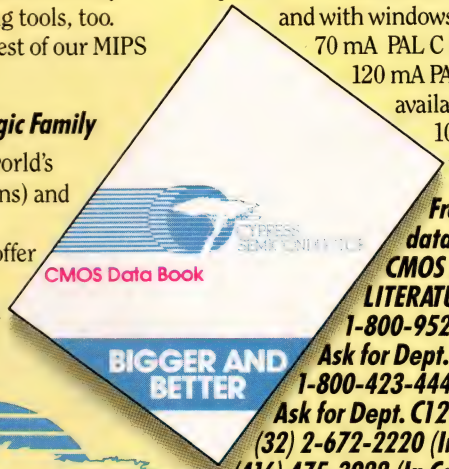

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CIRCLE NO 176

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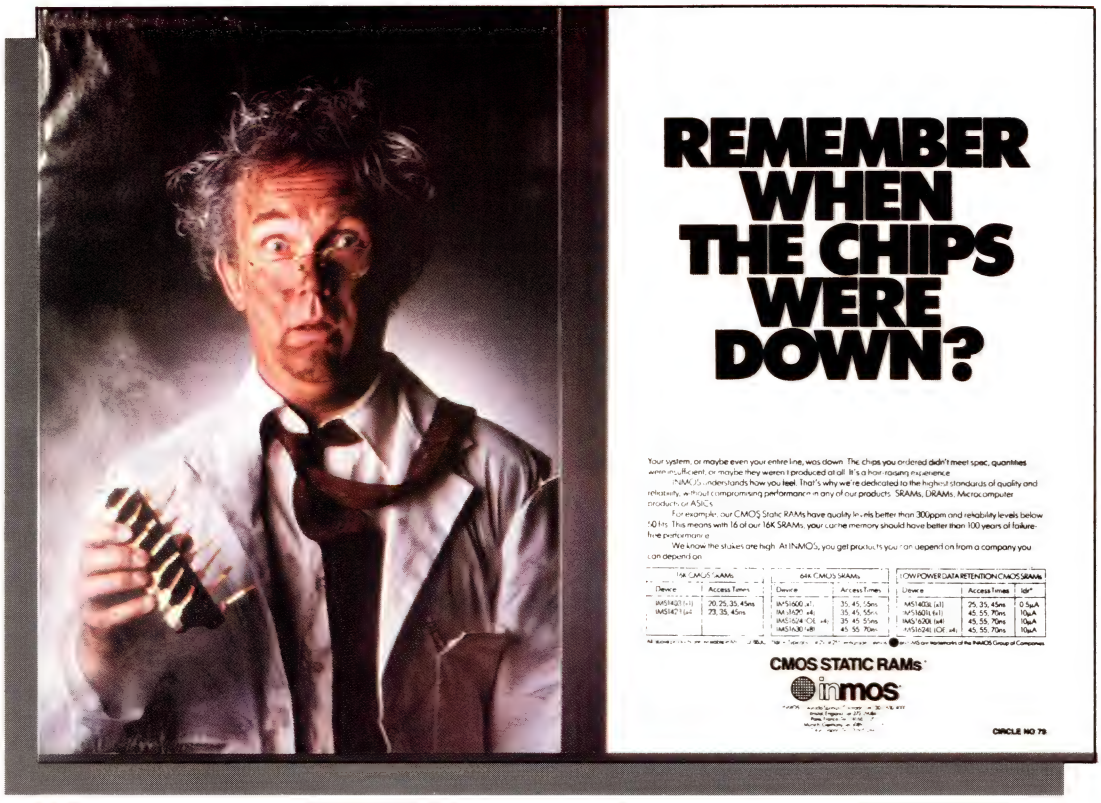

1st

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Senior Engineering Head
USN Ocean Systems Center

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Engineer
Hercules, Inc.

3rd

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MTS
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Senior Staff Engineer
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NASA

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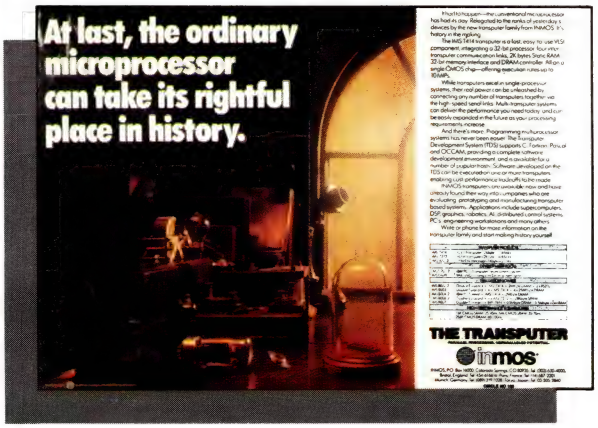

Company: INMOS Corporation
Agency: Thomas & Perkins

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Design & Development Engineer
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"Clever concept, like the product."

Production Manager
Centre Pad Systems

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Goodyear Aerospace

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Packard Electric Div.
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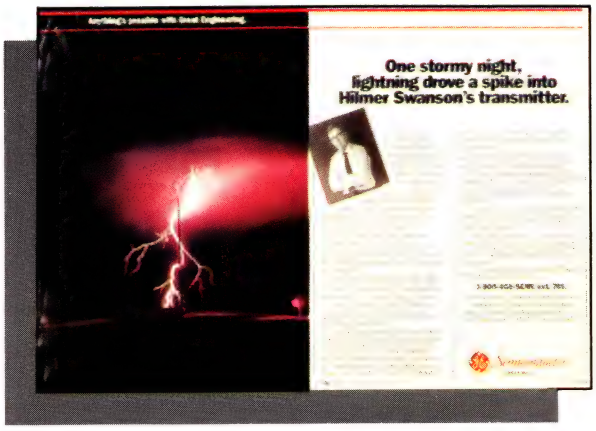
"Like the way it addresses 'Great Engineering.'"

Engineer
AT&T



Company: EXAR Corporation
Agency: In-house

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Avionics Engineer
Sikorsky Aircraft

"Complete and clear—exemplary ad."

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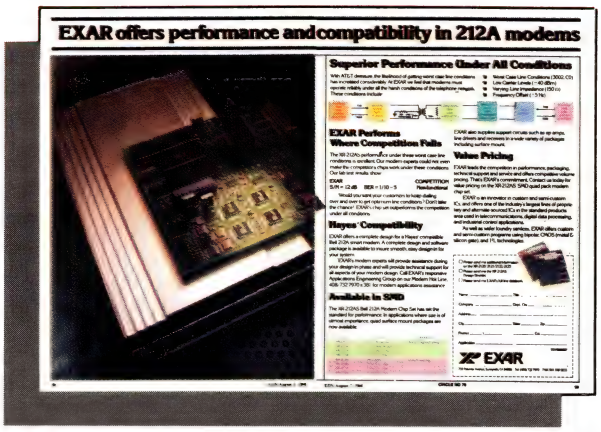
Group Engineer
Emerson Electric



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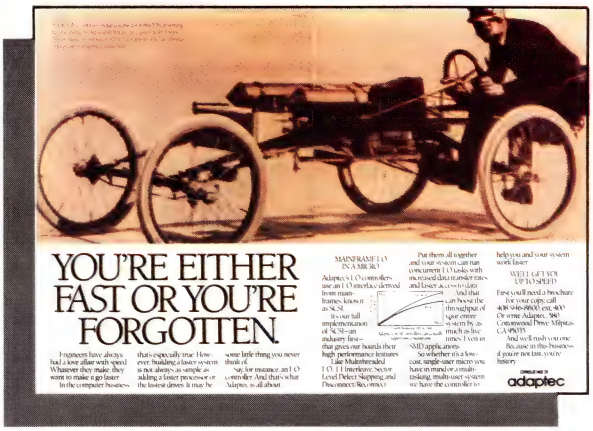

Company: Adaptec
Agency: Tycer Fultz Bellack

"Ad implies thrill of speed."

Senior Engineer
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Teledyne Systems

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Senior Engineer, Ai Research
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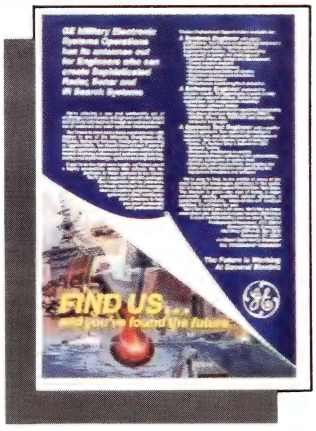
WINNING RECRUITMENT ADS



Company: GE Military Electronic Systems Operations
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"Bold color and good visual."

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Northrop

"Good company. Choice of jobs was of interest to me."

Systems Engineer
Digital Devices, Inc.

Company: Rockwell International Collins Transmission
Agency: Bernard Hodes

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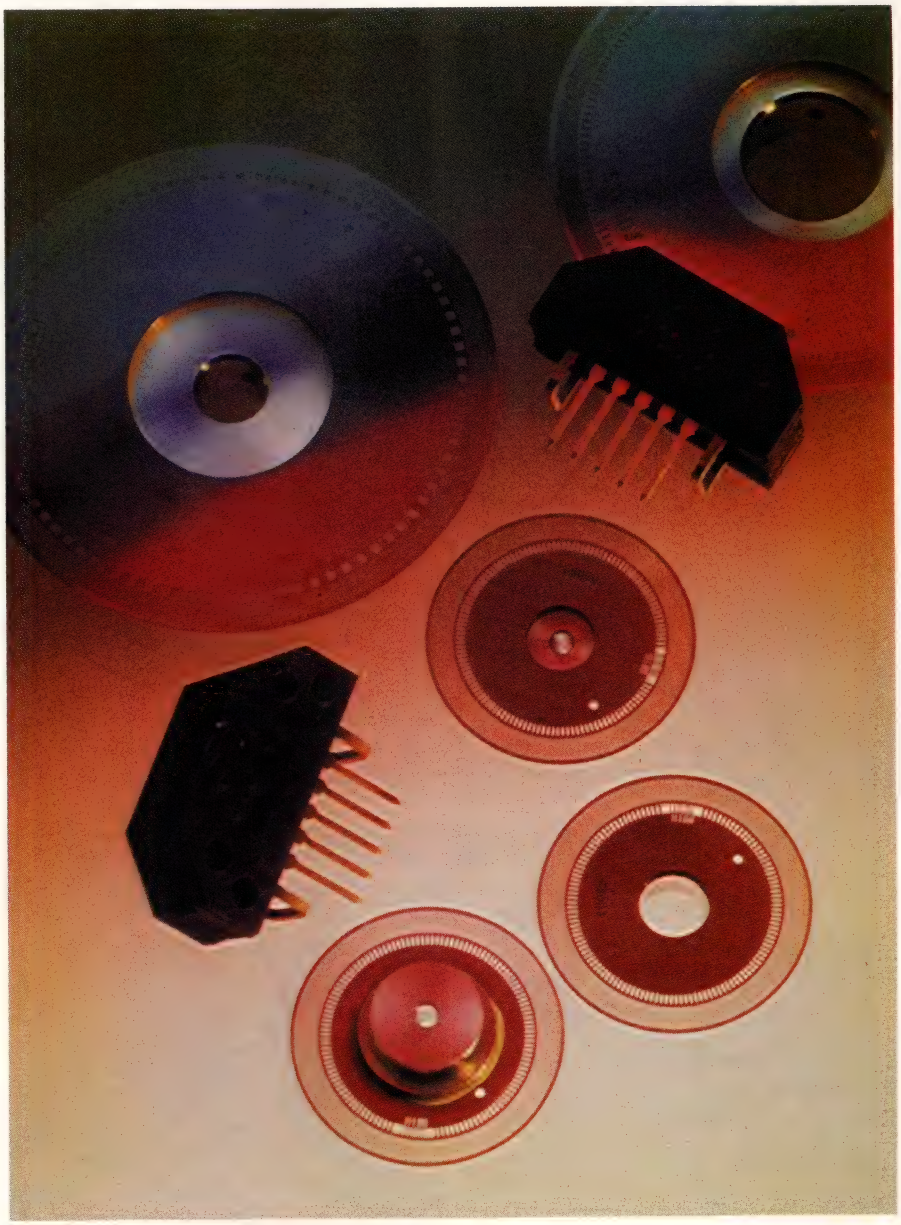
CIRCLE NO 115

Optical encoders are shrinking to satisfy position-sensing application requirements

Tom Ormond, *Senior Editor*



Thanks to its modular construction, *the HEDS-9000 module from Hewlett-Packard allows users a great deal of freedom in customizing their own incremental optical encoder.*

Computer, robotic, medical, and other high-performance electronic-equipment applications place stringent demands on position-control components. To satisfy these demands, manufacturers of digital optical encoders are offering smaller devices available in different guises, thus facilitating installation and use. Moreover, many of the optical encoders available today are less expensive than their predecessors.

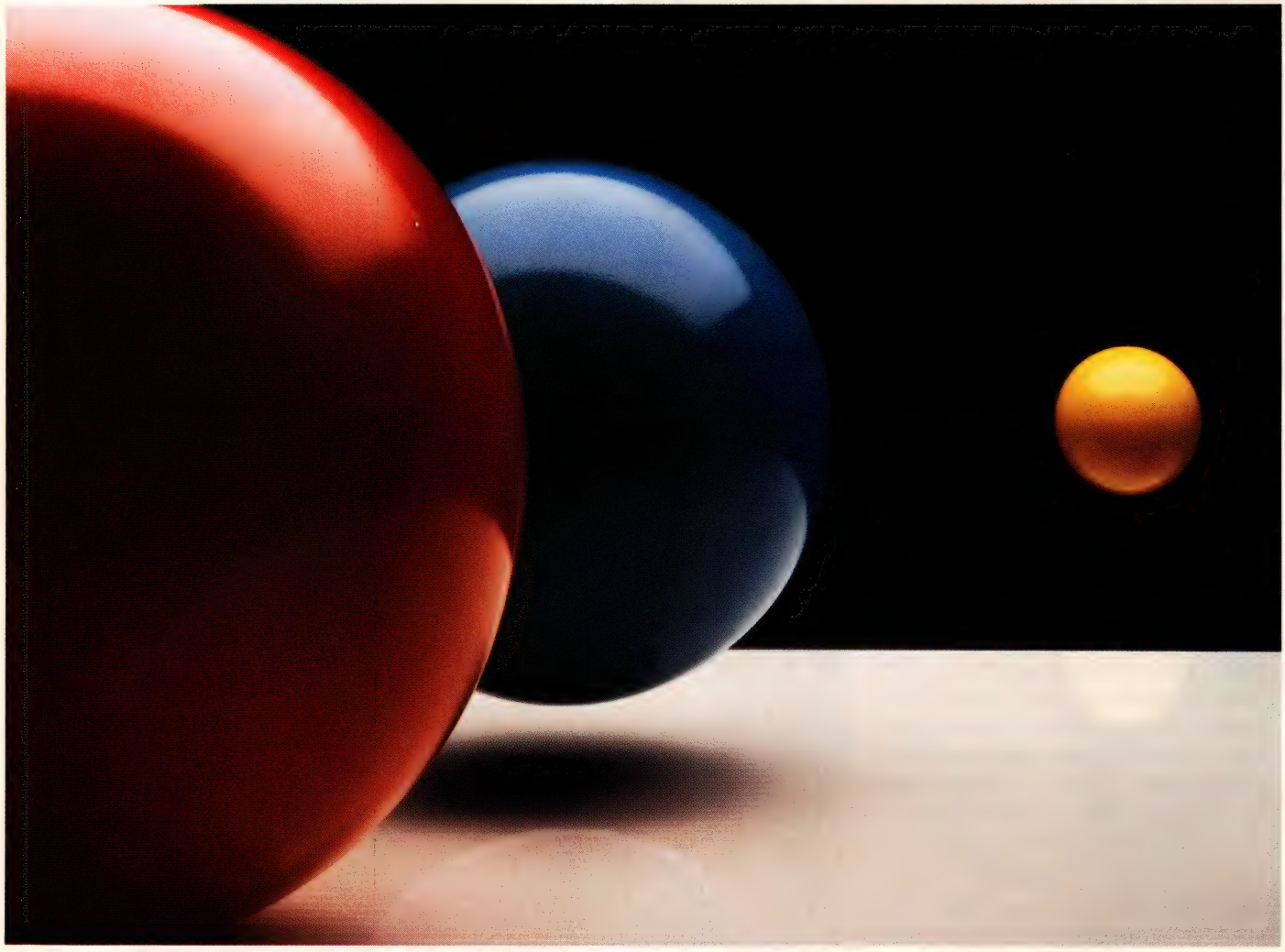
Optical encoders are noncontacting-type devices—that is, they have no brushes. They are also low-power devices and run much faster than do contacting-type encoders. Essentially, optical encoders consist of a coding disk, a light source, a light detector, and signal-processing electronics. Compared to other position-sensing components, such as potentiometers, proximity switches, and differential transformers, optical encoders offer a conceptually simple and straightforward encoding process. The two basic styles are called absolute and incremental.

An absolute encoder provides a whole-word output derived from a unique disk-code pattern representing each position. Independent tracks on the coding disk, which correspond to individual photodetectors, generate the code. Thus, the output from the detectors is high or low depending on the code-disk pattern for that particular position. Absolute encoders are capable of using thousands of different codes; the most common are Gray, natural binary, and binary coded decimal.

In contrast, an incremental encoder's disk has a series of equally spaced radial lines rather than a unique pattern. This type of encoder's output consists of a series of pulses, the number of which determines the shaft position relative to some reference point.

The incremental encoder is a simpler device than its absolute counterpart because it only has to generate a repeated signal for equal increments of shaft angle. It can also sense shaft-rotation direction using one additional code sensor. An incremental encoder features simple

Reach out for good ideas



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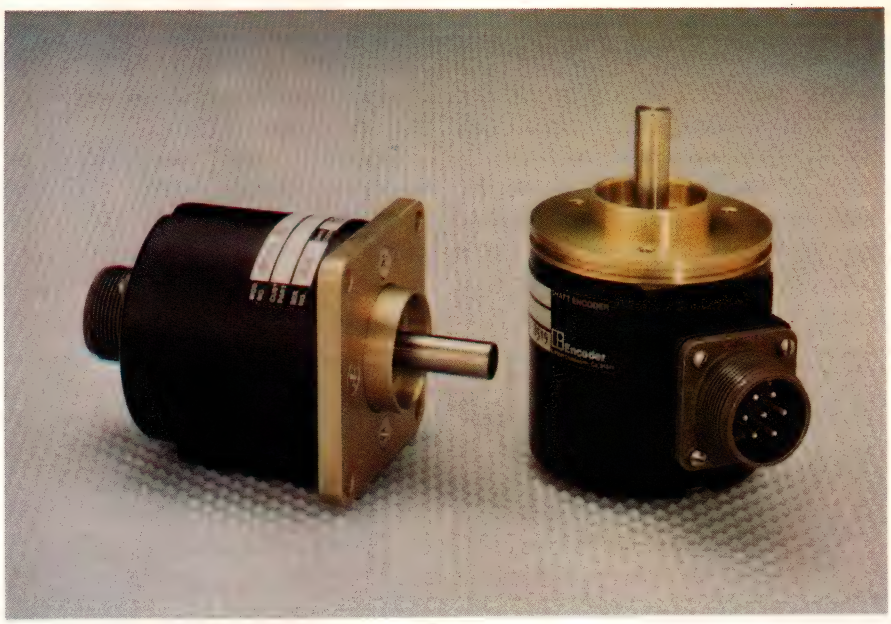
One good idea after another.

circuitry, modest power requirements, and high resolution. Nonetheless, an absolute encoder has one advantage: It retains position information during a power failure.

When it comes to selecting an optical encoder, you'll find quite a variety to choose from. You can, for example, buy an encoder in kit form or one that's already completely assembled. You can also buy individual piece parts, essentially customizing the components into an encoder. You can, in fact, even buy an encoder complete with a motor—an alternative that provides a very simple, comprehensive approach to position sensing.



Offering resolutions ranging to 2540 cycles, *Litton's Model 80 encoders provides quadrature outputs that are DTL, TTL, or CMOS compatible. They operate at 100 kHz.*

Taking the incremental approach

Data Technology, Sequential Information, Disc Instruments, and Litton all offer completely assembled encoders. Data Technology's MS58 incremental encoder is designed for industrial-automation applications. Packaged in a compact housing (58 mm in diameter and 72 mm long), it has a standard operating frequency of 100 kHz and is available with 50 to 5000 lines on the encoder disk.

Priced at $410 for a 5000-line model, the MS58 has a single high-powered infrared LED light source (GaAlAs) that has a minimum operating life of 150,000 hours (5-year warranty). A monolithic photodiode array, consisting of differential pairs, provides the signals for the encoder's three output channels. This scheme achieves a consistently stable output regardless of voltage and temperature variations. The encoder specs an accuracy of ±6 arc-sec for adjacent transitions.

The MS58 is immune to problems associated with electrical interference caused by high-powered switching drives and conductors close to the encoder cable. It features an internal dual Faraday shield, which establishes an electrostatic barrier that diverts electrical interference to the ground conductor. The encoder can withstand noise spikes of 60V peak amplitudes and 100V/μsec rise and fall times between the encoder housing and circuit ground.

The standard MS58 has a CMOS differential line driver (MM88C30). A TTL differential line driver (DM8830) is available as a no-cost option. The differential line drivers minimize the effect of transmission-line noise injected into the encoder cable by adjacent conductors. Operating range is 0 to 70°C, and standard supply requirements are 5V at 150 mA max (12V optional).

Packaged in a 3-in.-diameter NEMA housing, Sequential Information Systems' Model 30GN offers industrial users an incremental encoder capable of withstanding 220-lb radial and axial shaft loads. Four standard shaft diameters are available: ⅜, ½, ⅝, and ¾ in.

Priced between $250 and $375, the Model 30GN is designed to operate in industrial environments where rugged construction and the ability to withstand heavy shaft loading are necessary. It has a single LED light source; is impervious to dirt, moisture, and oil; and uses a spaced bearing assembly to improve shaft loading capability. The encoder also has high-level phototransistor detectors for high noise immunity.

You can select resolutions ranging to 2540 cycles/revolution, and you have a choice of outputs—square wave, single or quadrature, and a once-per-revolution zero pulse. Self-contained count-multiplication and direction-sensing logic multiplies the basic disk resolution 1, 2, or 4 times, providing the encoder with as many as 10,160 pulses/revolution. The outputs are available in TTL-, HTTL-, or CMOS-compatible formats and in single-ended, complementary or line-driver configurations. When ordering, you may choose flange or servo mountings, a rear- or side-exiting connector, and sealed bearings or heavy-duty shaft seals.

Modular encoders are for sale

The HDM Series, modular incremental encoders from Disc Instruments, are specifically designed for those applications requiring high performance, small size, and low cost. To meet motor-mounting and space requirements, the encoders—$29.50 (1000)—are available in three versions: size 11, 15, and 20. All have a height of 0.65 in. max. A quadrature output is standard, and

an index output is available as an option.

The encoders' sensor array and the photoelectric signal-processing circuitry are incorporated into a 0.4-in.-square hybrid circuit; all passive components are surface mounted on one pc board. A custom collimated infrared-LED/lens combination works in conjunction with the radial in-line sensor array to increase motor-mounting tolerances and to improve performance sensitivity to radial and axial end play.

Standard performance characteristics specify a 500-kHz operating frequency and 67.5° edge separation. A number of standard resolutions are available: 5 to 1200 pulses/revolution for size 11 and 15 versions, and 5 to 2000 pulses/revolution for size 20 units. The encoders operate from 5, 12, and 15V dc supplies and draw only 30 mA.

Glossary of optical-encoder terms

If this is your first attempt at selecting encoder-type position sensors, you might have trouble with some of the parameters you'll find listed on the data sheets. The following glossary will help clear up some of the confusion and simplify the evaluation process.

Ambiguity—Inherent error arising from multiple bit changes in a polystrophic code when going from one digit to an adjacent digit.

Angular misalignment—The maximum deviation in perpendicularity between the encoder shaft and the face of the mounting surface, representing the shaft-misalignment, shaft-runout, and mounting-face-runout totals measured at the worst respective positions.

Axial load—The maximum axial force that may be applied in either direction without affecting encoder life.

Capacity—The total number of counts available from an encoder.

Error—The algebraic difference between the indicated value of the input and the true value.

Monostrophic code—A binary code in which only one bit changes between any two adjacent code positions.

Mounting error—The error resulting from mechanical deformation of the transducer during the mounting process.

Operating speed—The maximum angular velocity at which an encoder may operate and still maintain specified accuracy.

Polystrophic code—A binary code in which for at least one count transition, two or more bits must change simultaneously while going from one adjacent code position to another.

Quantization error—The inherent fixed error associated with digitizing an analog shaft position.

Repeatability—The ability of a transducer to reproduce output readings when the same input value is consecutively applied in the same manner and in the same direction.

Resolution—A measure of the smallest input change that an encoder can detect.

Slew speed—The maximum velocity to which you can accelerate an encoder and still retain full accuracy when you slow it below its minimum speed.

Zero reference—An output signal produced once in some specified displacement (usually once per revolution). It's useful for power-fail recovery, error checking, or calibration.

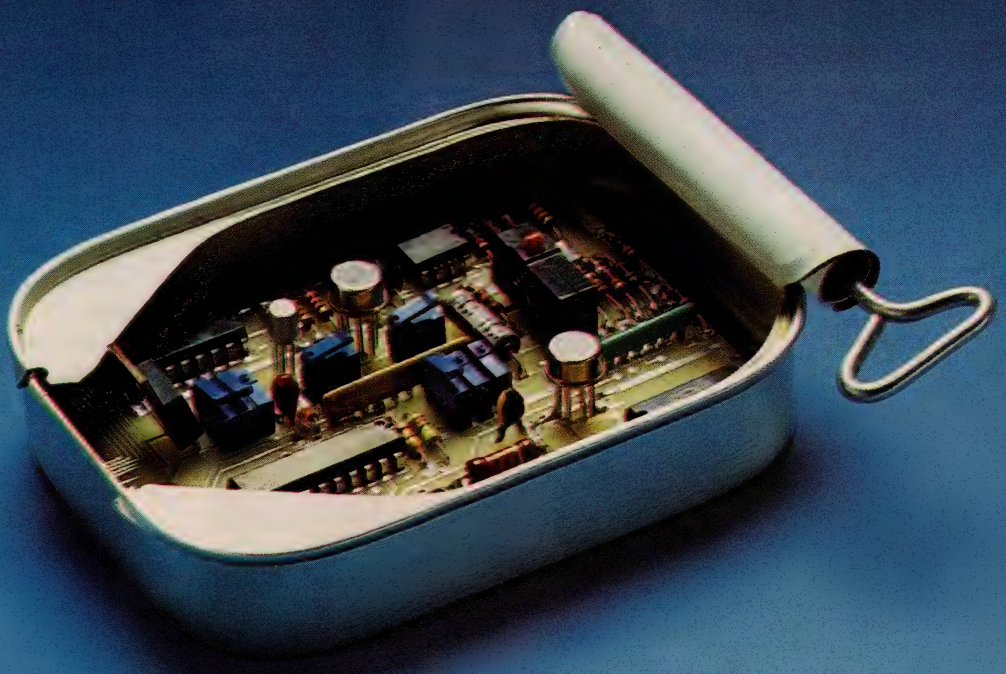
Handling moderate resolution

Litton's Model 22—$195 (100)—is a medium-resolution, absolute shaft-position encoder. Designed for applications where space is at a premium, it weighs only 6 oz, has a 2.187-in. diameter, and is 2.5 in. long. The encoder uses LED light sources for high reliability and long life (100,000 hours min). Internal electronics generate TTL- and CMOS-compatible 9-bit Gray code outputs. Shaft rotation is continuous and reversible. The direction of the encoder's ascending count is pin selectable.

Slewing and operating speeds are 3000 and 1000 rpm, respectively. Starting torque is 0.5 in.-oz max, and moment of inertia equals 600×10^{-6} oz-in.-sec^2 max. You can choose from three operating voltages: 5V (150 mA), 12V (100 mA), and 24V (50 mA). The encoder's operating range spans 0 to 55°C.

If you'd rather assemble your own encoder or if you'd prefer to do a little customizing, you can turn to manufacturers such as Hewlett-Packard or PMI Motion Technologies. The HEDS-9000 from Hewlett-Packard is a low-cost—$20.50 (250)—optical incremental encoder module that consists of an LED emitter and a detector IC enclosed in a small C-shaped plastic package. Operating with an appropriate code wheel, the module translates the rotary motion of a shaft into a digital 2-channel quadrature output.

The unit's light source is collimated into a parallel beam by means of a single lens located directly over the LED. An IC located directly opposite the light source comprises multiple sets of photodetectors and the signal-processing circuitry necessary to produce the digital output waveforms. The highly collimated light source and special photodetector array allow the module to toler-



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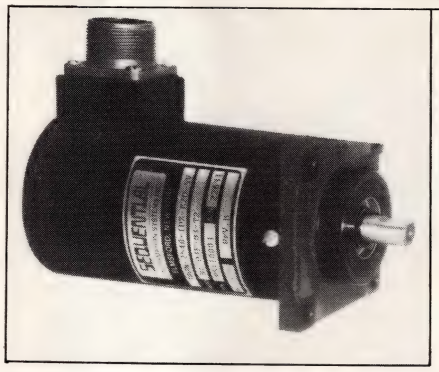
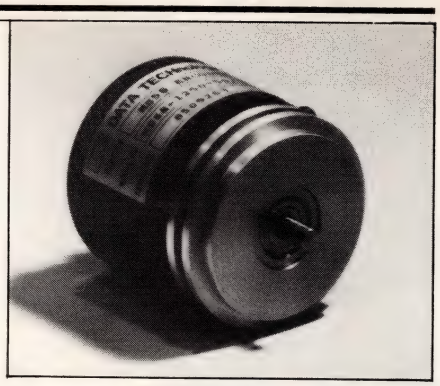


Designed to operate in industrial environments *where rugged construction is a necessity, the Model 30GN incremental encoder from Sequential Information Systems can withstand 220-lb radial and axial shaft loads.*



To achieve high noise immunity, *the MS58 encoder from Data Technology employs an internal dual Faraday shield, which establishes an electrostatic barrier and diverts electrical interference to the ground conductor.*

ate great mechanical variations during assembly and operation.

Although the HEDS-9000 is designed to operate with the manufacturer's HEDS-5100 and -6100 Series code wheels (which offer standard resolutions of 360, 500, and 1000 counts/revolution), you can substitute your own code wheel. In addition, the HEDS-9000's modular construction allows you a wide degree of freedom in selecting the shaft diameter and external housing to fully customize your encoder.

The HEDS-9000's special photodetector design also enhances its encoding performance. The logic-state-width error of the quadrature outputs typically varies by no more than five electrical degrees. Typical figures for phase error and pulse-width error are two and seven electrical degrees, respectively. The module is TTL compatible and operates from one 5V supply over −40 to +100°C.

PMI Motion Technologies' compact (1.65 in. in diameter by 0.84 in. high) M15 modular incremental encoders are available in kit form. The

For more information . . .

For more information on the optical-encoder products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

Data Technology Inc
4 Gill St
Woburn, MA 01810
(617) 935-8820
Circle No 708

Disc Instruments Subsidiary
Honeywell Inc
102 E Baker St
Costa Mesa, CA 92626
(714) 979-5300
Circle No 709

Hewlett-Packard Co
1820 Embarcadero Rd
Palo Alto, CA 94303
Phone local office
Circle No 710

Litton Systems Inc
Encoder Div
20745 Nordhoff St
Chatsworth, CA 91311
(818) 341-6161
Circle No 711

PMI Motion Technologies
49 Mall Dr
Commack, NY 11725
(516) 864-1000
Circle No 712

Sequential Information Systems Inc
249 N Saw Mill River Rd
Elmsford, NY 10523
(914) 592-5930
Circle No 713

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Motor Div
2275 Stanley Ave
Dayton, OH 45404
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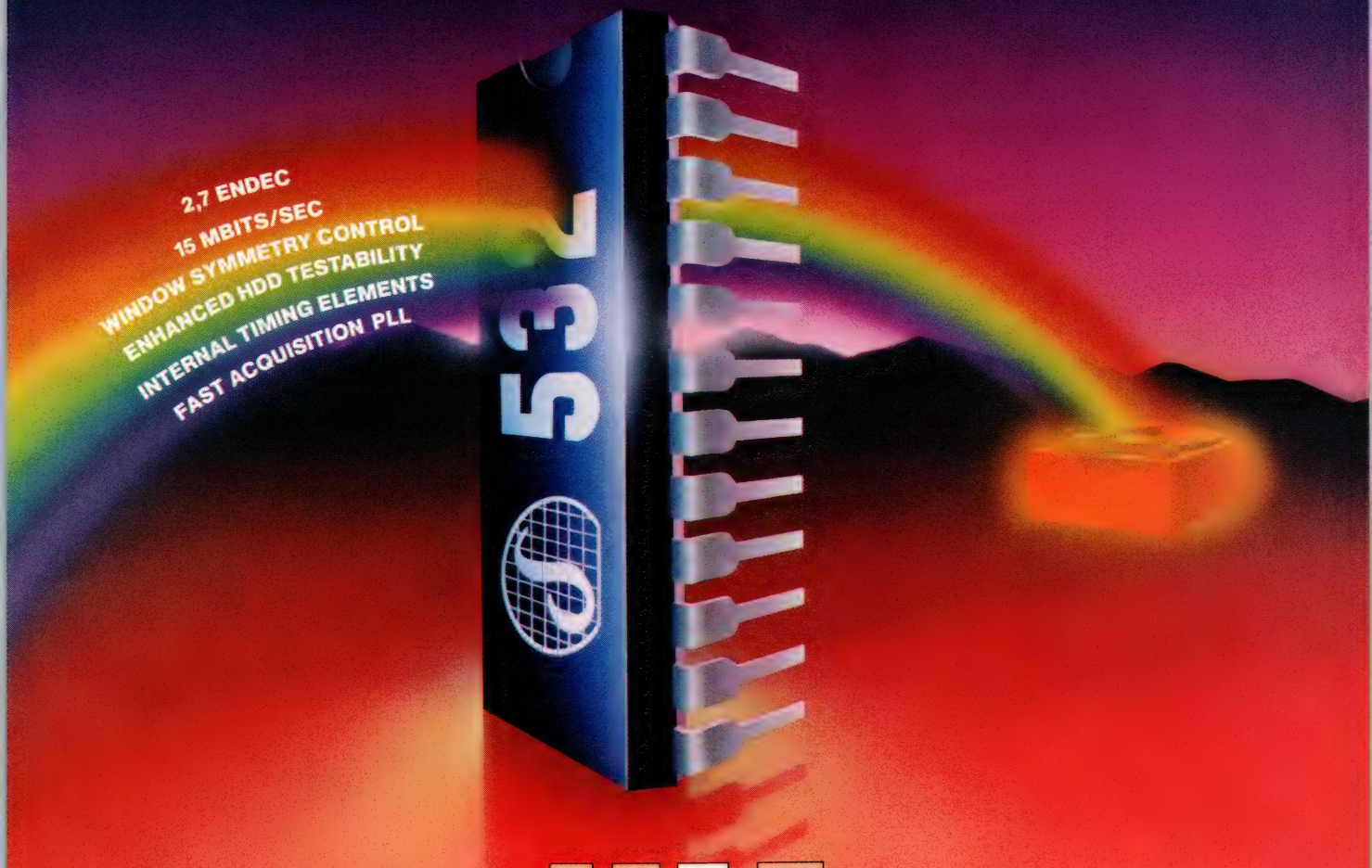
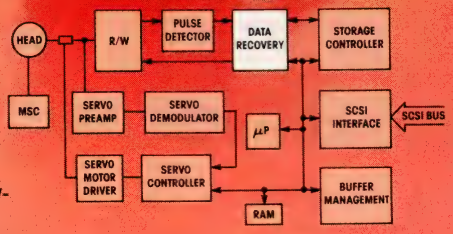


For mass storage disk drive electronics—Silicon Systems supports you best with total "head to host" IC solutions. Example: the Silicon Systems Data Recovery IC family. The flagship of this exciting new series is the SSI 532—the industry's most advanced single chip solution integrating data synchronization and ENDEC functions. Designed as a companion device to the SSI 452 and AIC 010 families of controllers, the 532 is destined to become the industry standard. And for good reason: it offers the type of raw performance and exclusive enhancements that really can separate your hard disk drive from the rest.



Just look at what this space-saver offers: 2,7 RLL encoding/decoding; window symmetry control with μP port for enhanced HDD testability; internal timing elements with a single external resistor to set the data rate; a precision decode window without the requirement of an accurate 1/4 cell delay; 15Mbits/sec. operation; fast acquisition PLL; plus a host of other dynamic features that will give your product the competitive edge.

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For more information on the SSI 532 and other exciting product families in the SCSI chip set, contact Silicon Systems today.

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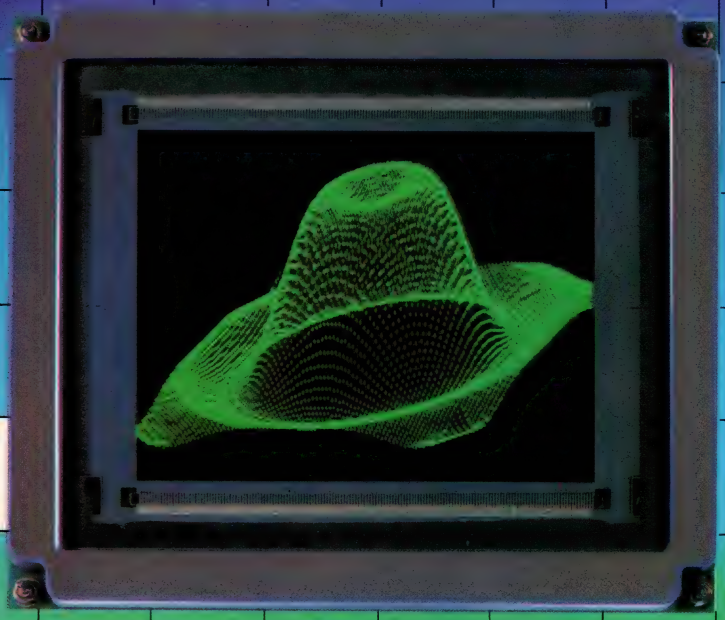
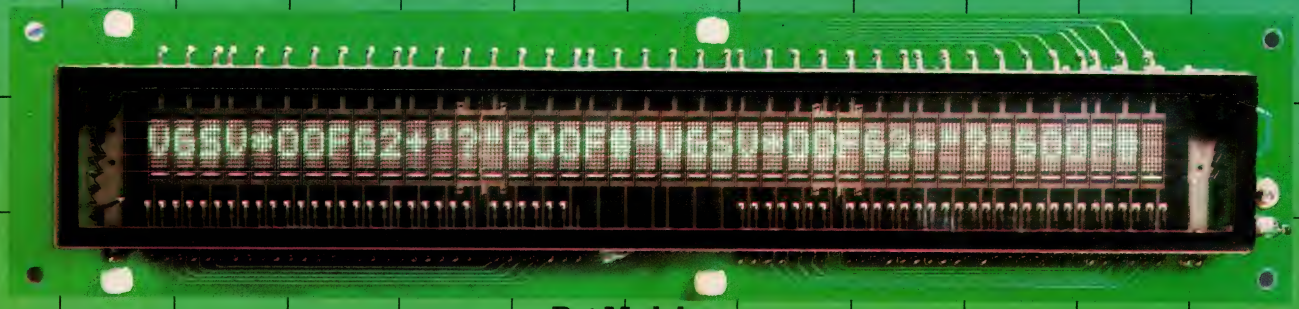


Graphic Module



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GP1006	256 × 64	0,65	166 × 41,4	VFD	40 × 6
GP1009	240 × 64	0,45	107,9 × 28,7	VFD	40 × 6
GP1001	320 × 120	0,375	120 × 45	FLVFD	52 × 12
GP1002	320 × 240	0,375	120 × 90	FLVFD	52 × 24

Inquire for single color Graphic Module

Dot Module Series List

Type code	Characters × Line	Dot Construction	Character Size	Nos. of displaying characters
M20SD01CA	20 × 1	5 × 7 dot	3.5 × 5.0	222
M20SD42CA	20 × 1	5 × 12 dot w/cursor	3.5 × 8.75	222
M40SD02CA	40 × 1	5 × 7 dot w/cursor	3.5 × 5.0	222
M40SD42CA	40 × 1	5 × 12 dot w/cursor	3.5 × 8.75	222
M202SD03CA	20 × 2	5 × 7 dot w/cursor	3.5 × 5.0	222
M402SD04CA	40 × 2	5 × 7 dot w/cursor	3.5 × 5.0	222

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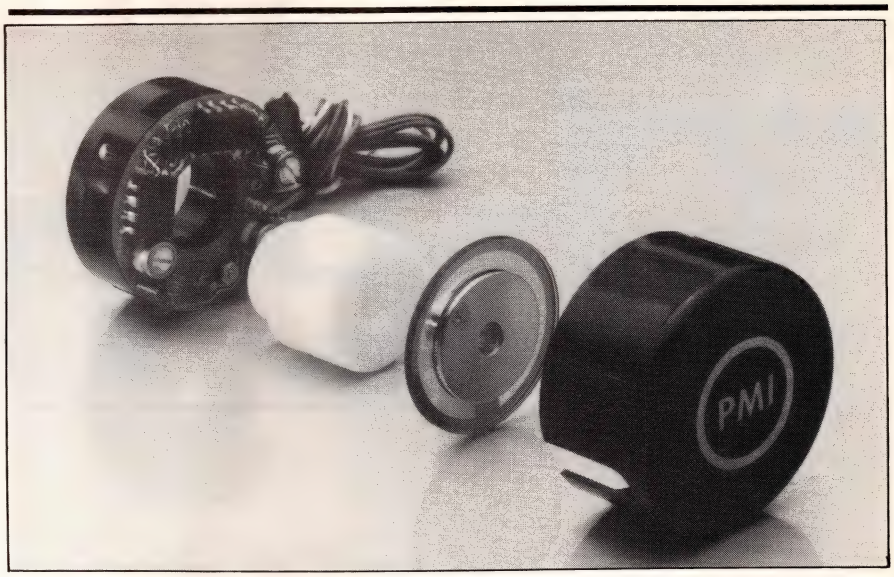
TECHNOLOGY UPDATE

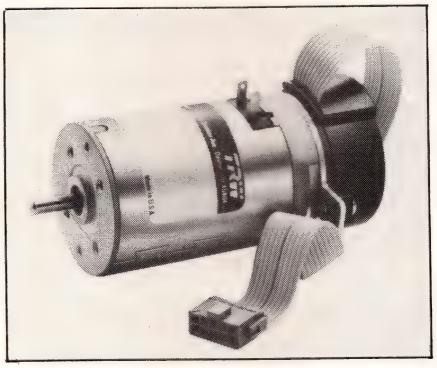


Offering track densities ranging to 1200 counts/revolution, *M15 encoders from PMI Motion Technologies feature a patented pre-alignment scheme that eliminates the need for phasing the outputs during installation.*

cost-effective units ($155) offer track densities as high as 1200 counts/revolution and TTL- and CMOS-compatible outputs.

They boast a patented pre-alignment scheme that eliminates the need for phasing the outputs during installation, and they employ an LED light source and a monolithic radial phototransistor array. Because all sensors are on the same silicon chip, they exhibit high uniformity that minimizes sensitivity to temperature and aging effects.

Output format is quadrature (A, B) plus index pulse. The quadrature-output channels have a 100-kHz frequency response; the index output has a 50-kHz frequency response. Moment of inertia equals 6.2×10^{-5} oz-in.-sec^2, slew speed measures 10,000 rpm, and phasing is 90±30° max. The encoders operate from 5, 12, or 15V supplies over 0 to 70°C and draw 100 mA max.



To provide a cost-effective position-sensing solution, *TRW offers a fully assembled motor/encoder combination that saves labor and inventory costs. Relying on user-supplied specs, product engineers at distribution motor-modification centers select the correct motor/encoder combination for specific applications.*

Making things easy

TRW has recently introduced a fully assembled motor/encoder combination that saves labor and inventory costs. A low-cogging unit well-suited to servo applications, it consists of an IM-15 motor and the appropriate encoder to your specific application. Product engineers at TRW distribution motor-modification centers evaluate your requirements and choose a suitable encoder.

Either a 1- or 2-channel square-wave output is available, and resolutions range from 90 to 512 pulses/revolution. Encoder inertia is 2.6×10^{-5} oz-in.-sec^2. The motor/encoder combination operates from 6, 12, or 24V supplies. It has a lifetime of 2500 hours (nominal) continuous duty when operating from 12 or 24V supplies. **EDN**

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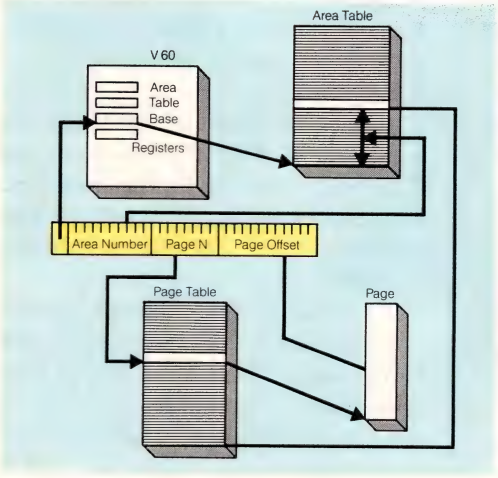
Leading

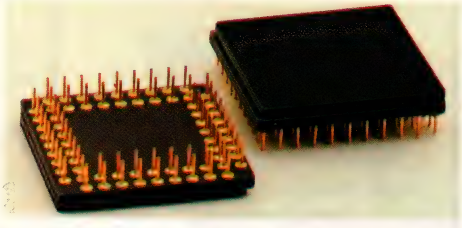
The new

V60/V70 – Revolutionary advances in CMOS technology for the ultimate 32-bit microprocessor performance. NEC's new supermicro family is based on a general purpose architecture with a whole arsenal of on-chip features to handle the most sophisticated and complex applications in industrial control, office automation and telecommunications.

NEC's proprietary CMOS VLSI technology, which packs more than 375.000 transistors on a single chip and achieves extremely low power consumption, is the key to performance. The V60 has an external 16-bit bus while the V70 is a full 32-bit machine. With a six-stage pipeline structure, both are designed for high throughput, performing at 3.5 and 5.3 MIPS (MAX) respectively. On-chip floating point functions provide the extra zip demanded by compute-intensive applications.



The on-chip memory management unit of the V60/V70 maintains a mammoth 4 Gigabyte virtual address space and a four-level protection mechanism for efficient implementation in multi-user environments. The processors can operate in native mode or 16-bit V20/V30 emulation mode, demonstrating yet again the fundamental compatibility strategy of the entire V-Series.



the field

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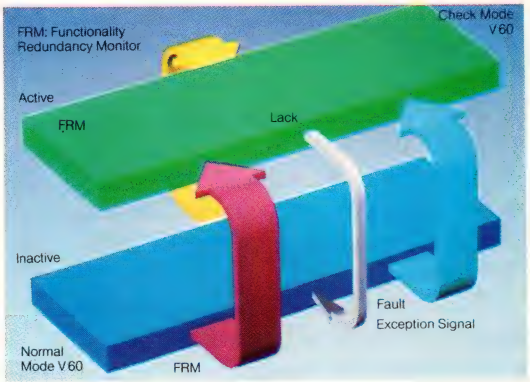
V60/V70
32-BIT SUPER MICROPROCESSORS

A powerful chip feature of the V60/V70 is the unique functional redundancy monitor. This feature allows the design of highly reliable, fault tolerant systems by putting together two or more processors to operate in parallel. Validity of outputs of these is automatically checked every machine cycle for early detection and possible correction of the System operations.



Hardware expandability for the V60/V70 is assured by the full line of compatible CMOS peripheral devices. Software power comes from the V60/V70 instruction set, ideally suited for high-level language support and compiler optimization. An on-chip debug facility cuts down development time by efficient on-line error detection. Standard V60/V70 operating software includes *UNIX V and NEC's own Real-Time Operating System.

NEC ORIGINAL MICROPROCESSORS
V/series

The V-Series. Powerful and flexible products from a world leader in microelectronics. Backed up by a world-wide manufacturing, sales and service organization.

* UNIX V is a registered trade mark of AT+T.

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Italy: Milano 02/67 09 108, Telex 315 355
Sweden: Täby 08/73 28 200, Telex 13 839
UK: Milton Keynes 09 08/69 11 33, Telex 777 565

CIRCLE NO 58

NEC

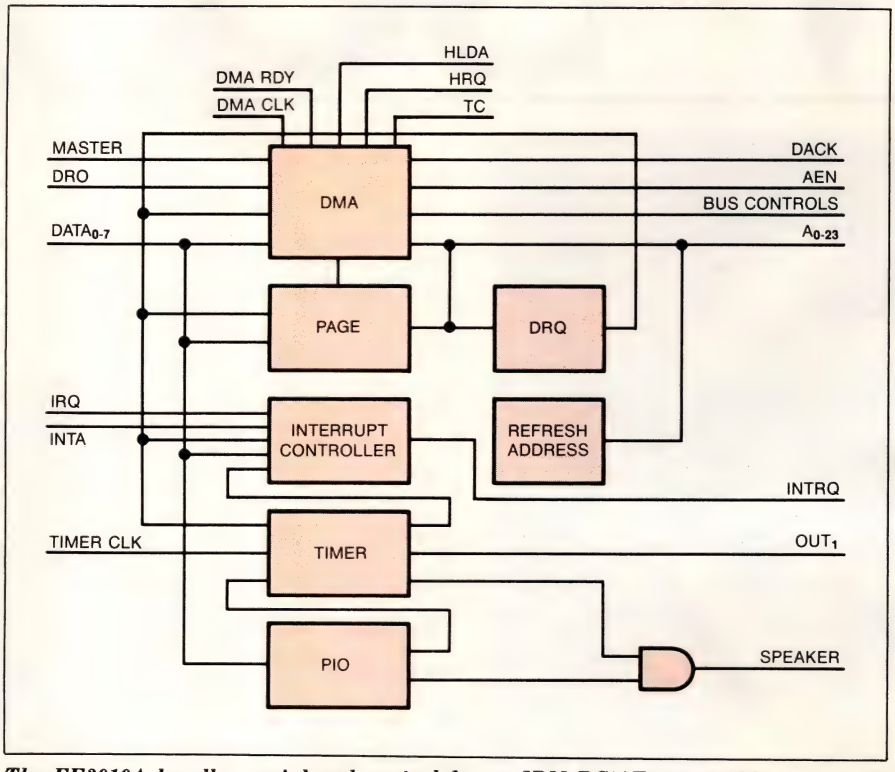
Chip supports peripheral-control functions for industrial single-board PC/ATs

The FE3010A peripheral-controller chip, when coupled with the FE3000 CPU-controller IC, implements an IBM PC/AT in only 4.5×7 in. of board space. (Memory chips require additional space.) The FE3010A supports many of the same functions supported by the 82C206 peripheral controller from Chips and Technologies Inc (Milpitas, CA), but to implement a PC/AT with the 82C206, you would need CTI's CS8220 5-chip set. As does CTI's peripheral controller, the FE3010A combines DMA-controller, interrupt-controller, and timer/counter capabilities on one chip. In addition, each of the chips serves as the memory and I/O interface for the corresponding PC/AT chip set.

The FE3010A peripheral controller and FE3000 CPU controller supply most of the functions of an industrial single-board IBM PC/AT mother board. You need to add circuitry for address, data, and memory-bus buffers; a memory-address multiplexer; a keyboard controller; and memory.

The FE3010A and FE3000 don't implement some seldom-used features of the PC/AT, however. The IBM PC/AT's interrupt controller, for example, can operate in single mode or cascade mode, but is hardly ever used in single mode. The FE3010A's interrupt controller is hard-wired in cascade mode. In contrast, the CTI chip set supports both modes, but the company recommends against using the single mode in order to maintain PC/AT compatibility.

In its most serious departure from the IBM configuration, the FE3010A lacks a real-time clock/calendar (which the 82C206 includes on chip). Further, the FE3010A and FE3000 do not include on-chip bus buffers (although the CTI chip set does). The FE3010A latches address lines $A_{8\text{-}15}$ (the CTI chip requires an external latch). The FE3000 is capable of supporting 1M-bit RAMs, and it can run at 6, 8, or 10 MHz. You can program it for zero, one, or two wait states. (The CTI chip set can be programmed for zero, one, two, three, or four wait states.)



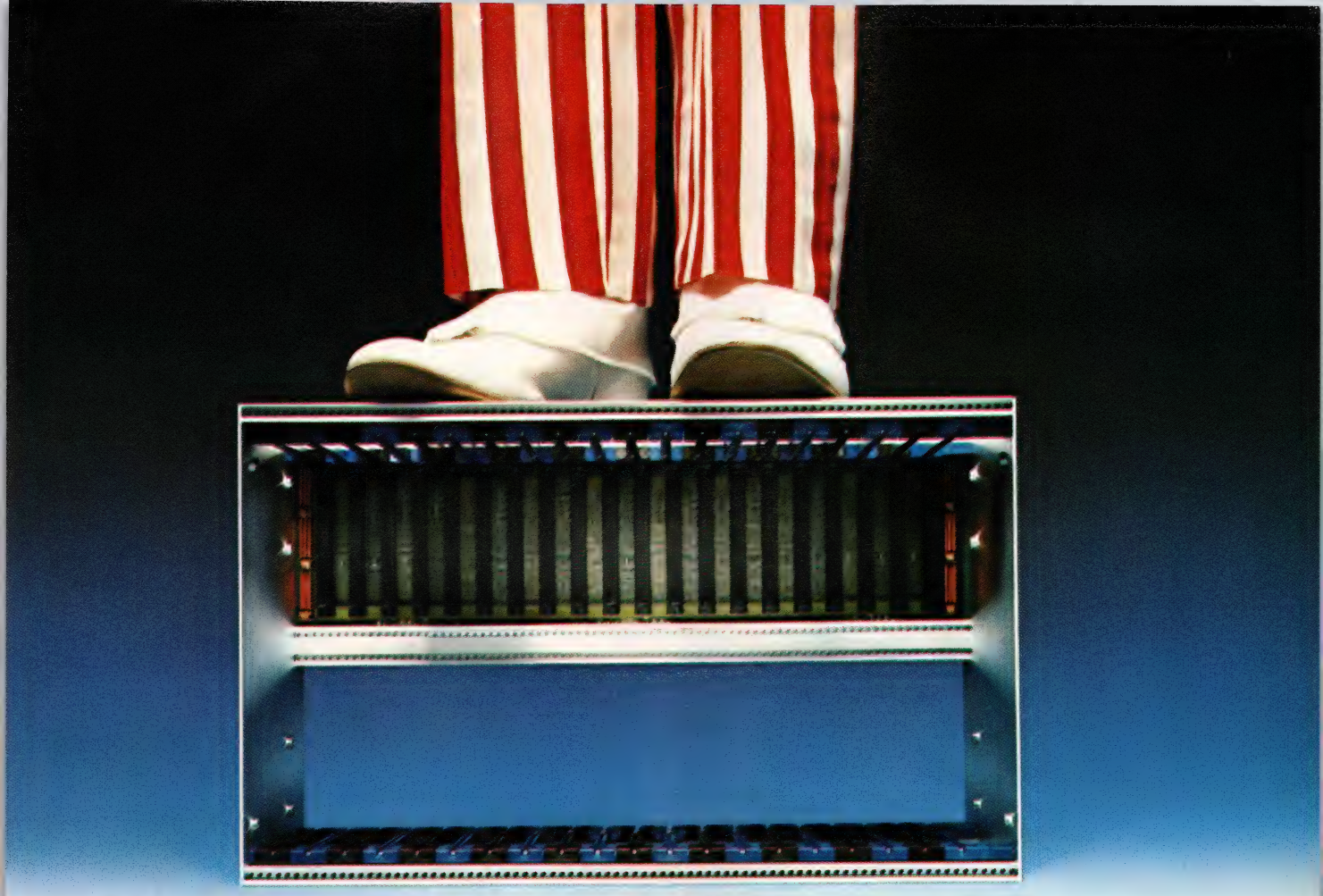
The FE3010A handles peripheral control for an IBM PC/AT-compatible system. *To implement a PC/AT design, you need to add an FE3000 CPU controller, RAM, bus buffering, and a real-time clock.*

The FE3010A is tailored for application in a single-board industrial PC/AT. (The CTI chips, on the other hand, incorporate the capabilities of the PC/AT's general-purpose components. The CTI chips are also capable of executing the same basic BIOS that the IBM PC/AT executes.) Instead of being able to use IBM's BIOS, the FE3000 and 3010A use only their manufacturer's BIOS, a limitation that can be an advantage in some applications. For example, the IBM BIOS checks for the presence of a keyboard and a monitor, and if your design lacks one of these components, your computer could hang up after you turn it on. The BIOS used by the FE3000 and 3010A does not include the keyboard and monitor check. FE3010A, $55 (delivery, 12 weeks ARO); FE3000, $22 (100).

—Margery S Conner

Faraday Electronics Inc, 749 N Mary Ave, Sunnyvale, CA 94086. Phone (408) 749-1900.

Circle No 726

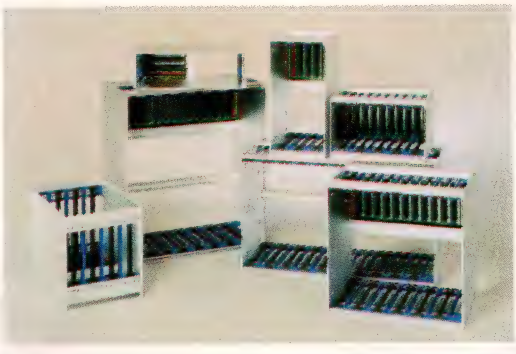


The Americanized VME Card Cage. We Stand On Our Reputation.

One reason Electronic Solutions became the world's leading supplier of Multibus card cages is that five generations of improvement gave our cages a reputation for indestructibility second only to a rock.

So when we decided to build an Americanized version of the VME card cage it was only natural that we would want to build it the same way. Because European kit-style cages don't measure up when it comes to strength.

Introducing Electronic Solutions V-800 Series VME Card Cages. We took a stand for ruggedness and rigidity. Right on top of them — to prove that a V-800 card cage could maintain its precise card alignment through thick and thin.



Rigidity gives your VME cards less room to flex and that means less room for things to go wrong. Connectors stay connected. And so do printed circuits. So when your system is shipped, moved, or dropped from a forklift the odds are a lot better that it will remain functionally intact.

But that's not the only part of our reputation we built into our VME card cages.

Our V-800 Series cages feature advanced, low-noise, high-performance backplanes designed for the fastest VMEbus signals. You can mount our new cages on any axis. And you can use our exclusive center adapter to convert any double slot to two singles or any triple size slot to a double and a single.

Electronic Solutions V-800 Series VME card cages. Step up to the best there is.

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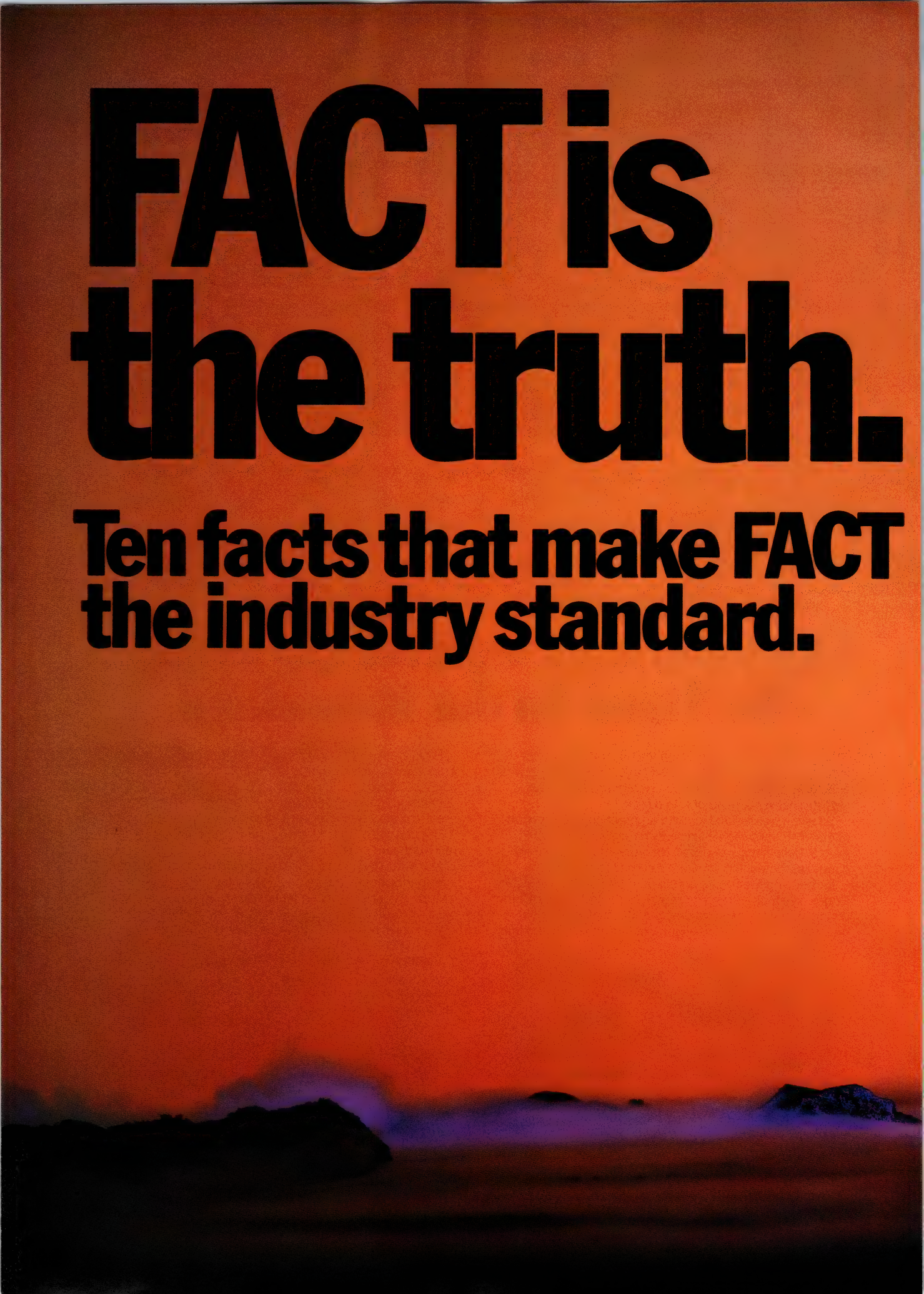
CIRCLE NO 112

FACT is the truth.

Ten facts that make FACT the industry standard.



Industry standard status doesn't happen overnight. A product or family has to prove itself under fire. It has to successfully compete in the marketplace and establish its superiority over every competitive alternative. It has to be the best. Hands down.

FACT (Fairchild Advanced CMOS Technology) is the best advanced CMOS family available today. It has become the standard of the industry.

Here's why:

1. FACT products have two major second sources. Six other manufacturers are committed to marketing devices that are functionally equivalent and pin-compatible with FACT parts.

2. FACT is pin-out compatible with existing TTL and HC logic devices.

3. FACT already has 46 parts on distributors shelves in a variety of packages, including surface mount. We are firmly committed to offering a total of 120 FACT parts in 1987.

4. FACT has wide industry acceptance and numerous design wins. Over 1000 customers have created high-performance products with FACT components.

5. FACT conforms to JEDEC standards for advanced CMOS logic.

6. FACT is military qualified. Our devices are available with full compliance to MIL-STD-883C.

7. FACT is backed by Fairchild's unparalleled experience in digital logic. FAST is the undisputed industry standard TTL logic family. Fairchild was the first to introduce high-performance CMOS logic successfully.

8. FACT is backed by Fairchild's extensive applications support including nationwide FAIRTECH™ Design Centers and a corps of field applications engineers.

9. FACT is growing into a total systems solution. LSI and VSLI parts will be introduced soon.

10. FACT combines all the best performance features of existing industry standard logic families into the ultimate logic solution.

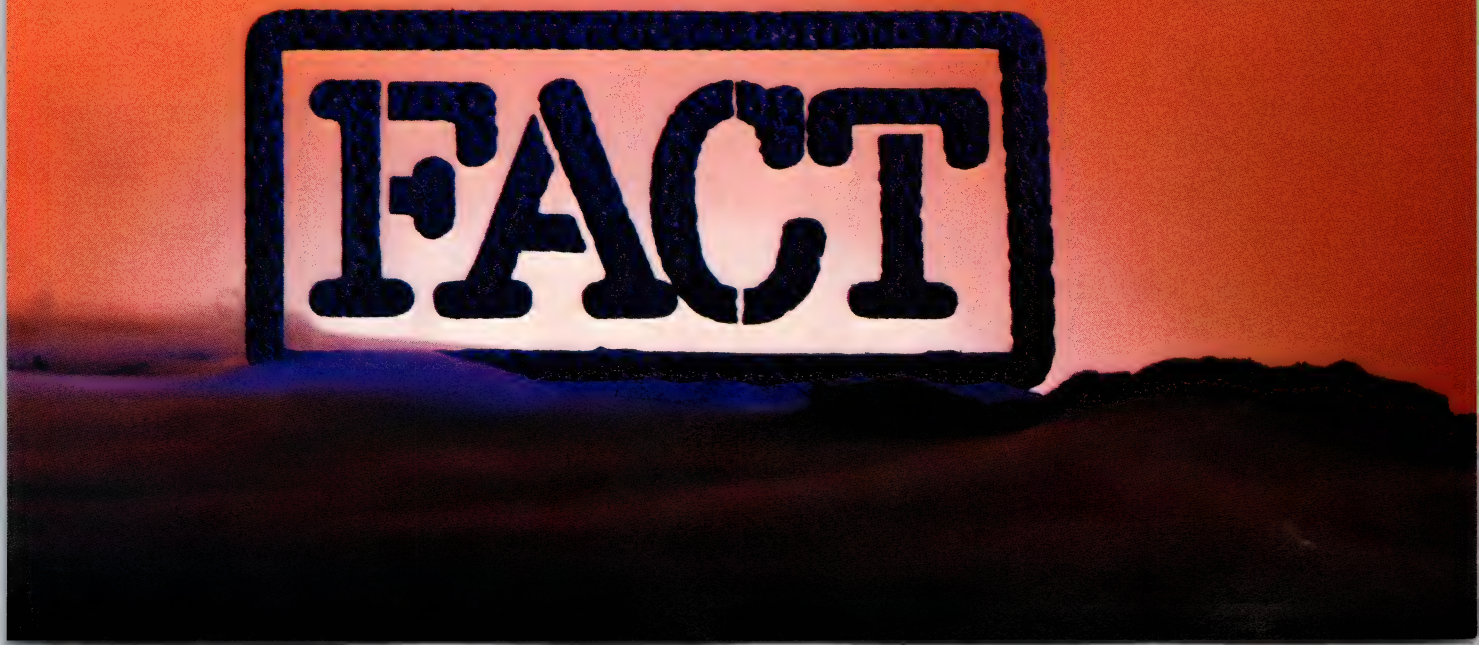
We're taking the high ground.

FACT is the truth. For free technical data and availability information or the number of your nearest sales office, contact the Fairchild Customer Information Center, **1-800-554-4443.**

FAIRCHILD

A Schlumberger Company

CIRCLE NO 113

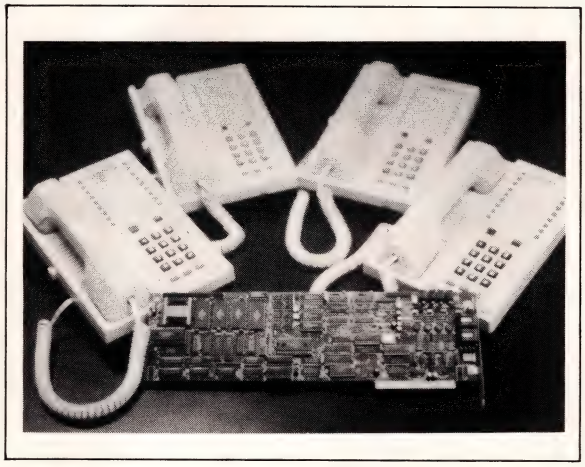


READERS' CHOICE

Of all the new products covered in EDN's **September 18, 1986**, issue, the ones reprinted here generated the most reader requests for additional information. In case you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, or refer to the indicated pages in our **September 18, 1986**, issue.

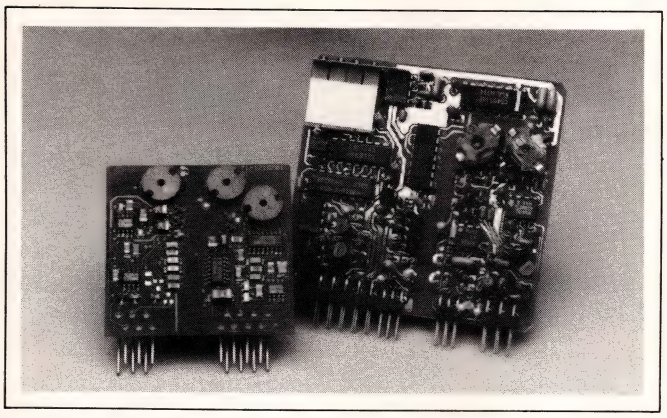
EXPANSION CHASSIS

The MacBus stand-alone expansion chassis plugs into the Apple's SCSI port and turns a Macintosh Plus computer into a μP-based data-acquisition and instrumentation-control system (pg 136).
National Instruments Corp.
Circle No 601



◀VOICE SYSTEM

The Dialog/40 board, a multiple-telephone-line voice I/O controller, can record, play back, autoanswer, and detect DTMF signals concurrently over four independent telephone lines (pg 352).
Dialogic Corp.
Circle No 603



MATH PROGRAM

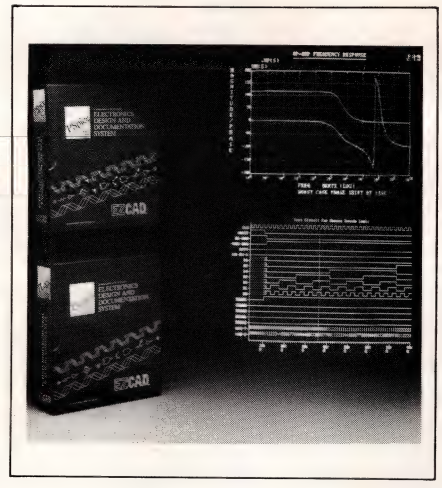
SciMath is a command-driven scientific mathematics program that allows you to perform numerical calculations without any programming (pg 370).
Spindrift Software Inc.
Circle No 605

▲ MODULES

The 5B Series signal-conditioning modules use surface-mount and small-outline devices to achieve a 3:1 reduction in volume as compared with the modules' older siblings (pg 140).
Analog Devices Inc.
Circle No 602

PERSONAL CAE ▼

This simulation package integrates the PLogic logic simulator and MicroSim's PSpice circuit simulator. It includes the graphics postprocessors LogicView and SpiceView, which create color and monochrome displays (pg 330).
E/Z CAD Inc.
Circle No 604



PHASE-LOCKED LOOP

The PC74HC4046A (CMOS-compatible) and PC74HCT4046A (TTL-compatible) PLL ICs are high-performance versions of the industry-standard, 16-pin 74HC406 and 74HCT4046 devices (pg 366).
Philips.
Circle No 606
Signetics Corp.
Circle No 607

MICROTEK DOES IT AGAIN

...AT THE LEADING EDGE

SUPER 8, 68020,

NOW 80386!

The Intel 32-bit 80386 microprocessor has arrived, and is set to play an important role in high-end, high-performance products. Due to wider buses and higher clock speeds, complex 80386 target systems now require more powerful developing and debugging tools. Selection of a good development system and emulator will be critical in determining whether or not 80386-based products are completed on schedule and within budget.

MICROTEK'S U.S. service, sales and marketing arm, NEW MICRO, now has the MICE-32/80386, a portable emulator that can run with any IBM-PC/XT/AT personal computer or compatible, VAX, and MicroVAX through parallel or serial interface. Or can stand alone with a terminal.

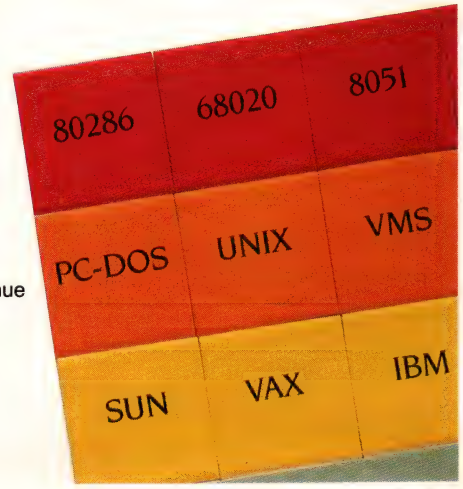
Look at these features:

- *Completely self-contained standalone emulator*
- *User-friendly command structure*
- *Emulation to 32 MHz*
- *"Snapshot" conditional, time-stamped trace*
- *256K Bytes soft mapped emulation memory*
- *Powerful symbolic debugger with user definable procedures under PC/MSDOS, VMS and ULTRIX.*

Other processors supported by Microtek
80286, 80186, 80188, 8086, 8088, 68000, 68010, 68008, Z80, NSC800, 8085, 6809, 6809E, 6502 (40 and 28 PIN) 8032, 8051, 8031, 8344, 8048, 8049, 8050, Z8, SUPER 8

NMI

New Micro, Inc.
16901 So. Western Avenue
Gardena, CA 90247
1-800-233-6048
In CA: (213) 538-5369



• IBM PC and PC-DOS are trademarks of IBM Corporation. VAX, MicroVAX, ULTRIX and VMS are trademarks of Digital Equipment Corporation. UNIX is a trademark of AT&T.

LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	0	27	46	27	0	0	8.5	9.3
Pot-Core	8	33	34	25	0	0	7.3	9.6
Laminate (power)	7	20	40	33	0	0	8.9	6.6
CONNECTORS								
Military panel	0	0	75	0	0	25	13.8	13.1
Flat/Cable	22	39	30	9	0	0	4.6	4.6
Multipin circular	0	31	54	15	0	0	7.4	10.4
PC	7	33	40	20	0	0	7.1	5.8
RF/Coaxial	18	35	35	12	0	0	5.4	5.9
Socket	30	25	30	15	0	0	5.3	5.3
Terminal blocks	15	35	30	20	0	0	6.3	4.4
Edge card	10	35	45	10	0	0	5.9	7.3
Subminiature	20	13	53	7	7	0	7.3	6.4
Rack & panel	9	9	55	18	9	0	9.8	7.3
Power	8	31	38	15	8	0	8.2	6.0
PRINTED CIRCUIT BOARDS								
Single-sided	0	48	52	0	0	0	5.1	4.8
Double-sided	0	50	50	0	0	0	5.0	5.8
Multilayer	0	14	62	24	0	0	9.0	8.8
Prototype	0	83	17	0	0	0	3.0	2.9
RESISTORS								
Carbon film	56	13	19	12	0	0	3.6	3.6
Carbon composition	46	17	25	12	0	0	4.3	4.6
Metal film	42	21	33	4	0	0	3.8	3.9
Metal oxide	27	27	37	9	0	0	4.9	4.5
Wirewound	18	41	29	12	0	0	5.1	6.3
Potentiometers	12	46	27	15	0	0	5.5	6.6
Networks	18	27	41	14	0	0	6.0	7.6
FUSES	48	35	17	0	0	0	2.1	3.7
SWITCHES								
Pushbutton	14	33	34	19	0	0	6.4	5.1
Rotary	5	30	35	30	0	0	8.2	6.9
Rocker	20	30	35	15	0	0	5.8	5.9
Thumbwheel	0	42	42	16	0	0	6.8	8.3
Snap action	17	33	42	8	0	0	5.3	4.9
Momentary	7	36	43	14	0	0	6.4	4.6
Dual in-line	15	31	38	16	0	0	6.2	3.7
WIRE AND CABLE								
Coaxial	35	41	18	6	0	0	3.2	2.8
Flat ribbon	27	41	23	5	4	0	4.5	3.8
Multiconductor	35	24	29	6	6	0	5.3	3.8
Hookup	41	41	11	4	3	0	3.7	1.9
Wire wrap	43	29	21	7	0	0	3.4	3.1
Power cords	21	34	34	7	4	0	5.4	3.8
Other	22	34	22	22	0	0	6.0	7.4
POWER SUPPLIES								
Switching	6	18	41	35	0	0	9.3	9.4
Linear	14	21	43	22	0	0	7.3	8.0
CIRCUIT BREAKERS	19	38	12	31	0	0	6.8	6.8
HEAT SINKS	29	33	29	9	0	0	4.5	5.1

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
RELAYS								
General purpose	30	15	35	20	0	0	6.3	6.2
PC board	7	27	33	33	0	0	8.5	6.8
Dry reed	10	20	30	40	0	0	9.2	8.2
Mercury	10	20	40	30	0	0	8.4	10.1
Solid state	6	19	38	31	6	0	10.0	8.9
DISCRETE SEMICONDUCTORS								
Diode	34	32	20	11	3	0	4.8	4.5
Zener	23	37	20	17	3	0	5.9	5.5
Thyristor	18	18	41	17	6	0	8.0	7.1
Small signal transistor	24	19	38	14	5	0	7.0	6.7
FET, MOS	13	13	47	20	7	0	8.9	8.6
Power, bipolar	21	16	42	16	5	0	7.6	7.3
INTEGRATED CIRCUITS, DIGITAL								
CMOS	21	21	31	24	0	3	7.8	7.6
TTL	29	25	25	17	0	4	6.5	7.5
LS	29	21	29	17	0	4	6.7	7.7
INTEGRATED CIRCUITS, LINEAR								
Communication/circuit	8	15	46	31	0	0	8.9	7.7
OP amplifier	21	29	21	29	0	0	6.9	9.2
Voltage regulator	28	32	20	20	0	0	5.4	8.2
MEMORY CIRCUITS								
RAM 16K	25	31	19	25	0	0	6.1	7.1
RAM 64K	29	29	24	18	0	0	5.3	6.2
RAM 256K	25	25	31	19	0	0	6.0	7.5
ROM/PROM	20	13	40	27	0	0	7.7	8.3
EPROM	23	32	32	13	0	0	5.4	7.4
EEPROM	20	27	33	20	0	0	6.4	10.8
DISPLAYS								
Panel meters	16	15	46	23	0	0	7.7	8.3
Fluorescent	0	11	56	33	0	0	10.0	10.4
Incandescent	0	13	50	37	0	0	10.3	10.0
LED	18	30	41	11	0	0	5.6	5.6
Liquid crystal	8	23	38	31	0	0	8.5	8.3
MICROPROCESSOR ICs								
8-bit	9	48	14	19	10	0	7.6	6.9
16-bit	0	41	29	18	12	0	9.1	7.0
FUNCTION PACKAGES								
Amplifier	0	25	38	37	0	0	9.5	7.3
Converter, analog to digital	0	25	50	25	0	0	8.5	8.3
Converter, digital to analog	0	25	42	33	0	0	9.2	10.1
LINE FILTERS	0	53	12	29	0	6	8.5	7.2
CAPACITORS								
Ceramic	26	19	37	18	0	0	6.3	5.5
Ceramic monolithic	25	29	25	21	0	0	5.9	5.8
Ceramic disc	29	8	46	17	0	0	6.5	5.5
Film	17	22	44	17	0	0	6.7	4.6
Electrolytic	24	32	28	12	4	0	5.8	6.7
Tantalum	10	30	41	15	4	0	7.2	6.1
INDUCTORS	10	40	25	25	0	0	6.8	8.1

Source: *Electronics Purchasing* magazine's survey of buyers

Two of a kind!

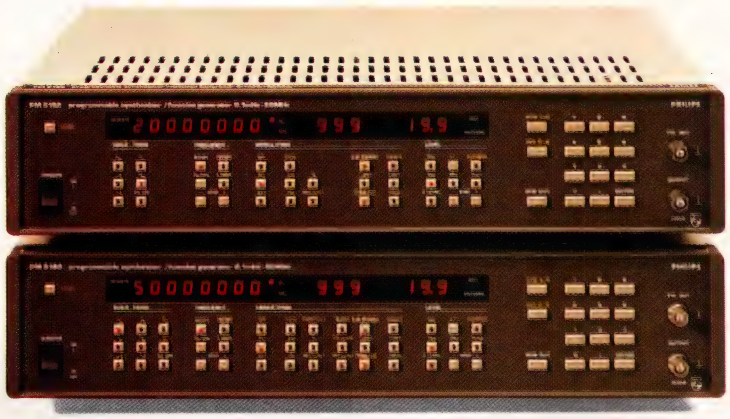
Our PM5192 and PM5193 Synthesizer/Function Generators are two of a kind. Both feature **8-digit frequency resolution;** so setting accuracy and reproducibility are guaranteed. Both are **IEEE-bus compatible;** so they can be integrated into automated system set-ups. Both are housed in identical **19" cabinets;** so they can be placed on a bench or mounted in a rack. And both offer the best **value-for-money** of any function generator on the market; so you get high performance without having to pay a high price!

■ The PM5192 is a **0.1mHz to 20MHz** instrument featuring: **5 selectable waveforms** with adjustable output to 20Vpp, and **AM/FM/Gating/Lin-Log sweep** modulation modes with internal **1KHz modulation frequency.** All function buttons have built-in **LED status signalling.**

■ The PM5193 **0.1mHz to 50MHz** generator offers the same fine features as the PM5192 plus an **extra 3 selectable waveforms** (including 3ns-Pulse and Haversine); **programmable modulation frequency** from 10Hz to 200KHz, and **counted burst.**

Test the difference

■ **Product credibility** in technology, technique, quality and service also is assured because the PM5192 and PM5193 Synthesizer/Function Generators are backed by the corporate resources of one of the world's largest electronics companies.



Test the difference and you'll also agree that Philips wins on price and performance!

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PHILIPS
Test & Measurement

PHILIPS

32-BIT RAPID DEPLOYMENT FORCE.

Intel's new military MG80386 microprocessor is now ready for immediate deployment.

We mean right away. Right off-the-shelf. Which means you can quickly get your design into production with all the benefits of Intel's world-class manufacturing capability.

Including our 1.5 micron CHMOS III process. The technology that provides both low power consumption and high total dose radiation tolerance (in excess of 100K RADS Si). Allowing you to build high performance, high radiation-tolerant systems that save space, weight and power.

Best of all, you get steady continuity of supply. Because CHMOS III is a proven technology that's delivered hundreds of thousands of successful products for years.

But continuity of supply is only half the story.

Consider that the MG80386 is the only 32-bit chip to provide complete hardware support for multitasking on-chip. Included in the CPU is a Memory Management Unit that provides support for virtual memory operations, optional on-chip paging and four levels of software protection.

Which makes it ideal for military applications that require a high degree of security and lightning-fast speed.

Military designers will also appreciate all the development support available for the MG80386. Like Fortran, C and Intel's own ADA™ language compiler. Which provides the most useful and most used language on easy-to-use development systems.

VHSIC	*MG80386*
• *Functional Throughput Rate*	*$3.0 \times 10^{12} \frac{Gates \cdot Hz}{CM^2}$*
• *Radiation Tolerance (Total Dose)*	*$>10^5$ RADS (Si)*
• *Input Clock Frequency*	*32 MHz*
• *Chip Density*	*Approx. 90,000 Gates (275,000 transistors)*

The MG80386 gives you a blazing 3.5 to 4 MIPS with a functional throughput that exceeds VHSIC product performance requirements.

For more information on the MG80386, call Intel toll-free: (800) 548-4725. Or write Intel Corporation, Lit. Dept. W-324, 3065 Bowers Ave., Santa Clara, CA 95051.

And get our rapid deployment force fighting on your side.

intel®

EDN's 13th Annual μP/μC Chip Directory

In the directory this year are 10 new entries, and missing are seven that appeared in the 1985 directory. But the most significant news is the way that two of the older families—the 8086 and 68000—have become even more dominant.

Robert H Cushman, *Special Features Editor*

In this year's directory, you'll find a spate of new DSP chips, listed on pgs 109 through 206. The most significant news is the continuing dominance of two general-purpose μP families—the 8086 and 68000—that were first listed in our 1978 directory, coupled with the appearance of leading μP families in ASIC cell libraries.

The degree to which the 8086 and 68000 families dominate the 16-bit arena is quantified by Dataquest, the San Jose, CA, market-research firm. Dataquest figures for '85 (the latest year for which complete values are available) show the 16-bit members of the 8086 family (including the 80186 and 80286) as having 60% of the unit volume. If the volume of NEC's V30, which is an admitted copy of the 8086, is added, the total 8086 dominance amounts to 65%.

The 16-bit members of the 68000 family (68000 and 68010) had 25% of the unit volume in 1985, leaving only 10% for all the other 16-bit μPs, including Zilog's Z8000 (4.45%), National's 32016 (3.82%), and stragglers such as GI's 1600, TI's 9900, and National's PACE.

The appearance of μP cores in ASIC libraries should increase the dominance of processors like the 8086. Intel argues that it will be some time before less-popular μPs are supported. The 8048 and 8051 from Intel and the 6805 from Motorola were among the first families to become cores in ASIC cell libraries, and Intel is now talking of 16-bit 8086 and 80186—and even 32-bit 80386—cores.

Where does the 8086 and 68000 families' dominance in the 16/32-bit general-purpose μP field leave the rest of the contenders? When we asked them, each responded, after agreeing that the 8086 and 68000 families did indeed at present dominate, with an explanation of why there was still room for them.

The most common argument continues to be that the general-purpose 32-bit world will not be dominated by any one μP and its instruction set because the level of standardization in the 32-bit world will be at the operating-system level.

In the general-purpose 32-bit world, that operating system is now and will be for the foreseeable future AT&T's Unix. As can be seen from the software-support sections at the bottom of the 32-bit entries in this directory, all—even Intel with its 80386—stress Unix support. For example, National Semiconductor says its 32000 family will provide the lowest cost 32-bit system to run Unix. AT&T says that, because it's the creator of Unix, its WE32 family will have the new versions of Unix first. Fairchild says that its Clipper will run Unix fastest of all.

Two additional reasons are offered why μPs other than the 80386 and 68020/30 will have a chance at being used in the 32-bit world. First is the established need for high-performance but reasonable-cost algorithm crunchers or accelerators. Second is that there will be just as much need for 32-bit controllers as there has been for 1-bit, 4-bit, 8-bit, and 16-bit controllers.

With respect to the algorithm crunchers, you'll find two different examples in our directory: the Inmos Transputer (T414, T212) and the 32-bit DSP chips. Inmos says that because its Transputers are the first

commercially available μPs designed to be paralleled, they will give OEMs the chance to implement certain algorithms faster than any ordinary μP is capable of. Many industry experts agree that highly parallel μP systems will be the wave of the future but wonder if the Transputer might be somewhat ahead of its time.

The 32-bit DSP chips are so much better at number crunching that involves multiplication that they need not fear that the 80386 or 68020/30 could shut them out of 32-bit applications, at least for the present. Those applications would typically be where sum-of-products numerical algorithms are used to process differential equations, as when audio-bandwidth analog signals are filtered in real time.

Examples of 32-bit DSP chips are the NEC 77230 and the AT&T DSP32, both of which are new to our directory this year and both of which are floating-point devices. But even these impressive DSP chips might feel threatened by the almost totally hardware approach of the A-100 chip from Inmos, which is also new to our directory this year. The chip's somewhat-brute-force approach can actually handle video analog bandwidth digitally in real time.

The suppliers of the specialized algorithm crunchers believe that, rather than competing with the 80386 and 68020/30, they will ride on the success of these leaders. An example of what they mean can be found in the mention of one of the Weitek math accelerators in the

(Text continued on pg 106)

By starting with standard μPs in core form, *you can paint your own custom system on a chip. As the entries in this year's directory demonstrate, more and more μP suppliers are making their μPs and associated support chips available as standard cells in ASIC libraries. (Photo courtesy Intel)*

Manufacturers of μP/μC chips

For more information on μP/μC chips such as those included in this directory, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card. The abbreviations in parentheses after some companies are those used in the directory.

Advanced Micro Devices
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Sunnyvale, CA 94086
(408) 732-2400
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Circle No 639

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(201) 770-3204
Circle No 640

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San Jose, CA 95134
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Circle No 641

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(415) 962-5011
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Circle No 653

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NCR Microelectronics Div (32-bit)
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Circle No 695

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Circle No 696

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Circle No 697

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Mesa, AZ 85203
(602) 962-4545
Circle No 698

Zilog Inc
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Campbell, CA 95008
(408) 370-8000
Circle No 699

ZyMOS Corp
Box 62379
Sunnyvale, CA 94088
(408) 730-8800
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entry for the 80386. This is the 1167 developed by Weitek to mate directly with the 80386 as a coprocessor. Here Intel symbiotically uses a potential competitor to help the 80386 outperform its 68020/30 rival.

Thirty-two-bit controllers could circumvent the dominance of the 8086 and 68020/30 because controllers don't have to be slaves to large software bases. An example of this freedom can be found in National Semiconductor's 8-bit COP 800 controller, which is new to our directory this year. National Semiconductor, which should know the controller applications because its COP 400 is second highest in unit volume among all μCs and μPs (of any type), said it felt under no compunction to make the COP 800 software compatible with any μP or μC—not even its own COP 400. Other 32-bit controllers include VLSI's 86C010 RISC-type μP and TI's 34010 graphics processor, both new to our directory this year.

This year we've dropped several μPs because Dataquest volumes and other indicators showed they had either gone past their prime or never reached it. We dropped TI's 99000; its demise has been in progress for several years (although at its peak the family did not do so badly; according to Dataquest, 1.6 million units were shipped in '83 for a 23% share of the 16-bit μP market, second only to GI's CP-1600).

We've also dropped the 3870. The first 8-bit 1-chip μP, it was in its day very successful. Dataquest figures showed that in '81 nearly 7 million units were shipped and the 3870 had a 19% share of the 8-bit 1-chip market. But in '85 it had dropped to 4 million units and less than a 3% market share. Because of the momentum from its past popularity, the 3870 will probably continue to be available for a number of years, but most sources are no longer recommending it for new designs. Another negative sign for the 3870 is that plans for CMOS versions have apparently been abandoned.

The National Semiconductor NSC800 never really made the grade. It sounded like a good idea—a CMOS version of the Z80 that would be bus compatible with 8080/85 peripherals. However, Dataquest figures showed that, although it got to 1 million units/year in '84, it dropped back down to 0.845 million units last year. Furthermore, it never received strong second-source backing.

We've dropped the DEC Micro T-11 and J-11 (μP versions of DEC's PDP-11, 16-bit minicomputer) because it turns out that they were never really seriously intended for OEMs. DEC actually discouraged sales by forcing customers to sign "restricted fields of use"

INDEX TO μP AND μC CHIPS IN EDN'S THIRTEENTH ANNUAL DIRECTORY

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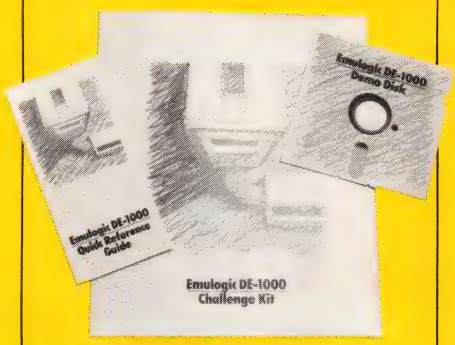

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agreements. DEC never has released its MicroVAX 32-bit μP to the OEM market, a further indication of its policy towards the OEM. From DEC's current, impressive sales success (against IBM) and even more impressive profitability in the otherwise depressed minicomputer market, however, it appears that DEC made the right choice.

Intermetall and STC Semiconductors requested, respectively, that we drop the UDPI-01 and DSP-128. Both of these DSP chips had their good points—the UDPI-01 promised a selling price of under $10, and the DSP-128 had an excellent state-of-the-art architecture. Nonetheless, the suppliers apparently realized that their early designs wouldn't be easy matches for the horde of new third-generation DSP chips suddenly hitting the market from major US and Japanese companies.

Finally, we dropped AMD's 29500, but not because it isn't still alive. Indeed, it's not only alive, but AMD has dropped prices and is at work on CMOS counterparts. The problem with including this family in our directory (a similar problem pertains to Analog Devices' Wordslice, which we decided to leave in another year) is that the 29500 devices are really extensions of the 2900 building-block family. Designers are as apt as not to use the parts on a mix-and-match basis with other 2900-type parts from other suppliers. What's really needed is a master cataloging of all the 2900 derivatives, something we'll leave for another year. **EDN**

Acknowledgment

EDN would like to thank Mel Thomsen, Janet Rey, and Patricia Galligan of Dataquest Inc (San Jose, CA) for their help with statistics on μP and μC use.

References

1. Cushman, Robert H, "EDN's Twelfth Annual μP/μC Chip Directory," *EDN*, November 28, 1985, pg 106.
2. Bader, Maryann, "Impact of Single-Chip Digital Signal Processors," technology report ($895) from Electronic Trend Publications, 12930 Saratoga Ave, Saratoga, CA 95070. Fairly detailed overview of 1-chip and bit-slice DSP chips based on information assembled from various sources (including EDN).

Article Interest Quotient (Circle One)
High 470 Medium 471 Low 472

μPD75XX, 75X

4-BIT CMOS

AVAILABILITY: Now for all 75XX models and all 75X models except 75308 (LCD), which is fourth quarter '86
COST: $1 to $6 for 75XX in 10k qty; less than $4 for masked-ROM 75X; $50 for EPROM 75P108
SECOND SOURCE: Gould AMI and Matra Harris (France) for 75XX; none yet for 75X

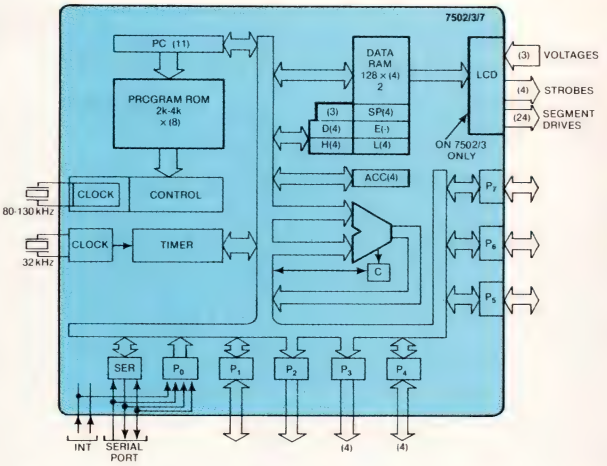
NEC Electronics Inc
(Corporate Headquarters)
401 Ellis St
Mountain View, CA 94039
Phone (415) 960-6000

NEC Electronics USA Inc
(Applications Help)
1 Natick Executive Park
Natick, MA 01760
Phone (617) 655-8833

Description: Sophisticated architecture for a 4-bit μC, especially now that family is in CMOS with added features. Older 75XX has HL and DE general-purpose pointer pairs like the popular 8-bit 8080. Even has stack pointer and instructions to manipulate it. In some applications, most attractive feature is the self-refreshing LCD-driver option. Latest 75X group is upward growth of 75XX. Has multiple register banks for faster interrupt processing, plus the 1-μsec instruction cycle is 2× speed. Bit manipulation added to instruction set.

Status: This family has been world leader in sheer volume of units, according to Dataquest figures up to '85. Only the National COP comes close. The 75XX has had 23½% of the 4-bit-μC market with shipments of 31½ million units. While probably the majority of this volume is in Japan and Asia, the parts are well supported in the US. All 4-bit chips are now receiving increased competition from low-end 8-bit μCs, and the supplier's answer is to add new parts, such as the 75X members, with increased speed and on-chip capabilities. The goal continues to be providing designers everything they need in just one package, including the complex outputs needed to drive vacuum-fluorescent and LCD displays.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Diagram shows 7502/3/7/8 architecture. There are now three dozen parts in the 75XX-75X family. See table for range of features.
2. 7502 and 7503 have self-refreshing LCD drivers on chip. Can drive as many as 12 positions of 7-segment LCDs and also handle 14-segment alphanumeric and dot-matrix units. Programmer determines display by bit mapping in memory, with the self-refresh feature freeing CPU from constant attention.
3. Observe that 8-bit timer/counter has its own separate clock. Intention is that this can be served by lower cost watch-type 32-kHz crystal; main clock for CPU can then be just an RC network.
4. Thin 44-, 52-, 64-, and 80-pin flat packages with leads coming out on all four sides are supplied for some family members. They are useful in miniaturized consumer products, especially those that have LCD displays needing many connections. However, because it has been widely used in CMOS calculators selling for less than $10 (such as those from Sharp), users can assume that it is amenable to low-cost mass production.
5. Newest chips in 75XX group are 7554/56/64/66 low-end inexpensive devices (the 7554/64 comes in 20-pin SDIP). Also the new 7533, which is only chip in family to have on-chip A/D.
6. Current introductions to 75X group include parts with drivers for LCD displays: 75308 and 75P308. (Parts with vacuum-fluorescent drivers available now.)

RANGE OF AVAILABLE FEATURES AMONG 75XX AND 75X MODELS

GENERIC PART	RANGE AMONG MODELS	ROM BYTES (×8)	RAM NIBBLES (×4)	I/O, TOTAL PINS	INSTR CYCLE, μSEC	PACKAGE PINS
75XX	MIN	1k	64	15	2.44	20
	MAX	6k	256	53	7.6	80
75X	MIN	4k	320	53	0.95	64
	MAX	8k	512	58	15.3	64

I—DATA-MANIPULATION INSTRUCTIONS
Add (75X has subtract)
Logicals, including complement, rotates and shifts
Bit manipulation (set and reset and test memory bits)
Increment and decrement
II—DATA-MOVEMENT INSTRUCTIONS
Transfers between accumulator and H, L, D, and E registers
Load HL and DE pairs with immediate data, on both 4- and 8-bit bases
Increment or decrement registers H, L, D and E and skip if value in registers becomes zero (75X has B,C and X registers also)
Table look-up
Input and output instructions (75X has bit transfer between Carry bit and memory)
III—PROGRAM-MANIPULATION INSTR
Jump-type instructions
Decisions implemented by skip-type instructions
PUSH and POP instructions for stack, including PUSH and POP of HL and DE pairs
Depth of subroutine and interrupt-save levels limited only by amount of available data in RAM
Instructions for timer (75X can use table in memory for access to frequently used instructions and subroutines).
IV—PROGRAM-STATUS-MANIP INSTR
Set and reset carry flag. (On 75X there are additional flags in PSW, and bit-manipulation instructions can affect PSW bits)
Save and restore PSW upon subroutines and interrupt. (On 75X, skip status flags in PSW support only-execute-first-in-string instructions)

Specification summary: For 75XX: 4-bit family with split-memory architecture common to calculator-derived 4-bit controller μCs; program side has 2k to 6k bytes ROM, and data side has 64 to 256 nibbles RAM. Data side has HL and DE 4/8-bit register pairs for pointer addressing, as well as a 7-bit stack pointer. I/O functions include timer/event counter with its own clock, serial port and interrupts to service these asynchronous functions, as well as external interrupts. Instruction cycle is 2 to 8 μsec. Supply voltage is 3 to 7V. Power drain is just 300 μA at 5V and 150 μA at 3V. Packaged in 28- and 40-pin DIPs, but with special 44- and 80-pin flat packages for applications that need miniaturization and extra pins. For 75X: Enhancement of 75XX having 4k to 8k bytes ROM and 320 to 512 nibbles RAM. Registers in four banks, each with eight 4-bit registers, with rapid context switching between banks. Added instructions for 46 total. On-chip functions include timers, 8-bit serial interface, and seven interrupt sources divided into five priority levels. I/O includes 32 high-current LED drivers (200 mA), 12 n-channel open-drain outputs that will withstand 12V, and four programmable threshold detectors. Incorporates 4.19-MHz (max) oscillator producing 0.95-μsec instruction cycle. Stop and Halt modes to reduce power. Packaged in 64-pin shrink DIP or flat pack.

HARDWARE — SUPPORT — SOFTWARE

Development system designed by US application arm of NEC (Natick, MA). Based on Intel Multibus, consists of three cards for that bus. One will be an 8080-based single-board computer; the others, interfaces to two 8-in. floppy-disk drives and peripherals such as CRT terminals. 48k of RAM will be provided. This development system will interface with existing line of Evakit evaluation boards, which contain ROMless 75XX devices for prototyping: Evakit 7520 ($1950) for PMOS part and Evakit 7500 ($1800) for the 7502/3/7 devices. LCD attachment, the 7500-LCD ($450), is required for LCD prototyping.

Crossassemblers, etc, to run under CP/M operating system on the Multibus-board-based development system. Also available for Intel Intellec under ISIS II and for Motorola Exorciser under FDOS II and now also for IBM PC under either CP/M-86 or MS-DOS.

So, Is There a Real ASIC Second Source Setup in the Picture?

(Hint: Raytheon's RL7000 and LSI Logic's LL7000 are like . . .)

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CIRCLE NO 62

COP400

4-BIT NMOS AND CMOS

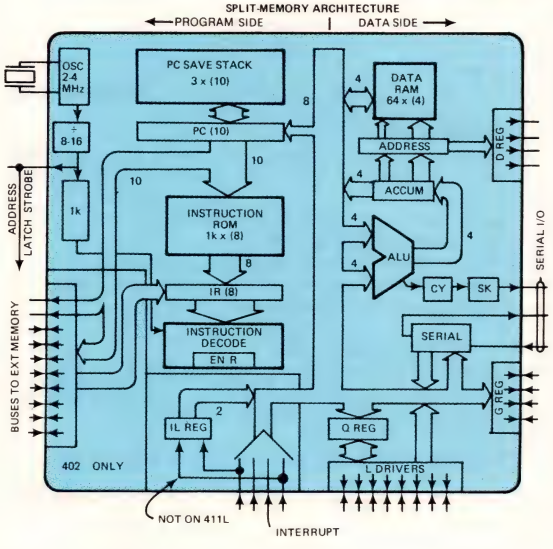
AVAILABILITY: Now
COST: Under $0.50 for 413L and under $1 for CMOS 413C in very high volume (1M/yr, which is common for successful 4-bit devices)
SECOND SOURCE: Thomson Semiconducteurs (over 5M units in 85)
CORE: Because this type of 4-bit one-chip device has, from the start, employed the μP core plus mixed-and-matched memory and I/O, the transition to ASIC semicustom is only a matter of making the design tools easy for customers to use.

Description: NMOS and CMOS minimum-cost single-chip family. COPs are complete microcontrollers intended to make lowest cost, intelligent products feasible. Contain the complete μC system—μP, memory, and I/O—necessary to implement dedicated control functions. Typical application would be as the lone chip in a low-cost toy for the mass consumer market. In such a product, the COP might receive inputs from a keyboard, do mainly BCD data manipulation (with some byte-wide ASCII manipulation also feasible), and drive a display (plus provide some direct control outputs). The OEM customer might order COPs at the rate of several millions annually, paying just $0.60 apiece.

National Semiconductor Corp
2900 Semiconductor Dr, MS 16-174
Santa Clara, CA 95051
Phone (408) 721-4345

Status: An example—not too common these days—where a US μP/μC has stood up to Asian competition in a very low-cost, very high-volume market. According to 1985 Dataquest 1985, National's COP has held second place in the mostly Asian-source-dominated 4-bit-μC market. The COP had 16% of the 4-bit market against first place 75XX from NEC, which had 17%. Total 1985 COP unit shipments were 29 million units, of which 24 million were from prime source National. Supplier is working on further cost reduction for high-volume users to maintain price advantage over 8-bit single chips like the 8048 and 6805, which usually cost twice the price of a COP. In addition, supplier is bringing out COP800 (see next directory entry) to compete in low-end 8-bit-μC market. The COP800 is similar to COP400 in name only, however; it has a different architecture and instruction set.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Binary arithmetic (add and subtract) with BCD handled by add immediate of correction. Only logical is exclusive-OR. Can test individual bits in RAM
II—DATA-MOVEMENT INSTRUCTIONS
Direct and indirect movements between data RAM and accumulator. Like some other 4-bit, 1-chip μCs, makes use of clever built-in exclusive-OR in instruction to flip back and forth between nibbles of data strings
Combination instructions permit indexing forward and backward through data RAM
Move 8-bit pattern from instruction ROM to Q output register, also 8-bit table look-up on input
Can set up operating modes on serial I/O with software, turning it into counter if desired
I/O instructions to individually serve unique I/O ports
III—PROGRAM-MANIPULATION INSTR
Jump and jump indirect
Jump and return from subroutine (three levels of return stack; two for 410L)
Skip-type conditional test instructions
Vectored hardware interrupt
IV—PROGRAM-STATUS-MANIP INSTR
Set and carry bit, and interrupt enable (There is a special means for saving carry status upon interrupts)
V—POWER-SAVING INSTRUCTIONS
Halt instruction disconnects internal circuitry from clock, which lowers power consumption to few μA. Because chip is static CMOS, all registers retain data, and upon Reset, will restart from where left off.

Notes:
1. ROMless 402 and 404 are available for development and low-volume production.
2. Power for CMOS will vary from 3 mA at 14-μsec cycle to 120 μA at 64-μsec cycle (using 32-kHz watch crystal) and 2.4V supply. "Asleep" drain will be 6 μA max.
3. All COP 400 models and peripherals are configured with National Microwire serial I/O for easy exchange of data with low pin count.
4. Introducing enhanced NMOS chips with LIP instruction for full utilization of L port, improved cycle time, optional power-on reset disable.
5. Also introducing enhanced CMOS chips with optional multi-input wake-up feature, improved timer, including interrupt-on-overflow; designed for increased ESD and latch-up margin.
6. 20-pin surface-mount packaging to be available in fourth quarter '86; 24- and 28-pin surface-mount packaging to be available in second quarter '87. These packages are suited for space-sensitive applications such as consumer goods.
7. In addition to the ROMless CPUs, piggyback CPUs are available; they carry standard EPROMs.

Specification summary: Single-chip μC with split-memory architecture; 8-bit-wide instruction side (1k for 420 part) and 4-bit-wide data side (64 for 420 part). Considerable on-chip I/O despite small package size (28 pins for 420) including clocked serial/event-counter port. Family includes 30 devices with different memory and I/O options and fabricated in several device technologies, including not only basic metal-gate NMOS but CMOS. Devices to operate mostly at 5V and require only minimal power-supply currents (25 mA for 420). Extended-temperature-range devices (−40 to +85°C) available, as well as extended-voltage-range ones.

COP PART	TECHNOLOGY	PKG (PINS)	MEMORY ROM (K×8)	MEMORY RAM (×4)	SPEED INST CYCLE (μSEC)	8-BIT BIDIR I/O	INTERRUPTS
410C	CMOS	24	0.5	32	4	YES	0
411L	NMOS	20	0.5	32	16	YES	0
413C	CMOS	20	0.5	32	4	YES	0
413L	NMOS	20	0.5	32	16	YES	0
420	NMOS	28	1	64	4	YES	1
420L	NMOS	28	1	64	16	YES	1
424C	CMOS	28	1	64	4	YES	1
444C	CMOS	28	2	128	4	YES	1
444L	NMOS	28	2	128	16	YES	1
440	NMOS	40	2	160	4	YES	4
402	NMOS	40	0	64	4	YES	1
404L	NMOS	48	0	160	16	YES	4
404C	CMOS	40	0	128	4	YES	1
*420H	NMOS	28	1	64	4	YES	1
*444CH	CMOS	28	2	128	2	YES	1

* IN PRODUCTION 1H87

HARDWARE — SUPPORT — SOFTWARE

MOLE (Microcomputer-On-Line-Emulator) consists of two hardware components and software for a host computer. The two hardware components are a general-purpose Brain board that is common to all National microcontroller μCs and a personality board, which plugs into the Brain board and is specific to the particular National μC being supported. COP is supported by one of the personality boards.
The general-purpose Brain board works in conjunction with a terminal or host computer such as the IBM PC. With the personality board plugged in, it provides the platform for both hardware and software development.
Application hot line: (408) 721-5582

Mole software is intended for user's host computer and is written for MS-DOS and CP/M operating systems. It includes COP crossassemblers.
Note: National originally had just CP/M system-based software using 8-in floppies, but now it bows to the popular trend and emphasizes IBM PC-based hosting.

COP800

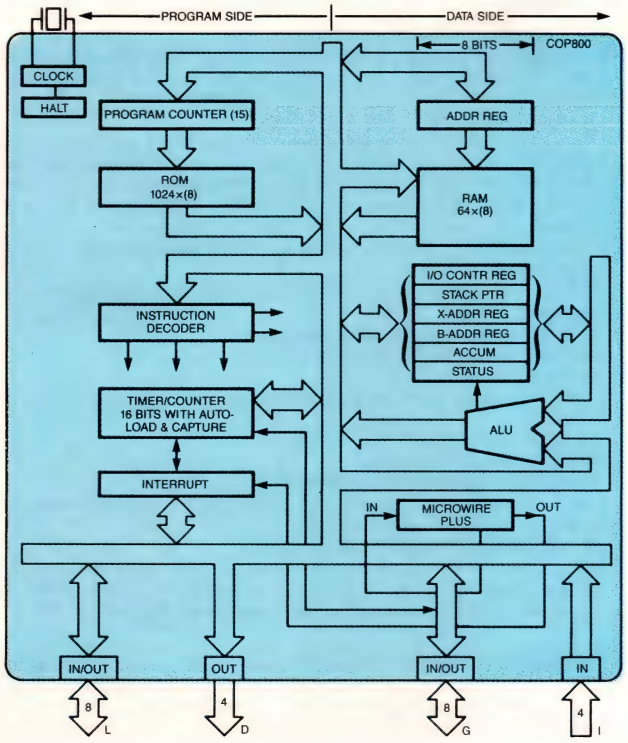
AVAILABILITY: Now for 1k ROM standard and EEPROM. Third quarter '87 for 2k ROM standard and EEPROM. First quarter '88 for 4k ROM standard and EEPROM
COST: $2 to $5 for standard parts, 10k qty
SECOND SOURCE: Sierra Semiconductor
CORE: Will be standard cell in National ASIC library

National Semiconductor Corp
Microcontroller Marketing MS 16-174
2900 Semiconductor Way
Santa Clara, CA 95051
Phone (408) 721-5582

Description: 8-bit CMOS one-chip family in which a purposely simple core μP is surrounded by varying amounts of memory, peripheral functions, and I/O. Some 20 parts exist or are in the works, and many more are forecasted for future. Initial core has provision for addressing 32k-bytes program memory and 256-bytes data memory, but that can be expanded in future. The program and data memory are treated separately; so, like the 4-bit COP400, the COP800 is Harvard architecture. Otherwise it seems more similar to von Neumann common-memory machines such as the Motorola 6805 (or National's 16-bit one-chip 16040).

Status: Having gained one of the leadership positions in the 4-bit-microcontroller field with its COP400, and having produced a 16-bit μC (the 16040), National has introduced this 8-bit controller to fill in the gap. The architecture of the core μP seems quite simple—a bit like the Motorola 6508—so it can be assumed that National was aiming at a small, low-cost core that would leave room and price margin for lots of memory, peripheral functions, and I/O. According to National, this family was also considered as an entry into ASIC from the start. It's being manufactured on National's new state-of-the-art 6-in. wafer line in Arlington, TX.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Add, Add with carry, subtract and carry
Logicals including rotates, shift compares and conditionals
Decimal correct
Increment and decrement
Bit manipulation: set, reset and test individual bits in data memory, which includes those in data registers and I/O ports
II—DATA-MOVEMENT INSTRUCTIONS
Load and exchange instructions with optional automatic post increment or decrement of the associated pointer. Most allow the use of either the B or X pointer
Decrement register and skip if zero
III—PROGRAM-MANIPULATION INSTR
Jump instructions: relative, absolute, absolute long, indirect
Subroutine, subroutine long, return and skip. (Subroutine levels are limited only by the amount of available RAM)
Push and pop
IV—PROGRAM-STATUS-MANIP INSTR
ALU-driven decision bits in status register (PSW) appear limited to carry and half-carry flags. They can be set and reset as well as interrupt control bits for various on- and off-chip interrupt sources
V—POWER-SAVING INSTRUCTIONS
Halt mode, entered by setting data bit and exited by resetting bit
Note:
The program-branch decisions are implemented in skip-the-next-instruction manner.

PART #	ROM	RAM	EEPROM (ROM)	EEPROM (RAM)	SUPPLY VOLTAGE	INTER-RUPT	TIMER	I/O	PINS	FEATURES
COP820C	1k	64×8			2.5-6.0	4	1	24	28	STANDARD
COP821C	1k	64×8			2.5-6.0	4	1	20	24	STANDARD
COP822C	1k	64×8			2.5-6.0	4	1	16	20	STANDARD
COP8620C	1k	64×8		64×8	2.7-6.0	4	1	24	28	SMALL EEPROM
COP8621C	1k	64×8		64×8	2.7-6.0	4	1	20	24	SMALL EEPROM
COP8622C	1k	64×8		64×8	2.7-6.0	4	1	16	20	SMALL EEPROM
COP8720C		64×8	1k	64×8	2.7-6.0	4	1	24	28	EMULATOR
COP8721C		64×8	1k	64×8	2.7-6.0	4	1	20	24	EMULATOR
COP8722C		64×8	1k	64×8	2.7-6.0	4	1	16	20	EMULATOR
COP840C	2k	128×8			2.5-6.0	8	2	24	28	STANDARD
COP848C	2k	128×8			2.5-6.0	8	2	36	40	STANDARD
COP8640C	2k	128×8		64×8	2.7-6.0	8	2	24	28	SMALL EEPROM
COP8648C	2k	128×8		64×8	2.7-6.0	8	2	36	40	SMALL EEPROM
COP8740C		128×8	2k	64×8	2.7-6.0	8	2	24	28	EMULATOR
COP8748C		128×8	2k	64×8	2.7-6.0	8	2	36	40	EMULATOR
COP880C	4k	192×8			2.5-6.0	8	2	24	28	STANDARD
COP888C	4k	192×8			2.5-6.0	8	2	36	40	STANDARD
COP8680C	4k	192×8		64×8	2.7-6.0	8	2	24	28	SMALL EEPROM
COP8688C	4k	192×8		64×8	2.7-6.0	8	2	36	40	SMALL EEPROM
COP8780C		192×8	4k	64×8	2.7-6.0	8	2	24	28	EMUALATOR
COP8788C		192×8	4k	64×8	2.7-6.0	8	2	36	40	EMULATOR

Specification summary: 8-bit Harvard (split-memory) architecture μC in CMOS. 15-bit program counter (PC) can address 32 bytes program memory that can include data and data tables. Initially the on-chip memory selections will be 1k, 2k, and 4k bytes. 8-bit data-address register can address 256 bytes of data. Initial plans are for up to 192 bytes RAM on chip along with optional 64 bytes EEPROM. All data, control, and I/O registers are mapped into the data-side memory space. Up to two bidirectional 8-bit and two unidirectional 4-bit I/O ports. Each I/O pin has software-selectable options to adapt the chip to specific applications. Maximum speed is 1-μsec instruction cycle (most instructions take one cycle), and because part is static CMOS, it will run down to dc and won't lose data in memory. Clock for 1-μsec cycle is 20 MHz. Fabricated in double-metal silicon-gate CMOS (2 μm). Will operate over 2.5 to 6V supply range and draws 15 mA running full speed at 1-nsec cycles, but less than 1 μA when halted. Packaged in 20-, 24-, 28-, and 40-pin DIPs and surface-mount packages. MIL-spec temperature range (−55 to +125°C) versions planned.

Hardware Notes:
1. Diagram shows the basic COP800 family architecture. More than 10 basic parts planned for the family. Each basic part has two companion parts created by adding EEPROM to the data-memory space and replacing standard masked-ROM with EEPROM in the masked-ROM address range.
2. Note that COP800 has three timers: a watchdog timer, an idle timer, and a 16-bit timer/counter with auto reload and capture.
3. The μP core is around 18 sq mils area, so would take up only about ⅓ of reasonable-sized chip. Therefore, there will be adequate room for basic memory, I/O, UARTS, A/D converters, additional timers, and LCD display drivers, as well as custom features for specific applications (ASIC).

HARDWARE — SUPPORT — SOFTWARE

Supported on National MOLE (Microcomputer-On-Line-Emulator), which consists of Brain mother board and COP800 personality board. MOLE can be used in conjunction with IBM PC as host (as well as some other computers, including those with CP/M operating systems).

Cross assembler and C compiler for IBM PC and other computers. C compiler adheres to Kernighan & Ritchie but has extensions for interrupt handling and 1-byte subroutine calls. Supports assembly-language insertions.

PIC1600 Family

8-BIT NMOS AND CMOS

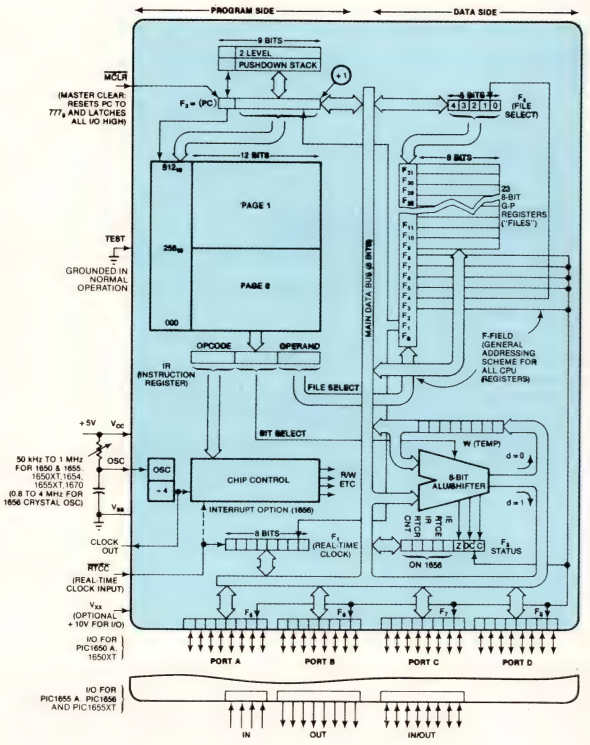
AVAILABILITY: Now for 1652, 1654, 1657, 16E57, 1655A, 1670, 1672. Newer Si-gate CMOS models are being further delayed for redesign to lower cost
COST: All less than $5 at 5k qty, with small-ROM parts (1652 and 1654) under $1 at 50k qty. ($2500 mask charge refundable after 10k qty shipment)
SECOND SOURCE: Plessey

General Instrument Corp
Microelectronics
2355 W Chandler Blvd
Chandler, AZ 85224-6199
Phone (602) 345-3287

Description: Family of 1-chip μCs that ranges from small 18-pin 1652 with 256×12-instruction capacity to 40-pin 1672 with 2k×13-instruction capacity. PIC1670 and PIC1672 have interrupt. Currently, mostly NMOS with one metal-gate CMOS member. Supplier has been "defining" silicon-gate CMOS parts for two years now.

Status: Although PIC design concept goes back 13 yrs, μP is still seeing volume demand—over 7 million units in '85 or 4.5% of 8-bit-μC market, according to Dataquest. The supplier's delay of silicon-gate CMOS parts may hurt family's longevity. For very large orders, price has dropped to well under $1 for 1652.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Add and subtract, decimal adjust (PIC 1670)
Logicals
Rotate right and left, decimal adjust
Swap halves
Bit set and clear
II—DATA-MOVEMENT INSTRUCTIONS
All RAM (general- and special-purpose registers) accessible by direct or indirect addressing
Page addressing
Move file
III—PROGRAM-MANIPULATION INSTR
Skip if zero (for comparisons and bit tests)
Move literal to W
Call subroutine
Go to routine
IV—PROGRAM-STATUS-MANIP INSTR
Can bit test on status-register carry, decimal carry and zero. Interrupt-status bits on PIC 1670 and PIC 1672
Notes:
1. Diagram applies to original 1655A. See tables and these notes for features of others.
2. 12/13-bit-wide instruction word allows all instructions to be single word, which produces compact code; supplier claims benchmarks show almost double the code efficiency of 8-bit instruction word.
3. All devices are NMOS single 5V with event counters. PIC 1670/2 has a 6-level PC-save stack; 1650A and 1655A have 2-level stack.
4. Si-gate CMOS parts promised back in '84 for second quarter '85 are still being delayed by redesign to reduce chip size to compete with Japanese CMOS prices.
5. 16E57 is n-channel Si-gate nitride with 3-μsec instruction time. It has 32×8 EEPROM that can be erased and rewritten by software in 25 msec. 10-yr data retention is claimed over −40 to +85°C. (Applications are for security devices, radio tuners, auto odometers, and maintenance reminders.)
6. Safety-conscious auto designers said to like way all program ROM locations contain instructions (no data trailer bytes), so glitch on program counter less likely to cause misalignment.

PART	ROM (12-BIT WORD)	RAM (BYTES)	INPUT LINES	OUTPUT LINES	BIDIR I/O LINES	INTER-RUPTS	I_{CC} (mA)	PINS	ROMLESS SUPPORT CHIP	AVAIL
REPRESENTATIVE CURRENT DEVICES										
PIC 1652	256	32	—	—	12	NO	50	18	PIC 1664	NOW
PIC 1654	512	32	—	—	12	NO	50	18	PIC 1664	NOW
PIC 1655A	512	32	4	8	8	NO	50	28	PIC 1664	NOW
PIC 1657[1]	512	32	—	—	20	NO	50	28	PIC 1664	NOW
PIC 16E57	512	32	—	—	20	NO	50	28	PIC 1664	NOW
PIC 1670	1k×13	64	—	—	32	3	100	40	1665	NOW
PIC 1672	2k×13	64	—	—	32	3	100	40	1665	NOW

Specification summary: Split-memory architecture with 12/13-bit-wide program ROM and 8-bit-wide data registers. Instructions executed in 4 μsec (1.6 μsec for PIC 1670, 2 μsec for PIC 1654) at 1- or 4-MHz clock (except when a condition test is true, then 8 (2) μsec). The instruction set is strong in bit manipulation and logicals. Devices are fabricated in economical ion-implanted metal-gate NMOS (except for 1652, -4, -7, -70, -72, which are silicon-gate NMOS) and need only one 5V supply at 2 to 70 mA. Not expandable in memory because intended for self-contained, stand-alone applications.

HARDWARE — SUPPORT — SOFTWARE

PICES II (PIC In-Circuit Emulation System) ($2500) turns any computer that supports CP/M Basic into a PIC microcomputer development system via two RS-232C channels. Contains a GI CP1600 μP as its control processor, 2k words of RAM, and personality modules with a ROMless PIC for emulation and prototyping of all available μCs. The 4×4-in. PIC field-demo board for emulation of the PIC series contains a ROMless PIC, two EPROMs, and 18-, 28-, or 40-pin cable with IC plug. Among the PFD boards available are:

PART	μC EMULATED	EPROM	PRICE
PFD1007	PIC1654	IM6654	$150
PFD1020	PIC1670/2	2716	$150
PFD3000E	PIC16E57/53	IM6654	$150

PIC crossassembler (PICAL) runs on any standard computer or μP development system with Microsoft Basic (to run under CP/M). PICAL produces an object-code module that can be downloaded to a PICES II or punched on paper tape. The PICES II resident 12k monitor software consists of an emulator and debug program and provides multiple hardware breakpoints, selectable trace, single-step capability, symbolic debug, instruction disassembly, instruction execution time, and self-test capability.
Literature: GI has prepared an enlarged applications manual that includes programs for fixed- and floating-point math, closed-loop motor-speed control, A/D and D/A conversion, etc. Ask for "PIC Series Microcomputer Data Manual," April 1983 edition, if still available.

8048 Family

8-BIT NMOS AND CMOS

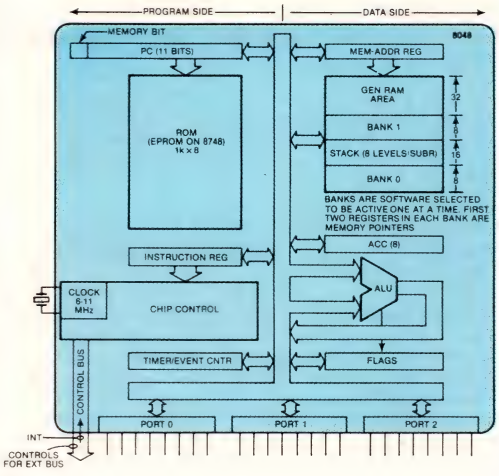
AVAILABILITY: Now for NMOS and CMOS (12 MHz)
COST: Masked-ROM parts $2 in high volume (100k qty). EPROM parts cost $18 in 100 qty. CMOS parts cost as low as $3 in 100k qty. Windowless-PROM parts cost $8 in 5k qty
SECOND SOURCE: Toshiba, NEC, Signetics/Philips, National, Oki, Siemens, Fujitsu, GE-Intersil, UMC (Taiwan), in rough order of volume and with leading Japanese sources outstripping prime source Intel.
CORE: Zymos has been using 80C49 as core for semicustom for a number of years. Others are following because 8048/49 combines widespread popularity with reasonably small core size.

Description: Broad family of 1-chip controller-type μCs, including version that can function as slave (8041). Basic models don't have serial communication ports (some versions from Philips do), but they can use 8080/85 peripherals for I/O expansion. See 8051 listing for enhanced version.

Intel Corp
ECO (Embedded Controller Operation)
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051

Status: Still the leading 8-bit one-chip family, based on Dataquest unit volume figures for '85. Total family shipments were 45 million units or 27% of the market. But there's a continuing trend for OEM designers to migrate upwards to 1-chip devices with more memory and more I/O functions, because the larger 8049 has displaced the 8048 (26 million 8049s vs 18 million 8048s in '85). The trend to CMOS seems more pronounced among the Japanese suppliers, perhaps because they were first to have low-cost CMOS versions. Prime supplier Intel persists in its claim that it is not turning away from 8048/49/50 in favor of its newer and more capable 8051 and 8096 families; in fact, Intel says its unit shipments of 8048 family are doubling every six months.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic
Bit set and reset
Two working banks of 8-bit registers
II—DATA-MOVEMENT INSTRUCTIONS
Both internal and external RAM are fully accessible by instruction set.
Indirect and direct data fetches
III—PROGRAM-MANIPULATION INSTR
Decrement and skip if zero
Over 20 conditional branches
8-level stack with expansion capability
Two vectored interrupts
Two programmable flag bits under software control
IV—PROGRAM-STATUS-MANIP INSTR
Status word is fully accessible and is stored in the stack
Note: Described are the 90 basic instructions for the 8048/8748.

Notes:
1. Diagram is for basic 8048. Table indicates some of other basic parts, most of which exist in both NMOS and CMOS.
2. CMOS parts are designated 80C48, 80C49, 80C50, etc.
3. There are many other variations on basic 8048 among the many suppliers. For example, Intel's 8041/42 chips are software compatible but can be configured as slaves to host μPs for interface applications. The National NS 405/455 use the 8048 core as basis of a terminal controller. Siemens has telecomm-oriented 80C382/482. A number of semicustom houses use the 8048 as a core processor in their libraries.

PART	MEMORY (BYTES)			PACKAGE PINS	
NO	ROM	EPROM	RAM	PARALLEL I/O	TOTAL
8035	0	0	64	3×8	40
8048	1k	0	64	3×8	40
8748	0	1k	64	3×8	40
8039	0	0	128	3×8	40
8049	2k	0	128	3×8	40
8749	0	2k	128	3×8	40
8040	0	0	128	3×8	40
8050	4k	0	256	3×8	40

Specification summary: Split-memory architecture with 1k to 4k bytes of program ROM (or EPROM) on chip and 64 to 256 bytes in separate space, also on chip. I/O has its own space and instructions to operate directly on I/O ports. All spaces are expandable: program memory to 4k bytes, data memory to 512 bytes, I/O to unlimited amounts. I/O can use 8080/85 peripherals. Devices have 8-level stack for subroutine nesting and interrupt response. Dual banks of working registers allow rapid context switching. Family members execute their 1- and 2-cycle instructions at 1-cycle times ranging from 1.36 to 15 μsec. NMOS 5V technology in 40-pin DIP and 44-pad chip carriers; UV-erasable ROMs (EPROMs) and windowless PROM parts are available. CMOS versions available with idle and power-down features and optional flatpack packages.

HARDWARE — SUPPORT — SOFTWARE

From Intel: ICE-49A In-Circuit Emulator ($6495) provides full 11-MHz emulation speed for 8048, 8049 and 8050AH. The emulator is hosted on Intel's Intellec Series II, III, and IV, which are microcomputer systems for software development and include hardware/software integration tools. The Series III and IV allow control of the prototype target system through the in-circuit emulators. System upgrades include hard-disk drive and networking capability to IBM PCs and VAX/VMS systems.
From NEC: Ekakit 84C-1 stand-alone emulator ($2000)

From Intel: ASM-48 package with linker to run on Intel microcomputer Development Systems running ISIS operating system ($1500 for 8-copy license).
From others: Because of the broad-based popularity of this family, dozens of independent sources of development and application software exist, including support on universal development systems from Tektronix, Futuredata, Sophia, etc.
Program library: Insite library contains variety of application programs.

8051/8052 Family

8-BIT NMOS AND CMOS

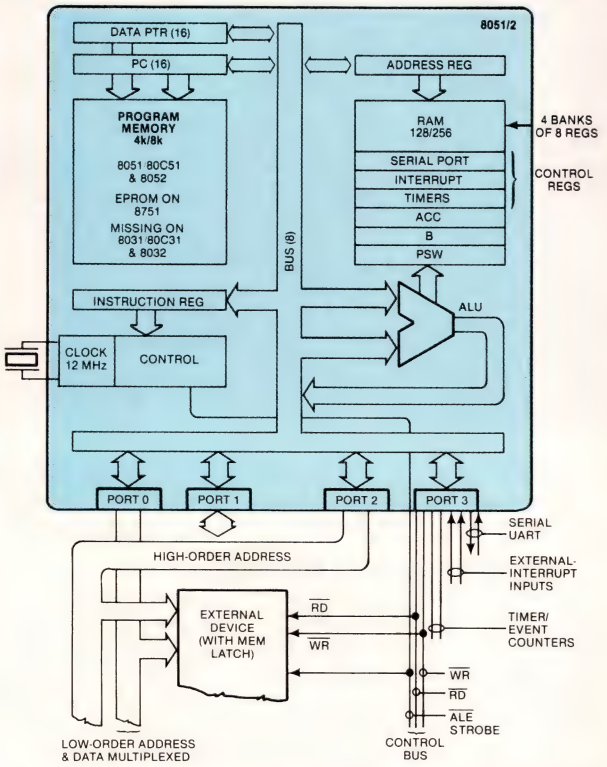
AVAILABILITY: Now for 8051, 80C51, 8031, 80C31, 8751, 87C51, 8032, and 8052 as well as special versions from second sources (see notes)
COST: $4.50 in 100k qty for 8051; $32 in 1k qty for 8751; $6.50 in 100 qty for 80C51; $5.35 in 100k qty for 8052; $44 for 87C51. $70 for EEPROM UPI-452 slave version, 1k qty)
SECOND SOURCE: Siemens, Signetics/Philips, AMD, Fujitsu, Oki, and Harris (Matra, France) licensed
CORE: Intel's new ASIC Components Group (Santa Clara, CA) considers the 8051 as their starting μP core.

Description: Expandable single-chip "controller," an enhanced version of the same supplier's widely used 8048 family. Architecturally, it features the more regular nonpaged form of addressing for easier programming, more interrupts with extra RAM register banks to service them, increased stack depth, and instructions such as multiply, divide, and compare. In peripheral support, it adds a full-duplex hardware UART and enlarged timer/counter capability.

Intel Corp
ECO (Embedded Controller Operation)
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051

Status: Generally acknowledged as the leader among the newer, more powerful 8-bit 1-chip μCs. According to Dataquest, the 8051 suffered a setback in '85 (probably because of the industry-wide slump), but still some 17 million units were shipped (10% share of 8-bit-μC market). It faces stiff competition from both high-end 8-bit μCs such as Motorola's 68HC11, NEC's 7811, Mitsubishi's 50740 version of the 6500/1, and National's new COP800 as well as from the new 16-bit μCs such as Intel's own 8096, National's 16040, and Thomson's 68200. However, based on the overwhelming popularity of 8051 with third-party supporters, it seems safe to say that 8051 will retain a leading position among microcontrollers.

HARDWARE CHARACTERISTICS SOFTWARE



Specification summary: Expandable 1-chip μC. Split-memory architecture has 4k- to 8k-byte ROM on chip and 128 to 256 bytes of RAM on chip. External memory expandable to 128k bytes. Four 8-bit ports on chip, but only one of these remains a port when all off-chip expansions and on-chip special functions are used. Special functions included on chip are full-duplex hardware UART (to 500k baud), two or three 16-bit timer/counters, and interrupt system to service these internal functions along with two external interrupts with 3- to 7-μsec latency. Instructions are a superset of the 8048's, with paged addressing eliminated. At 12-MHz clock, most instructions take 1 μsec; multiply or divide requires 4 μsec. Supplier's high-density HMOS silicon-gate n-channel technology used to achieve small die size and good speed. Packaged in 40-pin DIP and 44-pad chip carriers. 8051 is also available in CMOS (80C51) with 12- or 16-MHz performance and idle/power-down modes.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic, including add, subtract, multiply, and divide
Bit manipulation, including complex tests on bits (and branching on results)
II—DATA-MOVEMENT INSTRUCTIONS
Register addressing for the eight working registers in the four register banks
Direct, immediate, and indirect data addressing for more general data accessing
Table look-up in ROM via data pointer
III—PROGRAM-MANIPULATION INSTR
Depth of subroutining limited only by available space in 128- or 256-byte on-chip RAM
Conditional jumps on status-register flags
Conditional jumps on comparisons
Vectored interrupts to service two external interrupts, timers, and UART
IV—PROGRAM-STATUS-MANIP INSTR
CPU's program-status word fully accessible via software. Status bits in timer and UART also software accessible

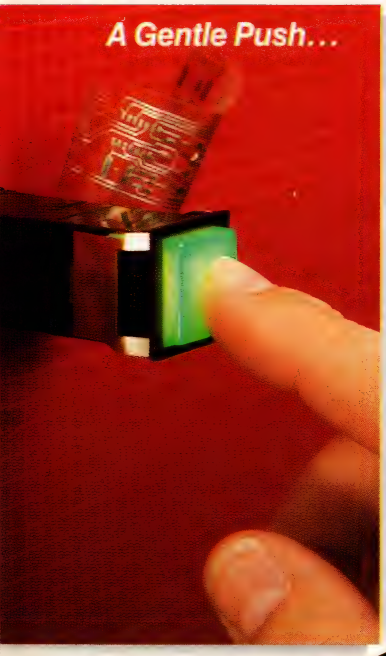
Notes:
1. The eight members of the 8051 family have between 128 and 256 bytes of RAM and differ mainly in their amount and form of on-chip ROM. The 8051 and 80C51 incorporate 4k bytes of masked ROM. The 8751 and 87C51 have 4k bytes of EPROM. The 8031 and 80C31 have no on-chip ROM. (Hence, because it must use ports to access external memory, only port 1 is available for I/O.) The 8052 has 8k bytes of masked ROM. The 8032 has no on-chip ROM. The 8052 and 8032 have 256 bytes of on-chip RAM.
2. The 8051's so-called Boolean-processor capabilities refer to the way instructions can single out bits in RAM, accumulators, I/O registers, etc, and perform complex bit tests and comparisons, then execute relative jumps based on results.
3. The slave version of 80C51, the UPI-452, is a counterpart of UPI-42 (8041/42) for 8048 family. It's intended for software-customizable interfaces.
4. Intel has one model of 8052 preprogrammed with a full Basic interpreter.
5. Siemens is developing proprietary enhancements called 80515 family. They feature 8k ROM with 8-bit I/O ports, 15-μsec 8-bit A/D with eight input channels, 12 interrupts with four programmable priority levels. They are 12-MHz (1-μsec cycle) NMOS, packaged in 68-pin PLCC and 88-pin PGA. Prices are $8 in 1k qty.

HARDWARE SUPPORT SOFTWARE

From Intel: ICE-5100/252 in-circuit emulator ($6995) supports the entire MCS-51 family including 8051, 80C51, and 80C52. Comes with macroassembler and editor. The emulator is hosted on an IBM PC AT/XT running DOS 3.1 or later, as well as Intellec Series III/IV development systems.
ICE-51 in-circuit emulator ($6000) hosted on Series III/IV Intellec supports 8051 at 12 MHz.
EMV-51A Emulation Vehicle ($2995) hosted on Intel's Personal Development System (iPDS). Includes macroassembler.
SDK-51 System Design Kit ($950) is a single-board computer for low-cost development of 8051 applications.
From Siemens: Meta-ICE-80515 in-circuit emulator for 80515, hosted on IBM PC.

From Intel: ASM-51 and PL/M-51, both containing a relocation and linkage utility, are available for the IBM PC and Intel Microcomputer Development Systems running either iNDX for ISIS operating systems. Price is $750 for single-user license.
From others: A number of third-party software suppliers have developed C-language compilers for 8051 that have special features suited to microcontroller applications. One from Micro Computer Control (Hopewell, NJ) sells for $1495; one from Archimedes Software (San Francisco, CA) sells for $851. Both are hosted on IBM PC.

Electro-Mech Introduces Dual Touch.™ Total Control of Two Switches in One.



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CIRCLE NO 63

6804/6805

8-BIT NMOS AND CMOS

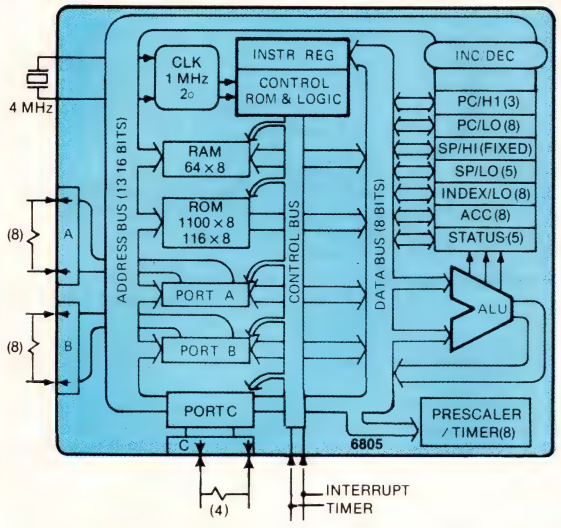
AVAILABILITY: Now for most models, but with continued introduction of new models
COST: $0.49 to $40. The $0.49 is 1M qty of 6804J1 (500k minimum order). CMOS parts remain more expensive than NMOS
SECOND SOURCE: Hitachi, RCA, Thomson Semiconducteurs, and AMI. RCA for CMOS parts only
CORE: Motorola and NCR have joint ASIC pact that will use CMOS 6805 as core along with NCR's similar 6502 μP core. RCA (now with GE) also uses CMOS 6805 as core. SGS has S6 core, which has an architecture that's somewhat similar to the 6804's.

Motorola Microprocessor Products Group
Highway 290 W at William Cannon
Austin, TX 78762
Phone (512) 440-2000

Description: Still-growing family of 1-chip μCs based loosely on 6800 architecture (but in some ways more like 6502). Family offers various amounts of I/O, RAM, and ROM. Internal bus frequencies span dc to 2 MHz. Some parts contain on chip an A/D converter, PLL frequency synthesizer, EEROM, serial I/O, and software security. The 6804s are meant to be lowest end and use some serial data paths internally to reduce chip size to as small as 113×98 mils.

Status: Supplier's steady commitment to this family over past seven years has apparently paid off; '85 Dataquest figures show the 6805 has grown to nearly 14% of the 8-bit-μC market, attaining a volume of nearly 23 million units/yr. It's second only to the 8048/49 family (which has 27% of 8-bit-μC market). Newcomer RCA is concentrating its efforts on the CMOS side of family and is bringing out its own enhancements. For some reason, the 6805's little sister, the 6804, has not caught on. Dataquest showed '85 volume at only ½ million units.

HARDWARE CHARACTERISTICS SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
All 6800 arithmetic, logic, and shift instructions. Bit set, clear, and branch on bit test (bit tests can be made quite generally on all I/O and memory bits). 68HC05 has 8×8 multiply
II—DATA-MOVEMENT INSTRUCTIONS
Relative addressing allows data relocation
True indexing within the 256-location limits of 8-bit index
III—PROGRAM-MANIPULATION INSTR
18 conditional branches, including branch of interrupt line test
Mostly the same conditional branches of the 6800, but with more emphasis on branch upon bit and interrupt tests
Only 15 levels of subroutine nesting, including interrupt returns; 31 levels on certain new parts
Four sources of interrupts: external, timer, software, and reset. 68HC05 has vectored interrupts to service its serial communication and peripheral interfaces
IV—PROGRAM-STATUS-MANIP INSTR
Instructions for manipulating bits in status register (and in timer)
V—POWER-SAVING INSTRUCTIONS
CMOS 6804s and 6805s have Stop and Wait instructions and will safely reset themselves when the clock is applied again

Specification summary: Common-memory architecture, in which instructions, data, I/O, and timers all share the same memory space. This allows I/O to be bit rotated, bit manipulated, etc. Dedicated bit manipulation includes bit set/clear and branch on bit set/clear. A 4-MHz oscillator provides a 1-MHz internal cycle on most -05 versions. New 68HC05s have a 2.1-MHz internal bus speed. Included are parts with program security, on-chip EEROM, A/D converter, serial peripheral interface (SPI), and PLL frequency synthesizer. Family consists of NMOS and CMOS parts in 20-, 28-, and 40-pin DIPs (also chip carriers, etc). NMOS requires 5V supply; CMOS will operate over 3 to 6V.

Notes:
1. Diagram is for nonexpandable Model P2 in 28-pin package.
2. Comparison of 6805 with 6800: Stack pointer has only five working bits, so stack is only 32 bytes deep. Only one accumulator. Index register only eight bits wide, so it can only span 256 memory locations. Program counter only 11 bits (adequate for P2's 2k-byte RAM+ROM memory space). Only one external interrupt.
3. Note additional 116 bytes in ROM for built-in self-check program that tests I/O, ROM pattern, RAM, and interrupts. Program is initiated by special pin.
4. RCA has emulator versions (68EM05/C4,C5) for prototyping and low-volume production. These are ROMless devices with all ROM access buses brought out for direct interfacing to industry-standard EPROMs. Come in 68-pin PCC or 40-pin piggyback (for 2732).
5. Hitachi has "ZTAT" EPROM versions that come in windowless packages for economical short-run production (to 10k).

RANGE OF FEATURES

FAMILY		SPEED BUS (MHz)	INSTR	ON-CHIP ROM	MEM RAM	I/O PINS	TIMER	INTER-RUPTS	POWER CONSUMPTION (mW)	PINS
6804	MIN	0	42	0.5k	32	16	—	3	0.01	20
	MAX	2	42	2k	128	20	YES	4	~400	28
68HC04 P3			42	1.7k	128	20 +2	YES	1	NA	28
6805	MIN	0	51	1k	64	16	—	3	0.01	28
	MAX	2	59	4k	176	32	YES	5	~700	40
68HC05	MIN	0	62	2k	96	32	YES	2	0.25	40
	MAX	2.1	62	7.7k	176	32	YES	2	0.25	40

NOTES:
1. CMOS VERSIONS CAN BE STOPPED (CLOCK = DC). IN THIS CONDITION POWER DROPS TO 10 μW.
2. SOME 6805 DEVICES CAN BE EXPANDED EXTERNALLY TO 8k MEMORY. RCA 6805E3 BRINGS OUT 16 LINES FOR 64k ADDRESS SPACE.
3. SPECIAL FUNCTIONS SUCH AS SERIAL COMMUNICATION PORTS & A/D CONVERTERS ARE AVAILABLE AMONG FAMILY MEMBERS.

HARDWARE SUPPORT SOFTWARE

From Motorola: HDS-200 hardware/software development station; operates stand-alone or interfaced to virtually any host with an RS-232C line (including Motorola's Exor-trademarked stations). The less costly 68705EVM (HMOS) or 1468705EVM (CMOS) boards, which have ports to a terminal and host computer, provide target-system emulation.
From RCA: Single-board evaluation kit that will interface to IBM PC via RS-232C.
From others: A number of third-party companies provide hardware emulators for the 6805 family: Sophia Systems (Santa Clara, CA), American Automation (Tustin, CA), etc. Most of these interface to IBM PCs.

From Motorola: Cross macroassemblers with linking loaders and resident macroassemblers for all Motorola Exor systems.
From others: Many cross macroassemblers and linking loaders, some relocatable. RELMS (San Jose, CA) has cross support for Intel development systems. Avocet Systems Inc (Rockport, ME) has crossassemblers for 6805 and 6804 that run on IBM PC, etc.

6801/6301/68HC11/68HC811

8-BIT NMOS AND CMOS

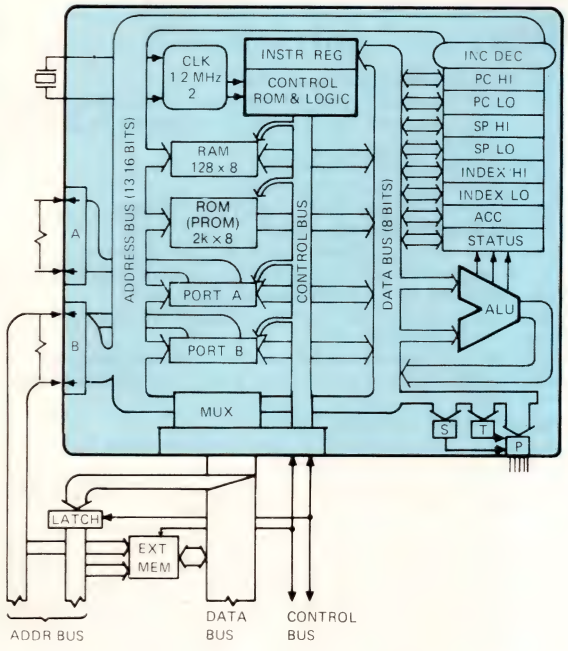
AVAILABILITY: Now for 6801, 6301, and 68HC11
COST: In 1k qty, from under $3 to $40 for 6801. $11.80 for Hitachi 63701VOP ZTAT windowless EPROM. $19.95 for 68HC11A8 in 1k qty; $125 for 68HC811A2 in low volumes
SECOND SOURCE: Hitachi, AMI, Thomson Semiconducteurs. Hitachi is prime source on the 63XX CMOS versions

Motorola Microprocessor Products Group
Highway 290 W at William Cannon
Austin, TX 78762
Phone (512) 440-2000

Description: 6801 is large, expandable 1-chip version of the 6800, with enhancements that include 10 more instructions, serial I/O, 8×8 multiplication, and a multifunction 16-bit timer. 6301 is slightly enhanced CMOS, and 68HC11 is further enhanced in static CMOS. 68HC11 has a second 16-bit-wide register, an 8-function timer, a 2-function pulse accumulator, an enhanced UART (SCI), a high-speed (1-MHz) serial shifter (SPI), an 8-channel, 8-bit A/D converter, and an EEROM.

Status: This has been a well-received family with over 12 million units/year in '85, according to Dataquest (8% share of market). Motorola is now following migration of customers to more powerful 1-chip devices and is concentrating on the new 68HC11 enhancement of the 6801, such as increased on-chip EEPROM. Apparently this is one broad-based market that hasn't been hit so hard by the slump in demand for personal computers.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic
Instructions to take advantage of two accumulators, including 8×8 multiply. 68HC11 has additional 16-bit operations, integer and fractional divides, and bit manipulation
II—DATA-MOVEMENT INSTRUCTIONS
Can reach the first 256 locations of memory with short instructions
Can list-process efficiently with the index register (two on 68HC11) and can add accumulator to index register, within a 64k-byte range
Relative addressing allows data relocation
Has 16-bit load and store
III—PROGRAM-MANIPULATION INSTR
Has PDP-11 branches and conditional branches. Has unlimited subroutine nesting via stack pointer, addressing LIFO stacks in RAM
Eight levels of prioritized, vectored interrupts (21 on 68HC11)
IV—PROGRAM-STATUS-MANIP INSTR
Instructions for storing status register or transferring to or from accumulator. 68HC11 has additional active bits related to "stop" mode
V—POWER-SAVING INSTRUCTIONS
6301 has sleep instruction. 68HC11 has Stop and Wait instructions similar to 146805 but with disabling provision via a bit in status register
Notes:
1. 6801 has all instructions of 6800 μP plus 10 new ones to handle additional resources such as advanced serial I/O ports and timers.
2. 68HC11 has enhanced 6801 instruction set, with 88 additional op codes.

PART	DESCRIPTION	MEMORY ON CHIP ROM	MEMORY ON CHIP RAM	EXT	INTERNAL BUS SPEED	I/O PAR	I/O SER	TIMER EVENT CTR	EXT INTS	PINS
6801	EXPANDABLE 1-CHIP μC	2k	128	64k	0.5M–2.0M	29	3	3×16	2	40
68701	EPROM VERSION OF 6801	2k	128	64k	0.5M–2.0M	29	3	3×16	2	40
6803	ROMLESS 6801	—	128	64k	0.5M–2.0M	13	3	3×16	2	40
68HC01 6301	CMOS	4k	128	64k	0–2.1M	28	3	1×16	2	40
C8HC03 6303	CMOS	—	128	64k	0–2.1M	17	3	1×16	2	40
68HC11	CMOS WITH UART, SPI, SERIAL, 8-BIT A/D	8k (ALSO 512 EEPROM)	256	64k	0–2.1M	28 32	6	4×16	2	48 (DIP) 52 (QUAD)

Specification summary: Expandable single-chip μC with common-memory architecture, in which all instructions, data, I/O, control, and data registers share the same memory space. This allows I/O, etc, to be handled like memory with all instructions applying. Instruction set is upwardly compatible with 6800, with 10 additional instructions for 6801 and, beyond that, 91 new op codes for 68HC11. The ROM, RAM, and I/O resources for 6801 and 68HC11 families are as detailed in table. Internal bus speed to 2 MHz for 6801 and from dc (asleep) to 2.1 MHz for 68HC11. The 6801 fabricated in NMOS, 6301 fabricated in CMOS, and Motorola 68HC11 fabricated in static CMOS (to allow dormant, micropower "asleep" state). 6801 in 40-pin DIP, 6301 in 64-pin DIP and flatpack, and 68HC11 in 48-pin DIP and 52-pin quad.

Notes:
1. Diagram is for 6801. See table for others.
2. Hitachi has developed some slightly enhanced CMOS versions, the 63XX Series, that Motorola has second sourced. "ZTAT" versions, such as 63701VOP, have EPROM program memories in inexpensive windowless packages for one-time programming in moderate-volume production (to 10k).
3. Motorola 68HC11 is very enhanced 6801. New 68HC11A8 has 512 bytes EEPROM. 68HC811A2 has 2k bytes EEPROM. EEPROM said to be handy for storing field and factory calibrations.

HARDWARE — SUPPORT — SOFTWARE

From Motorola: For 6801 family, MEX6801/MEX6801U4 development systems. Requires Motorola Exorciser/Exorterm with Debug software, 24k bytes of RAM and Exordisk II with MDOS. M68701EVM is evaluation module that has port for terminal and port for any RS-232C host and will program 68701 EPROM parts. For 68HC11, the similar M68HC11EVM. Also M68HC11EVB boards ($168.11) for evaluating EEPROM versions. For both 6801 and 68HC11, HDS-300 software-development station operates stand-alone or interfaced to most hosts with RS-232C.
From others: Third-party hardware emulators for 6801 family. For example SA1000/2000 Universal Development Systems ($7995) from Sophia Systems (Santa Clara, CA).

From Motorola: MEX6801/MEX6801U4 comes with necessary software. Cross macroassemblers with linking loaders for Motorola Exor systems. C compiler to run on Unix System V for 68HC11. For least expensive approach, you can use 6801 parts with LILbug monitor in on-chip ROM (MC6801L1).
From others: Cross macroassemblers and linking loaders, some relocatable, to run on popular minis and personal computers.

6500/1, 65C124, 50740

8-BIT NMOS AND CMOS

AVAILABILITY: Now for NMOS parts from Rockwell and NCR. Rockwell continues to schedule CMOS parts but NCR has canceled its CMOS plans (although its cores are only CMOS). CMOS parts from Mitsubishi have been in high volume for several years.
COST: Prices range from $2 to $20 according to complexity of part and volume, whether in NMOS or CMOS.
SECOND SOURCE: NCR (licensed) and GTE for Rockwell; WDC says it will soon announce a second source; Mitsubishi says Rockwell will be second source.
CORE: As standard megacell in libraries of NCR, Mitsubishi, WDC, SMC, etc (widely used because of compact 6502 die size).

Rockwell International
Semiconductor Products Div
4311 Jamboree Rd
Newport Beach, CA 92660
Phone (714) 833-4700

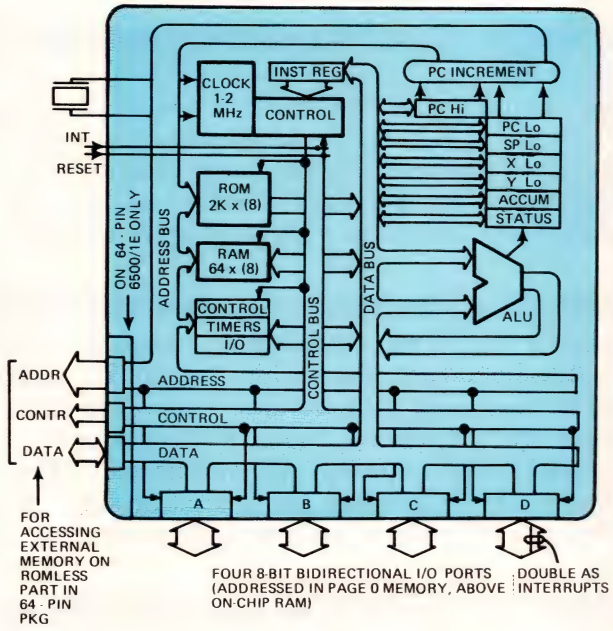
Western Design Center Inc
2166 E Brown Rd
Mesa, AZ 85203
Phone (602) 962-4545

Mitsubishi Electronics
America Inc
1050 Arques Ave
Sunnyvale, CA 94086
Phone (408) 730-5900

Description: There are three different sources for 1-chip versions of 6502 μP: the original 6500/1 family from Rockwell, the new 65C124 from WDC, and the very successful 50740 family from Mitsubishi. Most parts are 100% software compatible with the 6502, though in some cases enhanced instructions such as bit manipulation have been added. Because of small die size of the 6502 core, many of these parts are being designed via the standard-cell-library approach.

Status: According to Dataquest, Mitsubishi's 50740 Series reached 13½ million units in '85. Mitsubishi claims the 50740 has 35% of the CMOS 8-bit, 1-chip market. Rockwell's 6500/XX has achieved only a modest volume (2 million in '85 according to Data Quest), which means that its market share is still small (just over 1%) compared with other 8-bit, 1-chip devices (8051 and 6805/6801). Vendors claim 6502-based families have a speed advantage over competing 1-chip devices because of 6502's 2-cycle bus and pipelining.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logical. Decimal mode via control bit in status register. Can operate on locations in memory space (which can be either RAM or I/O ports)
Bit-manipulation enhancement on some models allows bit set and reset and branching on bit set or reset
II—DATA-MOVEMENT INSTRUCTIONS
True indexed addressing, though index offset limited to eight bits in two CPU registers—X and Y. Short-form addressing to zero page. Has two sophisticated indirect-indexed and indexed-indirect instructions for handling tables
III—PROGRAM-MANIPULATION INSTR
Conditional branches with signed relative addresses
Nonmaskable and/or maskable interrupt, depending on model
IV—PROGRAM-STATUS-MANIP INSTR
Push and pull status register from memory stack. Set and clear carry, decimal mode and interrupt bits
Notes:
1. 6500/1 instruction set is 100% identical to that of previous 650X-family devices such as 6502, with exception of bit-manipulation instructions for some devices.
2. No new instructions added to handle new on-chip features like timers and I/O because they are all handled as if in external memory space.

Notes:
1. Diagram favors initial Rockwell 6500/1 version. There are dozens of versions among the various sources, most of which are more complex.
2. Rockwell has a version (65F11/12) with run-time kernel of fig-Forth language in on-chip ROM. Forth application programs can be developed with aid of RG65FR external ROM and external RAM. Dynatem (Irvine, CA) has a board for it.
3. Mitsubishi 740 Series parts are all CMOS and have up to 8k bytes of ROM and 256 bytes of RAM. Some models have special functions such as UARTs, 8-bit A/D converters, LCD drivers, or high-voltage (−35V) outputs.
4. GTE has 65SC150, an enhanced 1-chip version with I/O suited to telecomm modems. Includes a dual 26-step sine-wave generator. In low-power mode (300 μA), device can be powered by telephone line. For ROMless model, price is $14.25 (1 MHz) to $15.90 (2 MHz) (100).
5. Like GTE, Rockwell is favoring communications market for newer models, such as 65C14 communications μC.
6. WDC says its first part, the 65C124, will use core strategy and be for a medically implantable μC that will have a token-passing serial interface.

Specification summary: 1-chip nonexpandable and expandable versions of 650X family. Have 2k- to 8k-byte ROM, 64- to 256-byte RAM, as many as 52 I/O lines, and one or two 16-bit programmable interval timers, as well as two or more programmable interrupts (plus the 650X's NMI interrupt). Family options (Rockwell) include RS-232C port and bus expansion. Operates from 5V, 500 mW and has separate 5V supply to keep 64 static bytes of RAM alive (50 mW required). Wide variety of package types and sizes from various suppliers, ranging up to an 80-pin flat pack from Mitsubishi. Full MIL-spec temperature range devices from WDC.

HARDWARE — SUPPORT — SOFTWARE

From Rockwell: Emulator part, the $75 64-pin 6500/1E, can be used in $995 R6500/1 personality card, which plugs into LCE System ($1250). Backpack part will be ROMless 40-pin 6500/1EA ($75), into which industry-standard EPROMs can be plugged.
From Mitsubish: Debugging machine PC4000E ($1000) with ICE cards for each device model ($750 to $1100).
From WDC: Toolbox design system that runs in conjunction with Apple IIe.

From Rockwell: Because the 6500/1 emulator runs on LCE System and Aim-65 (now from Dynatem (Irvine, CA)), existing 6502 program-development software can be used. A debug monitor is available for all 6500/1 and 6500/11 devices, and the macroassembler supports new (enhancement) instructions. Cross software for Intel ISIS-II, RDC-200 ($250 to $750). 65F11 and 65F12 devices have resident Forth kernel (an adaptation of fig-Forth-79 with additions for control of floppy disks and EEPROMs.)
From Mitsubishi: Cross software for MS-DOS, CP/M, and ISIS-MDS.

DAISY IS ENGINEERING

BULLETIN:

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1-800-824-2385 in CA.
Department D57.

For information on Daisy's growing Semicustom Design Solutions, and the Daisy product line, call the Daisy Literature Line at 1-800-556-6661 (in California, 1-800-824-2385) Department D **57**, or write the Daisy Literature Line, 3606 W. Bayshore Rd., Palo Alto, California, 94303.

Z8, SUPER8

8-BIT NMOS AND CMOS

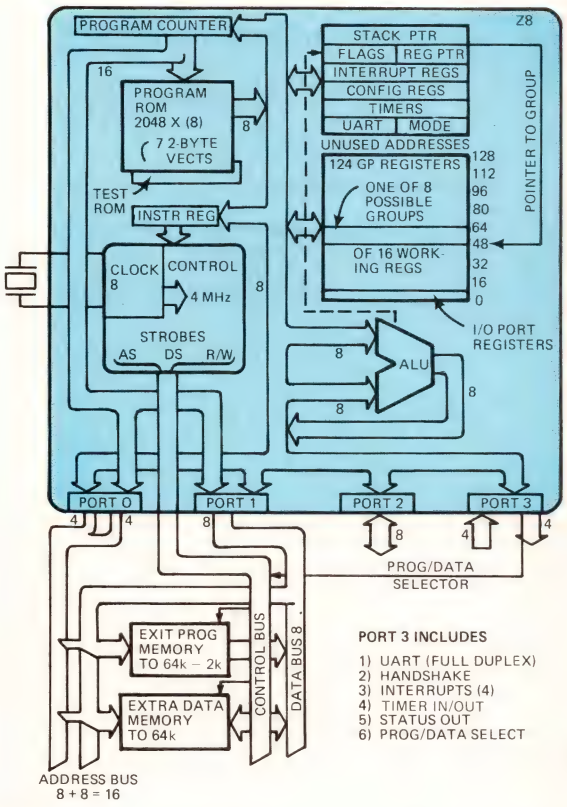
AVAILABILITY: Now for 2k-byte, 4k-byte, and ROMless parts at 8 and 12 MHz. Samples of Super8. Sharp and Zilog have CMOS now. SGS is sampling 4k EPROM and expects 8k ROM and EPROM in first quarter '87.
COST: Less than $3.50 for Z8 in volume; $6.50 for Super8 in volume (28-pin version for $1).
SECOND SOURCE: SGS (licensed); Sharp for both NMOS and CMOS; Seeq (not licensed) for EPROM version.
CORE: SGS's S9 core in 1.5-μm CMOS is based on Super8 architecture.

Zilog Inc
1315 Dell Ave
Campbell, CA 95008
Phone (408) 370-8000

Description: Z8 is a "maxi" single-chip μC that's a composite of many machines. It has powerful features that can't necessarily be used simultaneously, a common problem with single-chip units—particularly the expandable ones. Not really compatible with supplier's Z80 or Z8000 because architecture is so different; closest to Z8000. However, slave Z8 versions interface to the Z80 and Z8000 buses. Super8 version has more data and program memory, more on-chip peripherals, and more instructions.

Status: Z8 is both a large, ambitious chip with a different architecture. The Super8 enhancement is even larger and more ambitious. Supplier predicts Z8 will reach 12-million-unit level in '87, and says demand is increasing for $1 28-pin Z8, which is directed at appliance and brown goods applications. (Dataquest showed a volume of under 3 million for '85). Second-source Sharp has shipped a good portion of the Z8s, and second-source SGS says it is doing original design work shrinking parts and integrating Super8 as core into a semicustom cell library.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Diagram applies to basic 2k-byte version. Many other versions exist.
2. The 124 working registers (272 on Super8) are truly general purpose. Any one can be used as accumulator or indexer.
3. The register pointer singles out a workspace of 16 working registers for fast access. Eight such workspaces are possible in the 124-register space (16 in Super8) and provide mechanism for fast context switching upon interrupt.
4. The data- and program-manipulation instructions use the working registers in the CPU. The instructions that apply to the external data RAM are essentially just loads and stores. (There is a similarity to RISC philosophy.)

I—DATA-MANIPULATION INSTRUCTIONS
Add, add with carry, decimal adjust, increment byte and word, decrement byte and word, subtract, subtract with carry
Multiply and divide added to Super8 version
Logicals: AND, compare, complement, OR, and exclusive OR
Rotates and swaps
Bit manipulation: test under mask, test complement under mask, and logical tests of bits
II—DATA-MOVEMENT INSTRUCTIONS
The following address modes: immediate, register, register pair, indirect register, indirect register pair, direct, indexed, and relative
Block transfer: load constant autoincrement, load external autoincrement
Load: clear, load, load constant, load external, pop and push.
III—PROGRAM-MANIPULATION INSTR
Call, decrement-and-jump on nonzero, interrupt return, jump conditional, jump relative conditional, return
IV—PROGRAM-STATUS-MANIP INSTR
Set, reset, and complement of carry flag
Note: Ability to set, reset, and test any bit or combinations of as many as eight bits allows any byte to function as a user flag register.

Specification summary: Unique architecture with three memory spaces: program memory (2k or 4k bytes in internal masked ROM; rest up to 64k can be external), data memory (60k bytes external), and a CPU register file (a 256-byte space that includes 124 truly general-purpose working register/accumulators). Executes 129 instructions at 1.0 to 3.0 μsec at 6-MHz internal clock (12-MHz oscillator). Has built-in duplex 96k-bps UART and two 8-bit timers, each with 6-bit prescaler. NMOS chip originally measured 220×220 mils (shrinks under way) and requires only one 5V supply. Housed in 40-pin DIP; 28-pin economy versions planned. New enhanced Super8 has 352 bytes of on-chip data and control registers—256 are general purpose. Will initially be a ROMless part, but as much as 16k bytes of on-chip program ROM is expected. New multiply and divide instructions. On-chip peripheral functions include DMA, two 16-bit timer/counters, up to 40 I/O lines, full-duplex UART, and optional synchronous/asynchronous serial channel. Has fast (600-nsec) interrupt response, with 37 interrupt sources. On-chip oscillator now 12 MHz for 6-MHz internal speed, but will be 20 MHz giving 10-MHz internal clock. Comes in 48-pin package.

HARDWARE — SUPPORT — SOFTWARE

From Zilog: Zilog has dropped its hardware support systems and now refers customers to third parties (see below).
From SGS: Emulator for software/firmware developed on SGS UX-8/22 development system ($2200). Interface for IBM PC ($3000).
From Microtek (through New Micro, Gardena, CA): MICE-II ($4600 to $5600) real-time emulation system for Super8.
From Creative Technology (Atlanta, GA): Super8 Emulator ($1195) low-cost system for use with IBM PC. Documents, $50.
From others: Hardware development tools for Super8 from Orion Instruments and Sophia Systems.

From Zilog: A version of Z8 with Tiny Basic in ROM (Z8671) that allows stand-alone self-programming of chip. Super8 with Forth.
From SGS: Emulator package including debugger, disassembler, and trace function. Crossassembler for use with IBM PC.
Software (crossassemblers, etc) is also available from HP, Tektronix, 2500 AD, Western Ware, Avocet; for Super8, Allen Ashley, 2500 AD, Creative Technology, and Microtek.

7000 FAMILY

8-BIT NMOS AND CMOS

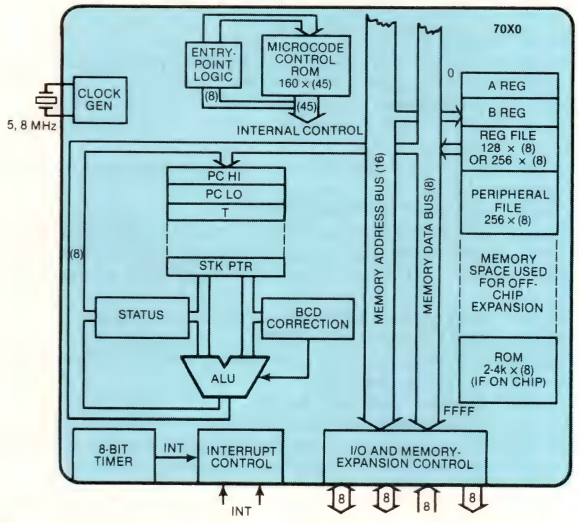
AVAILABILITY: Now for NMOS, NMOS EPROM, and CMOS. EEPROM NMOS from Seeq. 8k CMOS 77C82 promised by second quarter '87.
COST: 1987 pricing: NMOS, in 10k qty, from $2.78 for ROMless 7000 to $5.44 for 7042. $3000 mask charge. CMOS parts more expensive, ranging (in 10k qty) from $3.68 for ROMless 70C00 to $5.85 for 70C42. $6000 mask charge.
SECOND SOURCE: General Instrument (NMOS), Seeq (72720 "self-programmable" EEROM version).
CORE: See comments on "SCAT" architecture.

Texas Instruments Inc
Programmable Products Div
Box 1443
Houston, TX 77001
Phone (713) 879-2490

Description: Compatible family of NMOS and CMOS 8-bit expandable 1-chip μCs. Architecture laid out on chip so that new product variations in memory size, I/O, etc, are easier to accomplish. A full-duplex UART, enhanced timers and interrupts are incorporated on high-end family members. Instructions typically perform combined load, operation and store functions, thereby increasing overall system performance and code efficiency.

Status: Dataquest figures up to '85 indicate that this device has not gained much share of market—less than 1% in unit volume (about 1½ million units/year). However prime supplier TI has continued to bring out new CMOS models with expanded features, and promises an 8k ROM CMOS device by mid '87. Meanwhile second-source GI says that it has stayed with NMOS and has not only gone to 8k ROM, but on to 10k and 12k (parts that TI doesn't second source).

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, 8×8 multiply, BCD
Logicals, increment, decrement (single and double)
Rotates right and left. Bit test
II—DATA-MOVEMENT INSTRUCTIONS
Dual-operand moves avoid time wasted going through accumulator.
Apply to many instructions
Indexing via the B register
16-bit moves
III—PROGRAM-MANIPULATION INSTR
Call and return
Bit test and jump on both I/O and memory
Conditional jumps using PC-relative addressing
IV—PROGRAM-STATUS-MANIP INSTR
Status register contains carry, sign, zero, and interrupt enable. Instructions to change carry and interrupt enable

Note:
Supplier says it uses a "strip-chip" architecture (SCAT) to keep registers and control elements in isolated, self-contained modules in silicon, then uses single layer of metal to interconnect chip. This is similar to the cell-library, semicustom approach. Changes can be easily made, which helps TI bring out new models or give large customers special variants.

MODEL	ROM (kBYTES)	CLOCK (MHz)	INTERRUPT LEVELS	POWER REQUIRED VOLTS	POWER REQUIRED mWATTS
NMOS FROM TI					
7000	0	5	4	5	400
7020	2	5	4	5	400
7040	4	5	4	5	400
7002	0	8	6	5	400
7042	4	8	6	5	400
7742	4 (EPROM)	5	6	5	400
NMOS FROM GI					
7060	6	5/10	4	5	500
7080	8	5/10	4	5	500
70100	10	5/10	4	5	500
70120	12	5/10	4	5	500
CMOS FROM TI					
70C00	0	5	4	2.5-6	30
70C20	2	5	4	2.5-6	30
70C40	4	5	4	2.5-6	30
70C02	0	6	6	2.5-6	30
70C42	4	6	6	2.5-6	30
77C82	8 (EPROM)	8	6	2.5-6	30

Specfication summary: Unified-memory architecture in which application program ROM (EPROM), working registers, I/O registers, and some control registers all share a common memory space of 64k bytes. Low-end family members have an 8-bit timer with capture latch and 5-bit prescale, interrupt, 128 bytes of RAM, and 2k or 4k bytes of ROM (up to 12k ROM for NMOS GI parts). The high-end performance 7042 includes two 16-bit timers that are cascadable to 26 bits (one with capture latch), a UART with an 8-bit timer for baud-rate generation (or usable as a third timer), programmable interrupts, 256 bytes RAM, and 4k bytes ROM. The high-performance model operates to 8 MHz with basic microinstruction cycle taking 250 nsec. Most instructions take five to nine cycles. Miminum instruction time is 1.25 μsec, which includes load, logic, or arithmetic operations, and store. The 8×8 unsigned multiply takes 10.75 μsec at 8 MHz. I/O up to 32 pins with some models, including special functions such as UARTs and A/D. The NMOS and NMOS EPROM devices require a 5V supply; the CMOS operates over 2.5 to 6V V_{CC} and includes power-down modes. Available in 40-pin DIP and 44-pin PLCC.

HARDWARE — SUPPORT — SOFTWARE

From TI: XDS development system ($5000). It provides in-circuit emulation, target system debug (with breakpoints and logic-state trace) and RS-232C link to host computer or terminal. EVM evaluation board ($795) provides in-circuit emulation, programs 7742 and EPROMs, and has serial interface to standard terminals. The 7742 EPROM device and 70P162 piggyback device provide prototyping support for all NMOS family members (-00, -20, -40, -42 devices). The piggyback accepts 2764 and 27128 EPROMs. The SE70CP160 CMOS piggyback device supports prototyping for the 70C20 and 70C40 μCs. The SE70CP162 supports prototyping for the 70C02 and 70C42.

From TI: Crossware is available to run the XDS system from the following hosts: IBM PC-DOS (including TI lookalike), IBM MVS and CMS, DEC VAX VMS and TI Tx4, and AMPLUS and DX10 operating systems.
From Nuvatek Inc: Uniware cross-development software written to run on any UNIX-based host processor.
From Allen Ashley: System-TMS7 provides CP/M cross support with its macroassembler and interactive editor/assembler.
Literature: TI 7000 family data manual with applications, user's guides, etc.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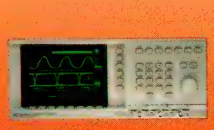

HEWLETT PACKARD

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1800 FAMILY

8-BIT CMOS

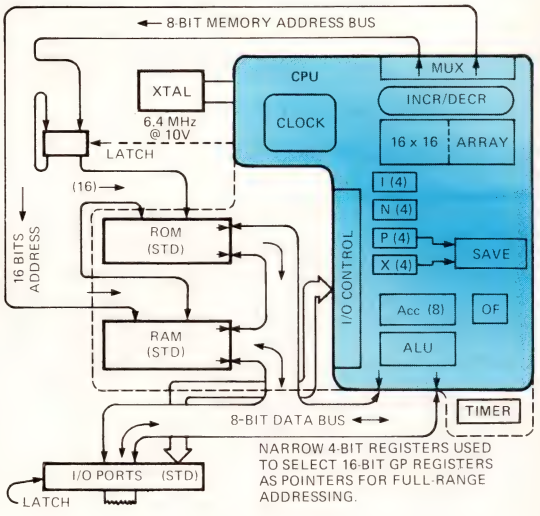
AVAILABILITY: Now.
COST: In 100 qty: $5.49 for 1802A, $17.75 for 1805A, $15 for 1806A, all in plastic.
SECOND SOURCE: Hughes.

RCA Solid State Div
Rte 202
Somerville, NJ 08876
Phone (201) 685-6000

Description: CMOS μP family that has proven suitable for controller applications in severe industrial, automotive, and military environments and for portable applications under battery power. 1804A 1-chip version and its ROMless counterpart (1805A) can be directly retrofitted in existing 1802 sockets for faster execution and enhanced instructions.

Status: A true survivor among the processors we have had in our directory: this CMOS pioneer was included in our first directory in 1974. Now, it's holding a steady volume of more than 2M units/year and a fairly wide (500 to 1000) customer base. The 1800 seems assured of a continued existence, particularly because some of its applications have been in long-lived military and industrial programs. It still occasionally finds its way into new designs because of its known performance in adverse environments. However, RCA is paying more attention to the 6805.

HARDWARE — CHARACTERISTICS — SOFTWARE



1804A 1-chip version (dashed outline) has 2k bytes masked ROM and 64 bytes RAM on chip as well as new built-in timer. But it does not have I/O ports. Instead, it brings out address and data buses like the 1802 and allows external addition of I/O and more memory. The 1802's second supply line (V_{CC}) is used to indicate when external memory is addressed. 1805A is ROMless 1804A, and 1806A is RAMless 1805A. Both 1804A and 1805A can be plugged into existing 1802 sockets to provide enhanced instructions and speed. Hughes is developing special RAM with auxiliary power-fail save area as PROM equivalent. (Note that Hughes has 512×8, 1k×8, and 2k×8 electrically erasable CMOS PROMs or EEPROMs.) RCA and Hughes have external 8×8 multiply and divide chip for 1802 and 1855. Two cascaded 1855s can perform 16×16 multiplication in 10 μsec.

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract and logical (× and ÷ with external 1855)
Reverse subtract (M-Accum)
Right and left shift (with and without carry)
Register-indexed and data-immediate addressing formats
II—DATA-MOVEMENT INSTRUCTIONS
Addressing 2-stage using registers in 16×16 array as pointers
The 4-bit registers select pointers and define their function I/O, interrupt and DMA control built into CPU
III—PROGRAM-MANIPULATION INSTR
Jump to subroutine by having the 4-bit P register address a different GP register in 16×16 array; GP register serves as PC. Return from subroutine by readdressing original GP register as PC. (However, 1804A and 1805A will have standard call and return.) Can use pointers to create multiple stacks in RAM
IV—PROGRAM-STATUS-MANIP INSTR
Mark, save and return instructions used to manipulate interrupt enable and P and X registers
Software maskable interrupt via line into CPU
RCA 1804A/05A/06A have 32 additional instructions. One unused opcode in 1802 is used for "escape," with following byte used to indicate to which new instruction. New instructions include those for 1804A's counter, 16-bit CPU-register loads and stores, interrupts, toggle output enable, eight BCD instructions, and standard subroutine call and return.

Specification summary: Data instructions are in same memory space (64k), but I/O is provided its own space (seven addresses in, seven addresses out). Most instructions are single byte and execute in 3.2 μsec at 5-MHz clock. Static CMOS chip dissipates 10 mW at 3.2 MHz/5V; 40 mW at 6.4 MHz/10V. 40-pin package, 4 to 10.5V supply range, −55 to +125°C operation. Is MIL qualified (SOS versions for radiation-hardened designs have been under development).

HARDWARE — SUPPORT — SOFTWARE

From Matric Ltd (Franklin, PA, (814) 432-2180): Development system, MS2000A, with 3½-in. dual Sony disk drives and Microdos operating system ($6000). Also the Microemulator, MSE3001, which includes CRT and full ASCII keyboard ($6000). These were originally developed by RCA but were sold to Matric, along with RCA's 1800 Family board-level products.
From Hughes: Note that Hughes no longer supplies the H800 universal development system, only application assistance.

From Matric Ltd: Microdos operating-system software included with MS2000 hardware. Included are a macroassembler and a full-CRT-screen text editor with instant update. High-level languages include Basic-1 ($300), a bare-bones integer Basic with compiler option; Basic-II ($500), a full floating-point Basic; and PLM-1800 ($950).
From Hughes: Note that Hughes no longer supplies support other than application assistance.

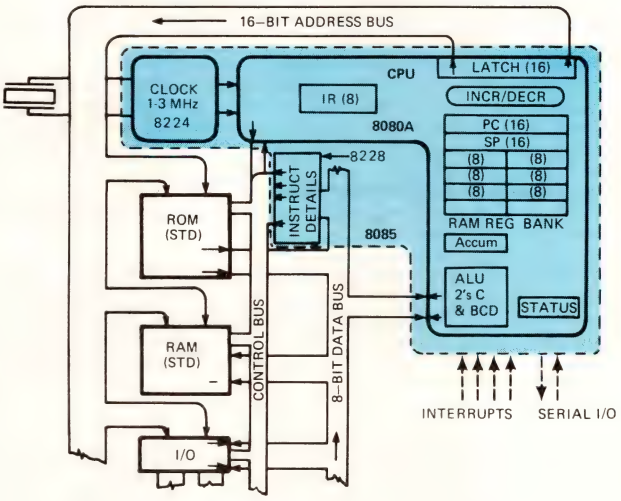
AVAILABILITY: Now for both in NMOS and for CMOS versions of 8085 (80C85).
COST: During present depressed, abnormal conditions in semiconductor market, prices for these older multisourced parts have dropped to $1 and below, with prices as low as $0.65 for volume purchases. CMOS parts, especially faster ones, are more expensive.
SECOND SOURCE: 8080A: Toshiba and NEC had most of market between them in '85, but (in addition to Intel) AMD and Siemens shipped parts. For CMOS 80C85, Oki and Toshiba, with expensive ($300 to $800) nuclear-radiation-hardened military version from Harris.

Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080

Description: Has proven a good general-purpose, midrange μP, though not the most efficient one for small programs. 8085 executes 8080 instructions, but with simpler hardware. Z80 (see elsewhere in this directory) is an enhanced 8080, but with different package pinouts and bus operation. New 8086 (see elsewhere in this directory) is only vaguely software compatible, but 8-bit-bus 8088 version of 8086 can interface to 8080 and 8085 peripherals.

Status: The venerable 8080—the μP that gave legitimacy to the μP revolution—is pretty much obsolete. It dropped to less than 1% of the 8-bit-μP market in '85, according to Dataquest. But the 8085 continues to do well, and Dataquest figures for '85 indicate that 14 million units were shipped, which gave the 8085 28% of the 8-bit-μP market, second only to Z80. Somewhat surprising, the Dataquest figures showed only 1 million CMOS 80C85s were shipped in '85, though Toshiba says it has been adding new CMOS peripherals.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic
BCD arithmetic
Double-precision operations (instructions string two data bytes together as 16-bit word)
II—DATA-MOVEMENT INSTRUCTIONS
Uses three pairs of so-called GP registers as pointers in CPU RAM bank to address low- and high-order bits of 16-bit memory address. Can perform multiple indexing with these, but takes additional steps compared with classical index-register concept. 8085 has two additional instructions—RIM and SIM—that interface with new serial-I/O pins (as well as interrupt system)
III—PROGRAM-MANIPULATION INSTR
Uses stack pointer (SP) to create LIFO stacks in external RAM for unlimited subroutine nesting
All GP registers can be incremented and decremented
Multiple-interrupt capability
Bus controls allow addition of DMA
IV—PROGRAM-STATUS-MANIP INSTR
Software access to status register

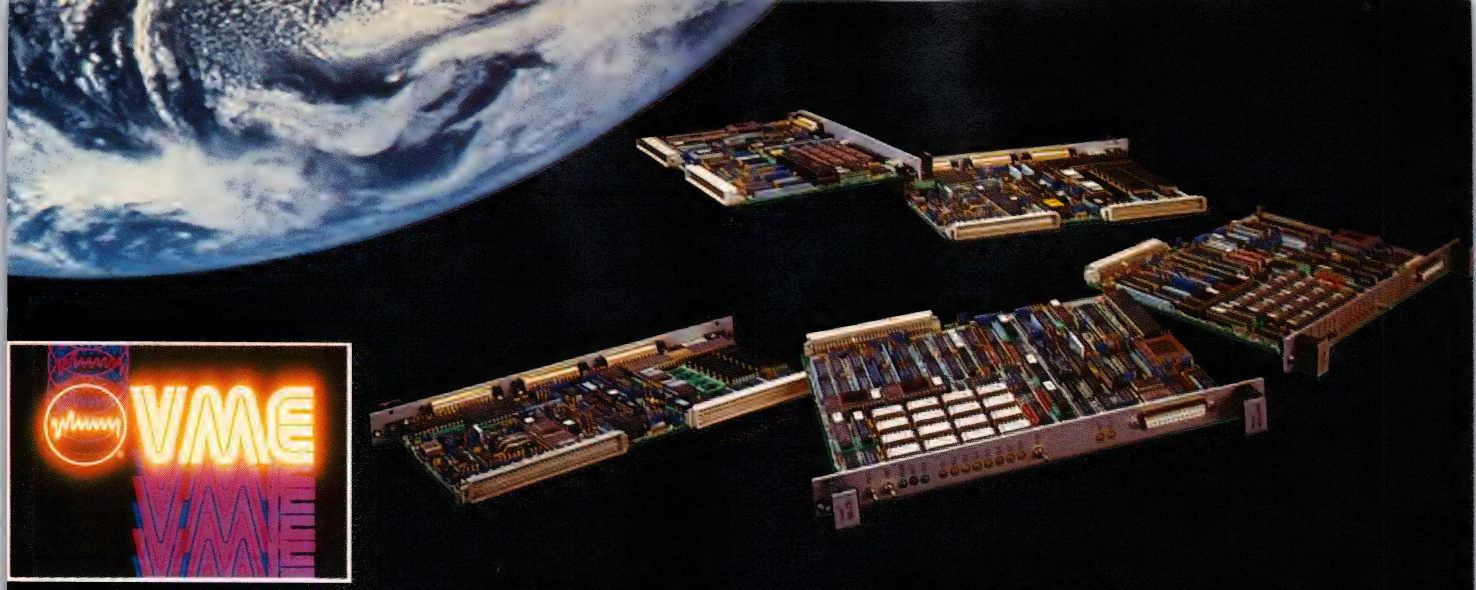
How 8085 differs from 8080:
8085 has on-chip clock, needs only a 5V supply, and has relaxed memory-access time. But because it multiplexes lower eight bits of address on data bus, it's not pin compatible with 8080. New pins gained by multiplexing implement address-latch strobe, four additional interrupts, and two serial-I/O lines. For small "few-chip" 8080 systems, designer can use 8155/56 and 8355/8755 combo chips with built-in address latches.

Specification summary: Common instruction and data architecture (64k bytes) with optionally separate I/O space (256 bytes). Three 16-bit pointer registers allow efficient addressing of 64k-byte main-memory space. 78 basic instructions with 2-μsec typical add-register-to-accumulator execute time. NMOS technology: 8080A requires 2-phase external clock and ±5V and 12V; 8085A has on-chip clock and needs only 5V. High-speed versions—3-MHz 8080A, 5-MHz 8085A—and CMOS versions also available.

HARDWARE — SUPPORT — SOFTWARE

From Intel: Intellec Series IV μP Development System ($6495) for emulator host and software development. iPDS Personal Development System for software development. ICE-85B in-circuit emulator for control of prototype target system ($6495). The SKD-85 single-board computer permits lowest cost processor evaluation and familiarization ($315).
From others: Model 8002A ($9950) from Tektronix and a similar system from Futuredata, plus a new, more expensive system (HP64000) from Hewlett-Packard.
Note: Check with suppliers on these development tools: Some have cut back on their support or introduced less expensive models.

From Intel: Series IV and iPDS Personal Development Systems are available to house an 8080/8085 macroassembler and link/locator utility, as well as PL/M, Fortran, and Pascal compilers and a Basic interpreter. Prices are from $975 for single-user copy to $2600 for 8-copy license.
From others: Most of the many companies that supply 8080 development systems include software. Also, many software houses have 8080 software in every conceivable category. One of the most important is the CP/M operating system sold by Digital Research, Pacific Grove, CA.



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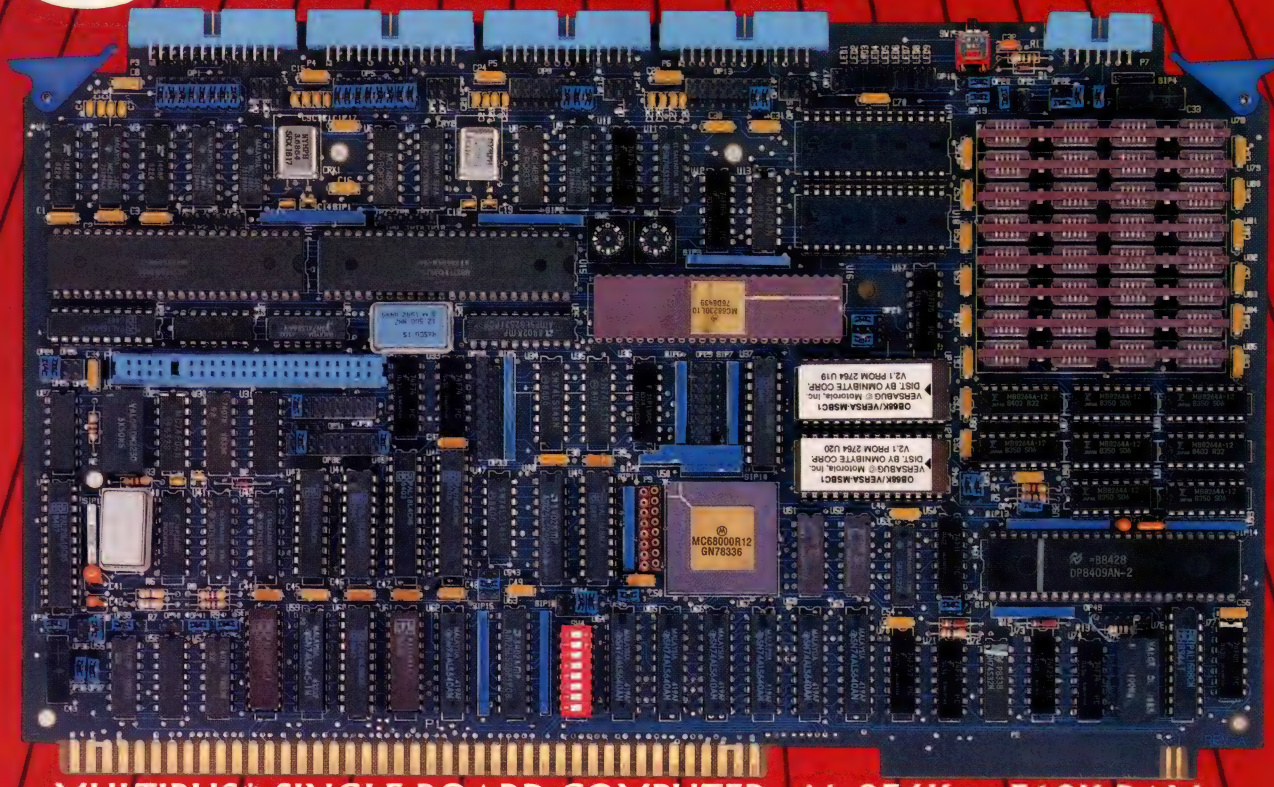

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CIRCLE NO 65

Z80

8-BIT NMOS AND CMOS

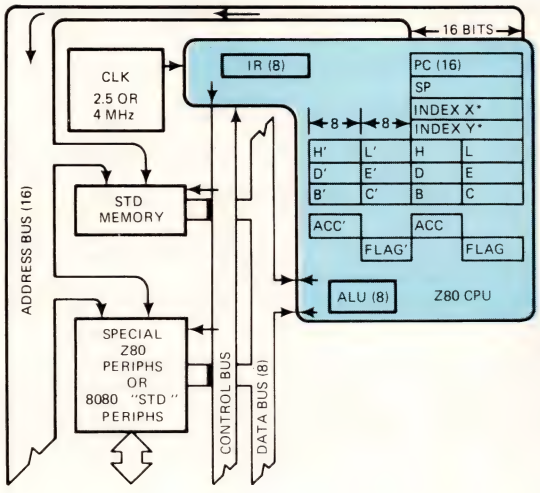
AVAILABILITY: Now for both NMOS and CMOS versions in 6 and 8 MHz.
COST: During last year's recession in the personal-computer market, and because of the many aggressive second sources for this very widely used part, NMOS price dropped to $1 and less in very high volumes; the CMOS volume price dropped to about $1.80.
SECOND SOURCE: NEC, Toshiba, Sharp, SGS (Italy). Toshiba and Sharp were first to have CMOS versions, which may be why Dataquest figures indicate these two Japanese companies took market share from other sources in '85. Additional sources mentioned by Zilog are Gold Star, VLSI Technology, and Rohm.

Description: Superset of widely used 8080/85; adds hardware and software features. Not pin-for-pin compatible with 8080 or 8085, but can use 8080 software and peripherals—though to do so would not take full advantage of the Z80 and its peripherals and might require additional TTL for interfacing.

Zilog Inc
1315 Dell Ave
Campbell, CA 95008
Phone (408) 370-8000

Status: By far the most successful 8-bit multichip μP. Its unit volume dropped from 26 million units in '84 to 18 million units in '85 because of the industry-wide slump, but it retained its 35% share of market, according to Dataquest. The Z80 is still being used in new designs, but may be superceded by the new enhanced versions described in the diagram notes on this page. Of these, the Hitachi 64180 seems to be the top contender, but the Z280 (the ex-Z800), would represent the greatest Z80 enhancement. Whatever happens, one thing is certain: the Z80 has established a momentum that will probably last for the rest of this decade.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
8-bit arithmetic and logicals
16-bit arithmetic BCD add and subtract
Nine types of rotate and shift directly on any register or memory location
Can set, reset, or test bit in any register or memory location
II—DATA-MOVEMENT INSTRUCTIONS
8- or 16-bit register or memory loads
Two index registers allow indexed addressing
Extensive memory-block move/search commands
III—PROGRAM-MANIPULATION INSTR
Uses 16-bit stack pointer with LIFO stack with RAM
Relative-jump capability. Interrupt capability with three types of selectable response
IV—PROGRAM-STATUS-MANIP INSTR
Seven flag bits, including arithmetic and overflow, can be stored and tested

Notes:
1. Support chips include peripheral interface (PIO), timer (CIO), serial communications (SIO), and DMA. All provide daisy-chained vectored interrupt for CPU and are being converted to CMOS.
2. Several enhancements of Z80 exist or are imminent. All are in CMOS. The first of these was the National NSC 800, which never became very popular (less 2% share of unit market in '85). The second is the recently introduced Hitachi 64180, which appears to be off to a good start. The third is the supplier's Z800, now renumbered as the Z280, which, though very impressive technically, has missed so many promised availability dates that it is hard to tell where it's at. Also, the NEC 78XX single-chip device has some similarities. Most are covered elsewhere in this directory.

Specification summary: Upward compatible with 8080A software, but adds 50 instructions, some of which are advance block-move and block-search macros. Instructions executed in 1.6 to 8.8 μsec (3 μsec avg) for 2.5-MHz Z80 and 1.0 to 5.5 μsec (2 μsec avg) for 4-MHz Z80A. 6-MHz and 8-MHz versions also available. User can switch between two identical banks of CPU registers for fast response to interrupts. NMOS circuitry requires single-phase clock and one 5V supply at 60 mA for Z80; 90 mA for Z80A. TTL-compatible I/O and built-in automatic-refresh signals for dynamic RAMs. MIL-temperature parts available. CMOS version consumes only 15 mA at 4 MHz and less than 10 μA when in power-down (clock-stopped) mode. Housed in 40-pin DIP. CMOS versions available also in flat pack and PLCC.

HARDWARE — SUPPORT — SOFTWARE

From Zilog: Zilog has stopped making its PDS and ZDS development systems because there are so many less expensive third-party support systems for the popular Z80. Instead, it supplies Z-Scan emulator boxes that can be used alone or with host computers. The Z-Scan-80 provides emulation for the Z80H ($6695).
From SGS: UX-8/22 development system based on CP/M and two 8-in. floppy disks. Package for full-speed in-circuit emulation.

From Zilog: Software for the various development systems. Macroassembler with relocatable assembler, linking loader, file-maintenance programs, and resident Basic, Cobol, C, Fortran and PLZ. (PLZ is a Zilog-created language that comes in "lower" level that mixes assembly- and system-language statements with a "higher" C language.) Z800 has cross software package (assembler, etc) that runs on DEC VAX or Zilog S8000 under Unix.
From SGS: Software package for UX-8/22, including debugger, disassembler, and tracer.
From others: A great deal of software of all sorts, including the CP/M operating system (Digital Research) and the MSX operating system (Microsoft), which is popular in Japan.

HD 64180, Z180

8-BIT CMOS

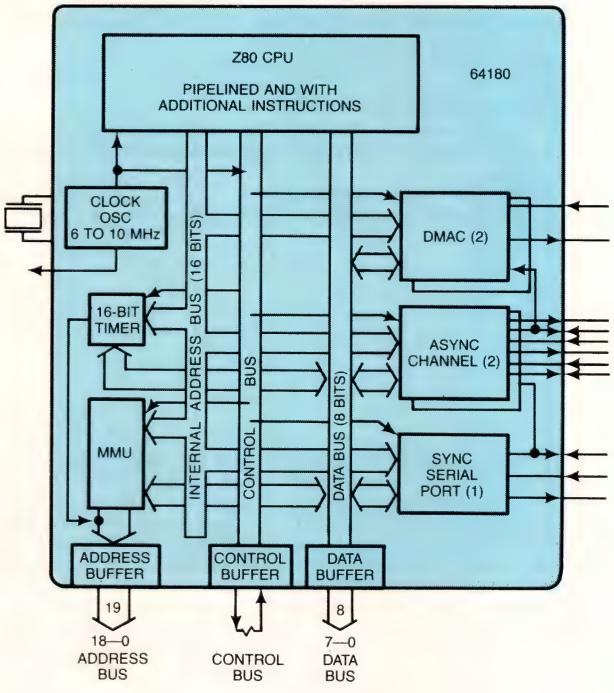
AVAILABILITY: Now for 6- and 8-MHz parts; early '87 for a 10-MHz version and Z180 version that will be compatible with Z80-family peripheral chips.
COST: $17.5 in 100 qty; $15 in 1000 qty.
SECOND SOURCE: Zilog (will do 64180 and Z180).

Hitachi America Ltd
Semiconductor and IC Sales
2210 O'Toole Ave
San Jose, CA 95131
Phone (408) 435-8300

Description: Enhancement of Z80 with various peripheral functions, such as memory management (to reach larger, 1M-byte memory space), DMAs, serial ports, modem control signals, added on CPU chip and realized in CMOS. Z180 version will be compatible with Z80-family peripherals chips.

Status: Yet another CMOS enhancement of the widely used Z80. This one has on-chip MMU, multiple DMA channels, and a UART like the much-delayed Zilog Z280, but it's not as ambitious. It doesn't have sophisticated big-computer features such as separate privileged "system" control registers and a cache. Moreover, the 64180's MMU is not for virtual and protected memory but just to translate between the Z80 64k address space and the 1M-byte space reached externally by the 64180. However, the 64180 has been out a year ahead of the Z280, and customers have been evaluating samples; some are starting production. Based on the interest shown by third-party support, and Zilog's decision to second source the 64180, it appears that the 64180 is off to a good start.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Unsigned 8×8=16 multiply
Nondestructive ANDs for comparing I/O ports, immediate data, and memory to accumulator
II—DATA-MOVEMENT INSTRUCTIONS
Immediately addressed locations
Block output to I/O. (Must set up MMU bank registers to translate between 64k of Z80 and 512k external)
V—POWER-SAVING INSTRUCTIONS
Sleep command disconnects processor from clock. (Interrupt or reset will reconnect)
Notes:
1. Only new instructions beyond Z80 instructions listed.
2. The MMU adds base registers to Z80 16-bit addresses to produce the 19-bit addresses needed externally.
3. Trap interrupt can be used both for catching undefined op codes and for allowing users to extend instruction set.

Specification summary: Object-code compatible with Z80 (and 8080 and 8085). Pipelined CPU. On-chip MMU generates 19 bits (512k to 1M bytes) external physical address space. Two-channel DMAC (direct-memory-access controller), 2-channel asynchronous serial port, synchronous (clocked) serial port. Can interface to 8080 or 6800/6500 buses (Z180 version is matched to Z80-family peripherals). 8-MHz CPU performance now, 10-MHz projected. CMOS 50 mW at 4 MHz with lower power in sleep and halt modes. Packaged in 64-pin DIP and 68-pin PLCC.

HARDWARE — SUPPORT — SOFTWARE

HI80ASE020H Adaptive System Emulator ($6000) plus H6805M01S, a 256k-byte memory board, for use with IBM PC, HP6400, or DEC VAX as host. Real-time operation to 8 MHz and real-time tracer buffer for 2048 machine cycles. All hardware lines are captured, and the trace is automatically disassembled.
American Automation AA 572-64180 real-time in-circuit emulator for use with company's E2-PRO development host.

Microtec Research (Santa Clara, CA) is supplying macroassembler, utilities, Pascal and C compilers (to run on IBM PC and DEC VAX hosts). Also, Avocet (Rockport, ME) and Allen Ashley (Pasedena, CA) have announced IBM PC-based assemblers. Hitachi provides help so that the additional 64180 instructions can be treated as macros on a Z80 macroassembler. Boston Systems Office (Waltham, MA) has VAX-hosted assembler ($3900). Software compatible with CP/M (Digital Research) and MSX (Microsoft) operating systems (latter being result of project for Japanese market).
American Automation has cross-software to go with development hardware (assembler, C compiler, and debugger).

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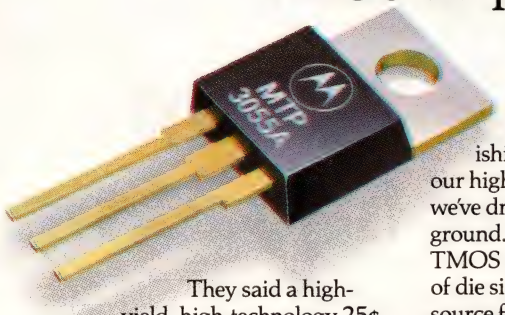

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CIRCLE NO 66

Z280 (ex Z800)

8/16-BIT CMOS

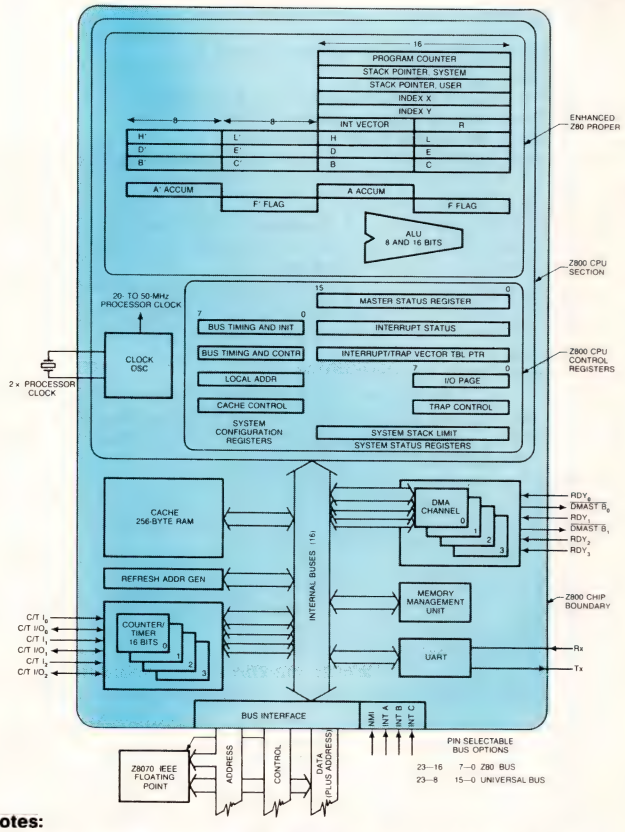
AVAILABILITY: Fourth quarter '86 for samples (10 MHz)
COST: Pricing to be the same as competitive chips, such as Intel 80186, or $15 to $20 in large qty.
SECOND SOURCE: None announced, but supplier says it will complete an agreement in '87.

Description: Enhanced Z80 μP, upgraded so that it has most of the features of larger 16/32-bit machines. It has "privileged" system-control hardware and associated software for multiuser, multitasking operating systems. It has memory management for virtual memory. It incorporates cache to achieve high throughput with ordinary, moderate-speed external memories.

Zilog Inc
1315 Dell Ave
Campbell, CA 95008
Phone (408) 370-8000

Status: By the time this chip is finally in silicon (fourth quarter '86 according to supplier's current promise), more than five years will have elapsed since the chip was first announced (as the Z800) and more than three years since first samples were promised. Hardly a trustworthy record. But this time the Z280 could really be on the verge of appearing: The supplier says it has already done several silicon iterations and has chips that are partially functional and almost up to speed. It will still be of interest to the many people still designing with Z80s because the Z80 is still king of all μPs when it comes to volume use (over 18 million units/year and 35% share of 8-bit-μP market). The Z280 will be of special interest to those engineers wanting to turn Z80 personal computers into multiuser systems with large virtual memories and multi-MIPS performance. While the Z280's realization has dragged out, other competing devices have become real (for example, the Hitachi 64180, which Zilog decided to second).

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Diagram indicates how basic Z80 CPU has been enhanced by adding other functions to the chip. Not so apparent are other enhancements to the Z80 CPU, such as more powerful, generalized 16-bit data and addressing operations.
2. Note that, though this design is largely the same as that originally announced (the preliminary data manuals from '83 and '84 still hold for the most part), there have been several changes:
- Device design has been converted from 2.5-μm NMOS to 2.0-μm static CMOS.
- Instead of giving users choice between maximum configuration (64-pin) package and minimum configuration Z80 (40-pin) package, supplier is only offering a 68-pin package that is pin programmable, so user can choose either 8-bit Z80 or 16-bit "universal" bus mode.

I—DATA-MANIPULATION INSTRUCTIONS
New 16×16 +32 multiply and 32/16=16 divide
Extended block mode manipulates data in blocks. (Can be used with supplier's Z8070 IEEE floating-point coprocessor)
II—DATA-MOVEMENT INSTRUCTIONS
New addressing modes for more general 16-bit use of Z80's 16-bit registers (HL, DE, BC pairs)
Instructions to communicate with coprocessors
III—PROGRAM-MANIPULATION INSTR
Jump on auxiliary accumulator/flag
Jump on auxiliary register file in use
System call
IV—PROGRAM-STATUS MANIP INSTR
New master status register; see category V instructions
V—SYSTEM CONTROL INSTRUCTIONS
New instructions for added system-control registers. These are privileged instructions to permit operating system to define the system configuration upon start-up, to use the new system stack pointer, master status register, and set up the cache's mode of operation
Note: Only those instructions that are enhancements of basic Z80 set are covered. Otherwise, the Z280 is object-code compatible with Z80 (and 8080).

Specification summary: The Z80 enhanced upwards in the direction of a general-register 16-bit minicomputer. On-chip memory management to address as much as 16M bytes of external memory. CPU is 3-stage pipelined with on-chip 256-byte program and data cache to automatically keep recently used instruction on chip for fast—to 2 MIPS—execution at 10-MHz internal bus clock. Planned mask shrinks from initial 2-μm geometry to 1.5 μm are expected to allow 25-MHz clock. Future mask redesigns to 1.2, 1.0, and 0.8 μm are expected to allow further speed improvements to 50 MHz. The I/O is pin programmable to match either 8-bit Z80 bus or 16-bit "universal" bus. Also included on chip are four 16-bit timer/counters, four DMA channel controllers, dynamic memory refresh control, and a serial UART port. Can use supplier's 8070 IEEE floating-point math coprocessor. Fabricated in static CMOS and housed in 68-pin PCC package with other options planned for future as requested by customers.

HARDWARE — SUPPORT — SOFTWARE

Hardware support to be announced by first quarter '87. Manuals should be available soon, because preliminary versions have been out since fall of '84.
Supplier says that two customers are readying Z280-based hardware, some of which may be of help in OEM development.

From Zilog: In addition to assembler, Zilog will provide compilers for high-level languages. Cross software to run on DEC VAX or Zilog S8000 under Unix.
From others: No specific information available, but because there are many suppliers for CP/M-based market, it's likely that there will be good support. EDN has talked with a number of suppliers for the Z80 CP/M market who had been working on enhancements to take advantage of the Z280 but had put these on back burner when they became discouraged with many delays of Z280 project. It's likely that the major software houses, such as Digital Research and Microsoft—both of whom have been associated with Z80 software—have Z280 projects on hold.

6800/6802 AND 6809/6309

8-BIT NMOS AND CMOS

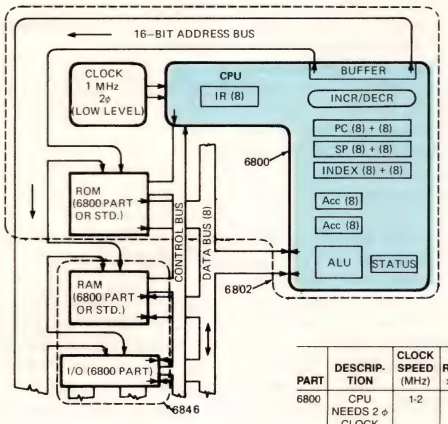
AVAILABILITY: Now
COST: In 1k qty, $3 to $4 for 6800 and 6802; $5 to $6 for 6809. In 100 qty, $9.50 for 3-MHz 6309E.
SECOND SOURCE: Hitachi, Fujitsu, and Thomson Semiconducteurs. Gould (AMI) has dropped out

Description: The 8-bit 6800 CPU was the original part in the family named after it. That family has been broadened to include not only the 2-chip 6802/6846 and 6809 covered here but also the 1-chip 6801, the low-end 6804 and the 6805 1-chip devices, and (loosely) the top-of-the-line 16-bit 6800. Note, though, that new CPU members of family aren't precisely compatible with the original 6800, especially at the low and high ends. Even the 6809 here is only software compatible with the original 6800 at source-code level.

Motorola Microprocessor Products Group
Highway 290 W at William Cannon
Austin, TX 78762
Phone (512) 440-2000

Status: Introduced in 1974, the 6800 has been the foundation of one of the longest lived and broadest μP families. Among its progeny must be included the 6809 covered here and the following Motorola μPs and μCs, which are described elsewhere in this directory: the 6804, 6805, 6801, and 68HC11. The 6800 itself is now way past its prime and is not recommended. We've retained it in the directory for reference. But the newer 6802 and 6809 continue to be shipped in volume. Dataquest showed 4 million units for the 6802 and 3 million units for the 6809 in '85. That gave the family a respectable third place (17% share of market) behind the Z80 and 8080 families. For new designs Motorola tends to steer designers to the 32-bit 68000 family (68008 has 8-bit bus) or to the 1-chip 68HC11.

HARDWARE CHARACTERISTICS SOFTWARE



Dashed lines indicate boundaries of the 6802/6846 2-chip-system parts. The 6802 includes a clock and 128 bytes of RAM; the 6846, 2k ROM, timer and 1/2 PIA port. The first 32 bytes of the 6802 RAM can be saved by battery in power-down mode with 8 mA drain.

PART	DESCRIPTION	CLOCK SPEED (MHz)	ROM ×(8)	RAM ×(8)	AVAIL	COST (100 QTY)
6800	CPU NEEDS 2 φ CLOCK	1-2	—	—	NOW	$4-$5
6802	CPU, CLOCK & RAM	1-2 (4 MHz EXT)	—	128	NOW	$4-$5
6808	6802 WITHOUT RAM	1-2	—	—	NOW	$4-$5
6846	COMBO CHIP FOR 6802	1-2	2k	—	NOW	(CONTACT FACTORY-MASK PROGRAMMED
6875	CLOCK FOR 6800	1-2	—	—	NOW	—
6809	CPU	2	—	—	NOW	$5-$6
6309	CPU CMOS	3	—	—	NOW	$9.50

Notes:
1. Diagram shown is for 6800 and 6802. The 6809 has another 16-bit index and a second "user" stack pointer, which make the 6809 more powerful than the 6800: The 6809 has more instructions made possible by these additional resources. On simple benchmarks, the 6809 is 270% faster than the equivalent-speed 6800, programs in 42% fewer instructions, and uses 33% less code.
2. Basic 6809 version has on-chip clock. A minimum system results with the following parts: 6809, 6810, and 6846. 6809E version has off-chip clock. An early valid-memory-address (VMA) signal on 6809E allows 3-MHz bus operation with a 2-MHz memory. External clock permits multiprocessing.
3. The memory-management unit (6829) allows the 6809 to run 32 concurrent protected tasks (per management unit) in 2M-byte address space.
4. Hitachi CMOS version (6309) will have 2-, 2.5-, and 3-MHz bus timing, and the Sync and CWAI instructions allow a low-power sleep mode.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic
Instructions to take advantage of two accumulators
6809 has unsigned 8×8 multiply with 16-bit product
II—DATA-MOVEMENT INSTRUCTIONS
Can reach the first 256 locations of memory with short instructions
6809 can use four index registers for merging three source blocks into one destination block
Can autoincrement and autodecrement by one or two directly and indirectly. (Page zero can be software relocated during program execution, effectively increasing its size)
Indexing uses the "true indexing" relationship between base and offset (0, 5, 8, 16 bits) rather than the 6800 relationship
Can utilize the user stack for Polish-notation operations or interpretive languages
III—PROGRAM-MANIPULATION INSTR
Has PDP-11 type branches and conditional branches. Unlimited subroutine nesting via stack pointer addressing LIFO stacks in RAM
Does not have vectored interrupt, but can achieve function with software (or with 6828 priority interrupt controller)
6809 has extensive relative addressing with wide reach, which allows creation of position-independent code and opens door to use of off-the-shelf, mass-produced standard firmware in ROMs
IV—PROGRAM-STATUS-MANIP INSTR
6809 has instructions for manipulating the status register (condition-code register). It may be transferred or exchanged with any 8-bit register, or pushed or pulled on either stack; any number of flag bits may be set or cleared in one instruction
IV—POWER-SAVING INSTRUCTIONS
6309 has SYNC and CWAI to put CMOS CPU in sleep mode. Sync instruction stops μP until it gets go-ahead signal from interrupt line

Specification summary for 6800: Common-memory architecture with 16-bit (64k-byte) memory space for instructions, data, and I/O; all data 8 bits wide. Instruction set patterned after the PDP-11 mini as closely as possible in shorter word machine with limited CPU registers. Execution times from 2 to 5 μsec. NMOS silicon-gate depletion-mode circuitry requires one 5V supply, 500 mW; housed in 40-pin DIP. Versions with −55 to +125°C MIL-temperature range also available.
Specification summary for 6809: An 8-bit machine with extensive 16-bit addressing capability. Has two 16-bit index registers and a 16-bit user stack pointer that can also be software-specified as a third index register. Upward compatible with 6800, but only at source-code level. Bus operates at 2 MHz, so basic speed is similar to that of 6800, but greater efficiency of 16-bit addressing significantly increases throughput. Instruction set has 59 mnemonics and seven addressing selections for a total of 1464 instruction-addressing options. Instructions vary in length from 1 to 5 bytes, with register-inherent operations executing in 1 μsec at 2-MHz bus speed (320-nsec memory access). Longest instruction takes 20 cycles. The 6800 direct or page zero register is retained but can be software relocated anywhere in memory via programmable register. Motorola "HMOS" depletion-mode load circuitry with one 5V supply. Two versions, each in 40-pin DIP.

HARDWARE SUPPORT SOFTWARE

From Motorola: Emulators range from low-cost (hundreds of dollars) boards to HDS-300 system (about $5000) plus personality modules ($5000). Support systems and OEM boards available from Motorola Semiconductor Div, 5005 E McDowell Rd, Phoenix, AZ 85008. Phone (602) 244-6900 or (602) 438-3500.
From others: Tektronix, GenRad/Futuredata, and Hewlett-Packard development systems support the 6800. Micro Industries (Westerville, OH) says it has acquired an exclusive license to Motorola Micromodule 8-bit boards.

From Motorola: Software can be obtained free for downloading over phone lines by calling (512) 440-FREE. The basic assemblers and other tools are for the IBM PC.
Two versions of Basic are available for the 6809: Basic-M and Basic09. The latter is designed to be fast and to permit structured programming. A Pascal compiler diskette is available.

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- ☐ *runs on IBM PC/XT/AT or compatibles*
- ☐ *full-screen 'windowing' text editor*
- ☐ *high-speed relocatable macro assembler*
- ☐ *linker/locator software*
- ☐ *fully symbolic software for customer assembler and emulator symbols*
- ☐ *group file/function-key control for single-keystroke sequences*
- ☐ *file transfer option for Intel/Hitachi/Motorola MDS's preserves existing program investment*
- ☐ *compatible with PL/M-51*
- ☐ *MMU and DMA support for 64180 family*
- ☐ *separate program & data memory for 8051 and 80515 families*
- ☐ *compatible with 8051 or 6301 C compilers*
- ☐ *real-time logic state trace with symbolic software*
- ☐ *program timer/ breakpoint timer*
- ☐ *built-in EPROM programmer for all common NMOS and CMOS devices*
- ☐ *EPROM programming support for 8751 and 63701 'ZTAT' microcontrollers*
- ☐ *MDSs available for:*
  - *6301X/6301Y/6303R*
  - *8031/8051*
  - *8032/8052*
  - *8044/8344*
  - *64180*
  - *80515/80535*
- ☐ *comes with power supply, cables and carrying case*

Software Development

Software Development Systems are supplied as standard with our Microprocessor Development Systems, or may be purchased separately. Each SDS consists of a full-screen text editor, high-speed relocatable macroassembler, linker/ locator, and file conversion utilities.

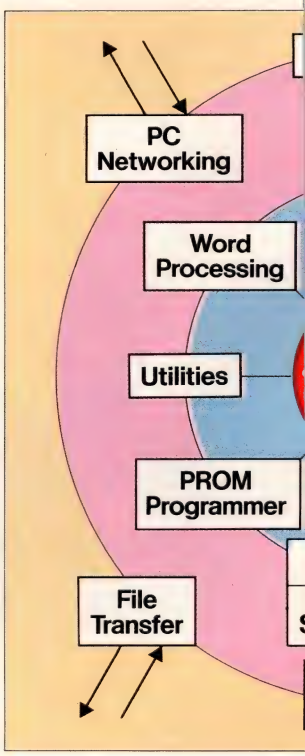
The systems available are:

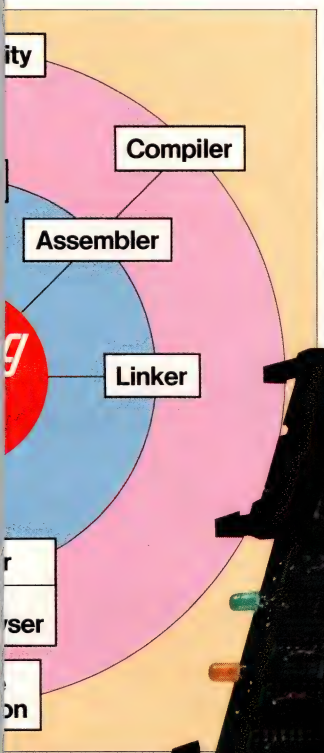
- ☐ *SDS8051 (Intel 8051/ 8052/8044)*
- ☐ *SDS6301 (Hitachi 6301/6801)*
- ☐ *SDS80515 (Siemens 80515/80535)*
- ☐ *SDS64180 (Hitachi 64180)*

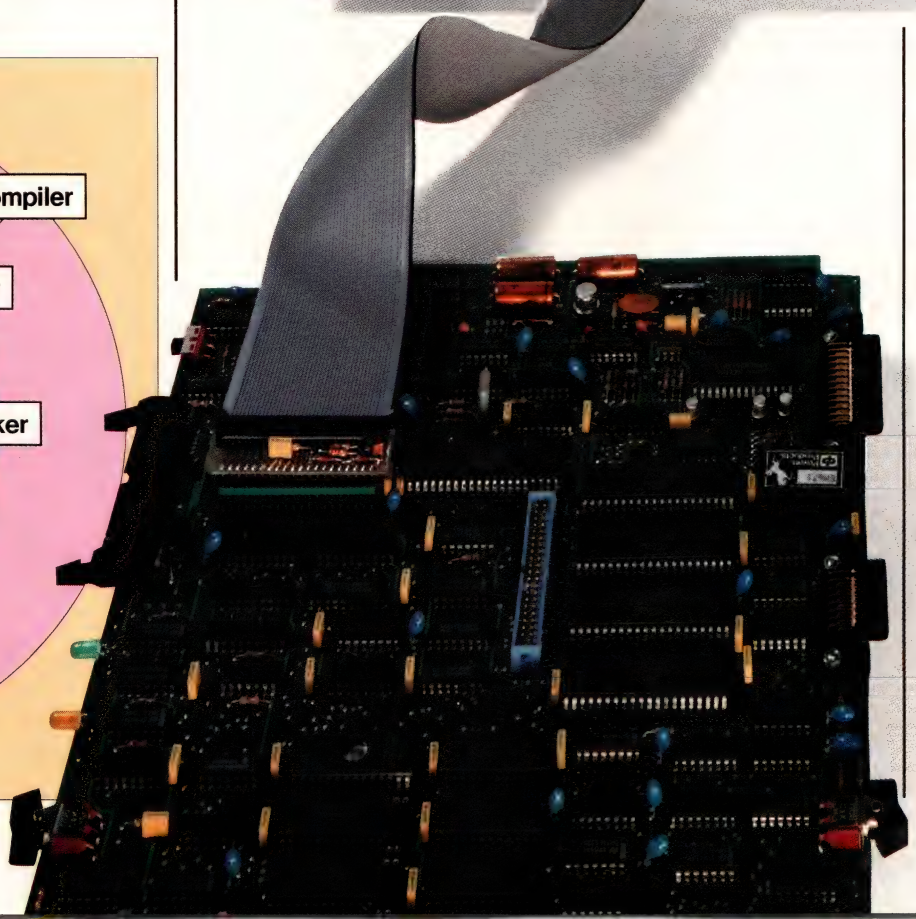
Ashling Systems Architecture contains all the hardware and software tools for microprocessor development within an integrated PC-based environment. Our commitment to compatibility enhances your systems options.

Ashling Microsystems is dedicated to making development systems an tools for microprocessor and microcontrollers based around industry-standard personal computers and software. This allows us to provide highly integrated and universal MDS's with both ease of use and an outstanding price: performance ratio.

Contact your local distributor or Ashling for further information.







Ashling

The Development Systems Company

Ashling Microsystems Limited, *Enterprise House, Plassey Technological Park, Limerick, Ireland. Telephone: (International) +353 61 334466. Telex: 70357 ASHL EI. Fax: +353 61 334477.*

Distributors: ***Austria*** *ing. e. steiner: (0222) 8274740;* ***Belgium*** *Air-Parts Electronics: (02) 2416460;* ***France*** *A2M: (1) 39.54.91.13, or Tekelec-Airtronic: (1) 45.34.75.35;* ***Israel*** *R.D.T. Electronics Engineering. (03) 483211;* ***Italy*** *Elettronucleonica: (02) 4982451;* ***Netherlands*** *Air-Parts International: (01720) 43221;* ***Norway*** *Teleinstrument: (02) 789460;* ***Spain*** *Instrumatic Espanola: (91) 455 8112;* ***Sweden*** *Aktiv Elektronik: (08) 7390045;* ***Switzerland*** *Instrumatic (01) 7231410;* ***UK*** *Instrumatic: (06284) 76741;* ***W Germany*** *Instrumatic Electronic Systems: (089) 858020.*

CIRCLE NO 60

650X, 65C0X

AVAILABILITY: Now for NMOS and CMOS, 4 to 6 MHz.
COST: Last year, the prices for both NMOS and CMOS were said to have dropped to less than $1. However "legitimate" US price said to be $2 to $3 for NMOS and twice that for CMOS
SECOND SOURCE: Rockwell, GTE, NCR, WDC, Ricoh (Japan), and UMC (Taiwan). WDC (Western Design Center) has been creator of some of the CMOS designs, which it has licensed to some of the other suppliers and which is one explanation why second sources have proliferated
CORE: NCR has pioneered the use of 6502 as semicustom core. Many of above sources also specify it as part of their cell libraries, as does SMC (Hauppauge, NY)

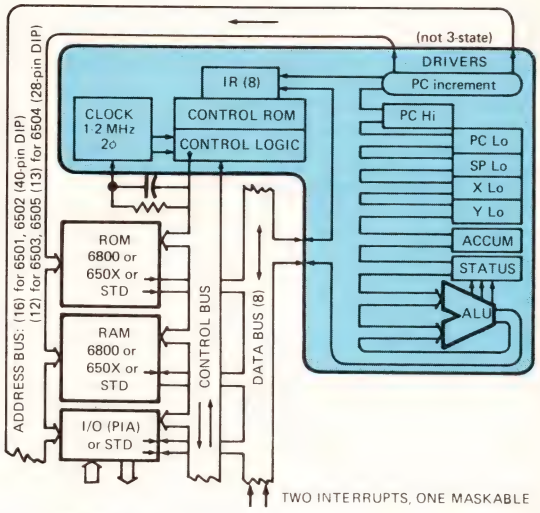
Description: Supplier's goal was to achieve as much PDP-11-style addressing capability as would fit in an economical 138×151-mil chip. Because of the μP's short 8-bit index registers, it is optimally suited only to applications requiring access of smaller blocks of memory (although it benchmarks ahead of most other 8-bit μPs with respect to its speed of execution of high-level languages such as Basic and Pascal). New CMOS parts also have small economical die (70×52 mil). See 6500/1 and 6500/21 for 1-chip versions and 65SC816/802 for 16-bit-internal version.

Commodore
1200 Wilson Dr
Westchester, PA 19380
Phone (215) 431-9100

Note: Originator **Commodore,** formerly MOS Technology, no longer sells outside to merchant market. Contact second sources

Status: Volume has dropped (1,850,000 units in '85, according to Dataquest) because of cutbacks in game and home-computer markets. CMOS share continues to rise, partially because some large volume users are dropping CMOS parts into NMOS sockets, as the CMOS price differential is so small. Because of small CPU die size, a number of the semicustom houses are using this as core processor for their cell libraries, and WDC is encouraging this through low up-front cost licensing of its CMOS designs. WDC65SC802 (see separate entry) is plug-in, software-compatible replacement for 6502/65C02, which can be software switched into enhanced 16-bit internal mode.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes on CMOS versions:
1. CMOS 65CXX family members are slight enhancements of NMOS counterparts and can serve as plug-in replacements.
2. Among hardware enhancements are new 4-phase clock that gives decreased memory access time and a memory-lock (ML) output and bus-enable (BE) input that simplify multiprocessor designs. Also RDY in write as well as read and 3-state buses.
3. Among the software enhancements are the treating of all unused op codes as NOPs and removing the page-boundary restrictions on JMP indirect.
4. Decimal mode is automatically set Off upon reset or interrupt, and the N, V, and Z flags are made active during decimal mode.
5. A BRK followed by interrupt is executed.
6. See instruction set for comments on new instructions.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logical. Decimal mode via control bit in status register. Can operate on locations in memory space (which can be either RAM or I/O ports). CMOS parts have bit manipulation
II—DATA-MOVEMENT INSTRUCTIONS
True indexed addressing, though index offset limited to eight bits in two CPU registers—X and Y. Short-form addressing to zero page. Has two sophisticated indirect-indexed and indexed-indirect instructions for handling tables. CMOS parts have indexed absolute indirect and zero-page indirect
III—PROGRAM-MANIPULATION INSTR
Conditional branches with signed relative addresses. Nonmaskable and/or maskable interrupt, depending on model. CMOS parts have branches on bit test
Stack pointer for implementing 256-byte LIFO in external RAM
IV—PROGRAM-STATUS-MANIP INSTR
Push and pull status register from memory stack. Set and clear carry, decimal mode, and interrupt bits. (6502 and 6512 have external input to one status bit, useful for handshaking with peripherals)
V—POWER-SAVING INSTRUCTIONS
Wait and Stop on 65C02 stop processor and disconnect clock, respectively, to lower power consumption

Specification summary: Common-memory architecture with instructions, data, and I/O in same 64k-byte space; 57 instructions (68 for CMOS) execute in 3 μsec typ at 1 MHz, 1.5 μsec typ at 2 MHz. Many instructions provide choice of 13 PDP-11-type addressing modes (15 for CMOS). Advanced indexed-indirect addressing mode. NMOS and CMOS silicon-gate, depletion-mode circuitry requires one 5V, 250-mV supply. Some CMOS parts can run at 4-MHz clock (250 nsec/cycle). CMOS parts require 4 mA/MHz for operating and 10 μW standby (0 Hz).

HARDWARE — SUPPORT — SOFTWARE

From Rockwell: LCE low-cost emulator ($1250) that will optionally interface to Intel ISIS-II or IBM PC host.
From Western Design Center: Tool Box Design System ($5000) to run with Apple host. Includes pod for in-circuit emulation.
From GTE: GEM-I in-circuit-emulator package ($3750) capable of interfacing with a variety of host computers including ISIS development system and Apple. Functions as a stand-alone assembler and disassembler using a dumb terminal. Evaluation board for 65SC150 ($499) that functions as in-circuit system when coupled with GEM-I.
From NCR: Hardware emulator interfaces to Apple IIe through RS-232C. Allows complete in-circuit software debug.
From Dynatem (Irvine, CA): AIM-65 single-board computer and RM industrial modules.

From Rockwell: Cross software for Intel ISIS-II, and personal development system ($250). Support (in firmware) for assembly ($35), monitor ($65), Basic ($65), PL/65 ($85), Forth ($65), Pascal-"instant" ($100), math package ($35), and disk operating system ($50).
From Western Design Center: Emulation and test software is part of Tool Box.
From GTE: 65SC00 macroassembler for Apple Computer ($100), assembler for Intel ISIS ($1800), and Fortran assembler ($1800).
From NCR: Monitor for use in conjunction with emulator. Supports breakpoint, change memory and registers, software trace, and real-time execution, etc.
From others: Because the 6500 is so widely used, there are innumerable sources of software at different language levels; for example, the Orca Series of macroassemblers and utilities from Byte Works (Albuquerque, NM, (505) 898-8193).

65C816/65C802

8/16-BIT CMOS

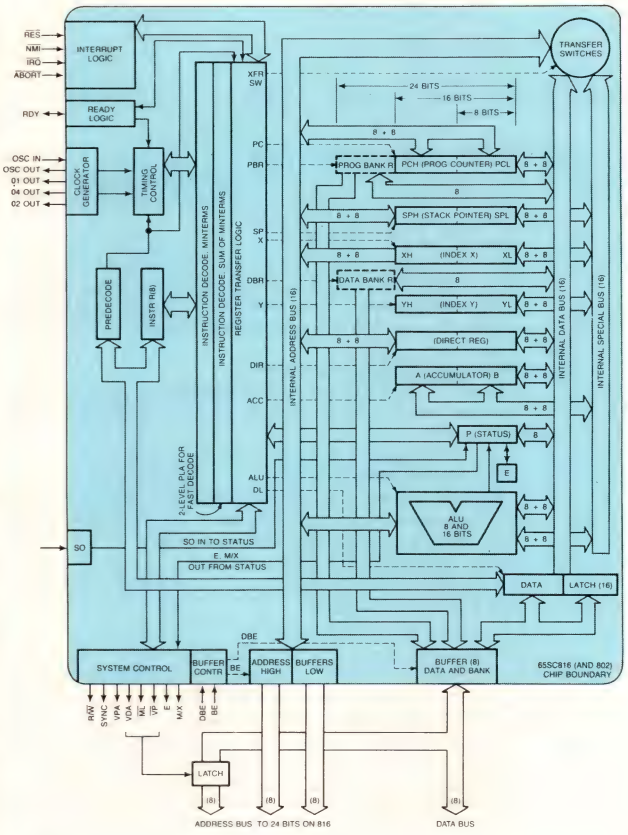
AVAILABILITY: Now for 4-MHz parts. 6-MHz by fourth quarter '86 and 8-MHz parts in '87
COST: In 100 qty, plastic, $20 for 816 and 802
SECOND SOURCE: GTE, VTI, Hyundai, and Ricoh (note that WDC follows a policy of low up-front cost licensing that may explain proliferation of second sources)

Western Design Center Inc
2166 E Brown Rd
Mesa, AZ 85203
Phone (602) 962-4545

Description: CMOS 8/16-bit μPs featuring software compatibility with 8-bit 6502 (both original NMOS 6502 and enhanced CMOS 65C02). The 802 is pin-for-pin compatible with the 6502, so it can be plugged into existing sockets. The 816 has a different pinout but expands the addressing range of the 6502 from 64k to 16M bytes. Additional hardware enhancements on the 816 allow it to be used for multiprocessor systems and in systems that have data and program caches. (Not the same as Synertek's aborted 6516 "pseudo-16." See EDN's 1979 μP/μC Directory.)

Status: Apple's use of the 65C816 in the IIGS upgrade of the widely used Apple computer boosts the credibility of this μP. It gives a firm basis for hardware availability and implies that there will be both an operating system and software to take advantage of enhancements. The next question is whether the IIGS will become as successful as the original 6502-based Apples and whether third-party software houses will write for the 65C816.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Compare diagram with previous 6502/65SC02 (elsewhere in directory) to see nature of architectural enhancements. The 8-bit registers have been widened to 16 bits and the 16-bit registers widened to 24 bits.
2. The new control-bus outputs on the 816 facilitate multiprocessing, caching, and virtual memory.
3. The new control-bus inputs on the 816 allow you to abort instructions for virtual memory and to control bus access.
4. Apple is said to have had to resort to special semicustom chips to allow the Apple IIGS to operate efficiently and at full system-level speed.

I—DATA-MANIPULATION INSTRUCTIONS
The 6502/65C02 instructions with 16-bit versions of add, subtract, BCD, and logicals. No multiply, but future 65C832 version will have provisions for floating point on chip
II—DATA-MOVEMENT INSTRUCTIONS
6502/65C02 instructions, but with choice of 8- or 16-bit indexing and 8- or 16-bit data widths
On 816, addressing can span 16M bytes with aid of paging through new register extensions. New block-move (forward or backward) instructions. Increased stack-pointer addressing modes, including stack relative, indirect, and indexed
III—PROGRAM-MANIPULATION INSTR
Wait for interrupt, stop clock (restart via interrupt). (Abort instruction on 816 via pin input acts like interrupt and directs program to perform memory repair and retry)
IV—PROGRAM-STATUS-MANIP INSTR
Additional bits in status register allow software selection of 8- or 16-bit modes for indexing and data. Also, new E bit associated with status register (but not handled as part of it) provides software choice of emulation or native mode
Notes:
1. Upon reset, 802 and 816 are in 6502 emulation mode. To go to native (enhanced) mode, the E bit must be reset to 0 via an exchange with previously reset carry bit in status register.
2. Full-sized 16-bit registers reported to facilitate high-level-language compiler writing as compared with 6502. The 16-bit index registers and the 16-bit stack pointer with no page-1 confinement help. Further, the more sophisticated stack-pointer addressing modes directly serve needs of compiler writers.
3. Possible tendency of new native (enhanced) mode coding to become trickier than 6502, because of tightly packed architecture (all 256 op codes used) and opportunity to flip back and forth dynamically between modes and between register and data widths.

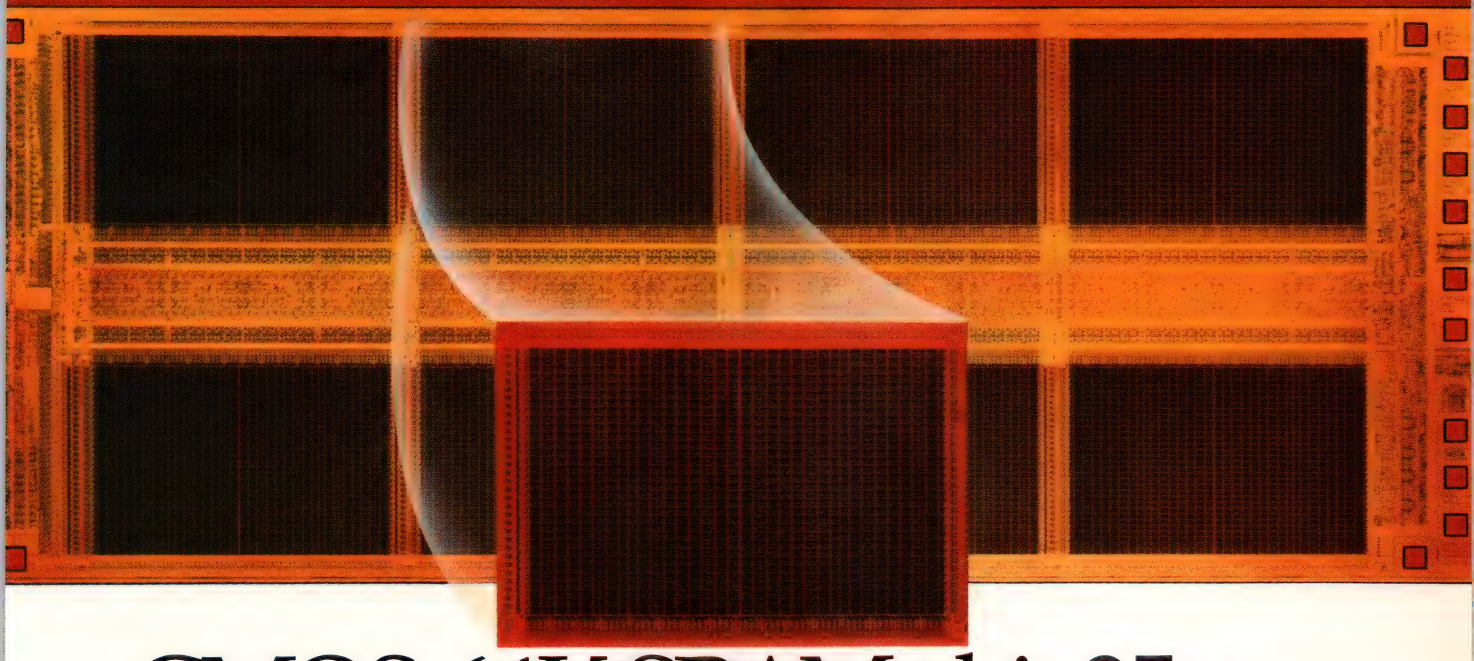
Specification summary: Enhanced 6502 with 16-bit internal data option and 24-bit addressing option, software selectable. Data I/O off chip remains 8 bits, however. The 802 version is hardware compatible with 6502 (or 65SC02) and can be plug-in replacement. It will reset into 6502 emulation mode but can be software switched into varying degrees of 16-bit operation. The 816 version is almost identical internally to 802, but it has different pinouts because it brings the additional bits for 24-bit address space out of the multiplexed 8-bit data bus, and it has special control lines to facilitate virtual memory, coprocessors, and data and program caching. Performance is mostly identical to 6502 of same clock speed, except that extended addressing and data modes take additional cycles. Clock now to 4 MHz, but 6 to 8 MHz is expected to be available. Fabricated in 3- and 2.4-μm CMOS (1.5 μm by this year) and specs 5-mA/MHz power consumption with 1 μA standby.

HARDWARE — SUPPORT — SOFTWARE

From Western Design Center: The Tool Box in-system emulator ($1495) for real-time emulation of 802/816 parts using Apple μC.
From GTE: Prototyping board for 816 that may be released as product. Includes gate-array memory mapper.
From Microtek Lab Inc (Gardena, CA): In-circuit emulation.
From Dynatem (Irvine, CA): RMX-1600 board with 65C816. For RM-65 bus industrial systems. Unused middle row of DIN connectors used for extending address bus to 24 bits.
From Apple (Cupertino, CA): The new Apple IIGS personal computer ($999) for use as development platform because it uses 65C816.

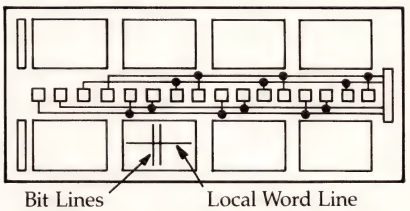
From ByteWorks (Albuquerque, NM, (505) 898-8183) and distributed by Quality Software (Chatsworth, CA): The Orca/M ($79.95) cross-assembly and utility package that runs on Apple μC under ProDOS. Comes on four disks and has 400-pg manual. Supports 816's 24-bit addressing.
Pascal compiler in progress.
From Apple (Cupertino, CA): Software for Apple IIGS (as well as that supplied by third-party sources).

MOTOROLA



CMOS 64K SRAMs hit 25 ns.

New Static family achieves faster speed and lower power with innovative architecture, proven process.



Unique design features provide both lower power and 25 ns speed for a new family of 64K and 16K CMOS Static RAMs available now from Motorola.

The MCM6287 is a 64K×1, the MCM6288 is a 16K×4 and the MCM6268 is organized in 4K×4.

Rows vs. columns.

A reversal of the traditional Row-Column architecture runs the bit lines across the short dimension of arrays separated into 8K blocks.

The resultant bit lines are one-fourth the traditional length, significantly reducing resistance and capacitance for a tremendous speed increase. And, only one-eighth of the chip is powered up at a time, so power consumption is held to the absolute minimum.

Patented power down boosts speed.

Another speed boost is achieved by a patented circuit which allows power down without any speed penalty. The result is that access from Chip Select is the same as from Address Valid—25 ns.

Proven, volume technology.

Although these SRAMs are among the first to utilize double metal, they are fabricated in standard double poly, 1.5 micron CMOS. So it's a case of SRAM performance achieved through innovative design, produced in a proven process that's years along the experience curve.

Motorola's newest fast Static RAMs

Device	Organization	Speed (ns)	I_{CCA} (mA)	Production
MCM6287	64K×1	25,35	70,60	Now
MCM6288	16K×4	25,35	90,70	Now
MCM6268	4K×4	25,35	90,70	Now
MCM6164	8K×8	45,55	90,80	Now
MCM6168	4K×4	45,55	80	Now
MCM2018	2K×8	35,45	150	Now

These fast CMOS Motorola SRAMs serve all the 64K and 16K sockets included by 64K×1, 16K×4, 8K×8, 2K×8 and 4K×4. They are available in volume with short lead times from your Motorola sales office or distributor.

For technical information, send the completed coupon or write to your Motorola sales office.

We're on your design-in team.

MOTOROLA INC.
European Semiconductor Group

Write To: Motorola Ltd., European Literature Centre, 88 Tanners Drive
Blakelands, Milton Keynes MK14-5BP, United Kingdom

Please send me more Motorola fast Static RAM information.

302EDN112786

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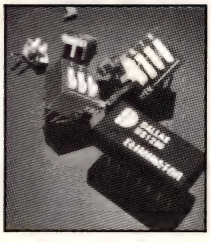
NOTHIN' TO IT



"I depend on a computer to manage the farm. But the last circuit board I got for my PC was so confusing, with those DIP switches and all, I had to call a fella clear from town to figure it out. Cost me a pretty penny, too. Well, the next circuit board I bought had a little part called an "Eliminator" on it. I installed it myself and it started right up! I know a lot more about farming than computering. Dallas Semiconductor must have had folks like me in mind when they made the Eliminator."

Dallas Semiconductor's DIP Switch responds to software control. The low cost DS1290 Eliminator gives system designers the ability to individualize their products for a wide range of customers. Features such as memory size, printer format and modem baud rate can be selected without the burden of accessing mechanical DIP switches.

The end customer can make the switch settings through a keyboard Alternatively, a software program can make the settings without any operator intervention. That's a welcome change from hard-to-set mechanical DIP switches or jumper wires. Too often, customers who are not technically inclined must go to the expense of calling a service representative. Also, the Eliminator is nonvolatile; it won't forget settings when power fails. The CMOS DS1290, in a 14-pin package replaces the equivalent of an eight-station manual DIP switch and pull-up resistors. A larger version, the DS1292 in a 22-pin 3/10" wide package, replaces 16 stations. Any number of Eliminators can communicate with the system bus through an adaptor circuit called the DS1206 Phantom Interface. This interface listens for switch-related signals without interfering with system operation. Call us for more information.

DALLAS SEMICONDUCTOR

4350 BELTWOOD PARKWAY ♦ DALLAS, TX 75244 ♦ 214-450-0400

INTERNATIONAL DISTRIBUTORS: ALFATRON, Australia, BETEA, Belgium, REA, France, TEKELEC, France, CET, Hong Kong, MALHAR, India, STG, Israel, COMPREL, Italy, TEKELEC, Italy, SYSTEMS MARKETING, Japan, DYNAMAR, Malaysia, DIGICONTROLE, Portugal, INTEGRERAD ELEKTRONIK, Scandinavia, PROMILECT, South Africa, VINE OVERSEAS, South Korea, COMELTA, Spain, KONTRON, Switzerland, LANDCOL, Taiwan, JOSEPH ELECTRONICS, United Kingdom, ATLANTIK ELEKTRONIK, W. Germany

8096 FAMILY

16-BIT NMOS AND CMOS

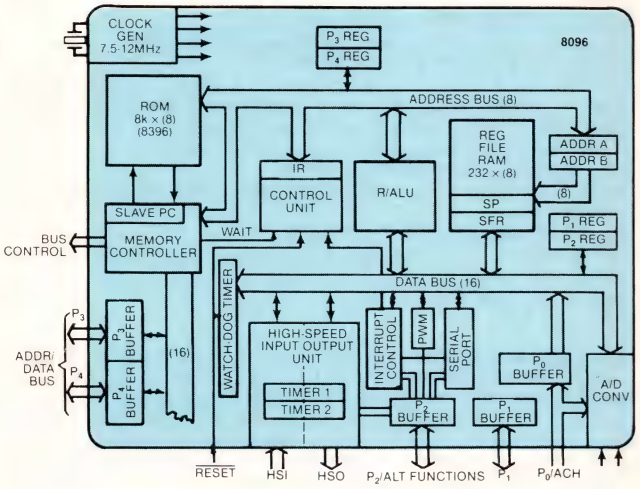
AVAILABILITY: NMOS 809XAH in production (see note 4). 809XBH in production first quarter 87. EPROM versions of 809XBH being sampled. CMOS 80C96 by end of '87
COST: Less than $10 in 10k qty
SECOND SOURCE: Signetics/Philips (fourth quarter for AH samples, second quarter '87 for production; second quarter '87 for BH samples)

Description: Highly integrated 16-bit microcontroller combining 16-bit CPU with extensive I/O handling. On-chip memory includes 8k bytes of ROM and 232 bytes of register-file RAM. I/O capabilities include an 8-channel, 10-bit ADC, full-duplex UART, 8-level priority interrupt, pulse-width-modulated output, high-speed pulsed I/O, four 16-bit software timers, five 8-bit I/O ports, and a watchdog timer.

Intel Corp
Embedded Controller Operation Marketing
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051

Status: According to Dataquest figures had top share of 16-bit-microcontroller market in '85. But because volumes still small in that market (only 145k units for 8096), it's too early to tell whether this will be another case of Intel dominance. A problem will be that Intel is going to be late with a CMOS version, now saying that it won't be available until end of next year. Meanwhile, Thomson says it is readying its CMOS version of the 68200, and National says its CMOS-from-the-start 16040 is in production.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Four high-speed trigger inputs record times at which external events occur. Storage in 8-deep FIFO.
2. Six high-speed pulse outputs can trigger external events at preset times. Commands are stored in 8-deep content-addressable memory. Output section can concurrently run as many as four software timers simultaneously.
3. 16-bit watchdog timer allows recovery from hardware or software error.
4. The 8096 family consists of three parts—8095 through 8097—that come with or without A/D converter and onboard ROM, and with either 48 I/O lines (68-pin package) or 32 I/O lines (48-pin package).
5. 8k-byte EPROM version (sampling now with production first quarter '87) will have onboard programming capability and read/write selectivity.

I—DATA-MANIPULATION INSTRUCTIONS
8- and 16-bit signed and unsigned arithmetic in binary, including multiply and divide
Logicals
Bit, byte, word, and double-word operations
II—DATA-MOVEMENT INSTRUCTIONS
Addressing modes include Direct, Immediate, Indirect, Indexed, and Indirect with Autoincrement
Load and store, push and pop
III—PROGRAM-MANIPULATION INSTR
Has calls, jumps and returns
Conditional jumps upon Boolean functions of flags within ±128 bytes of instruction
Iteration control of loops
IV—PROGRAM-STATUS-MANIP INSTR
Zero, sign, overflow, carry, overflow trap, interrupt enable, sticky bit (records previous value of carry during right shifts)
Can set and clear some bits

Specification summary: 16-bit μC with split-memory (von Neumann) architecture and 8k-byte ROM and 232 bytes of register-file RAM on chip. External memory expandable to 64k bytes, with data bus dynamically programmable as 8- or 16-bits. Register-to-register architecture with ALU operating directly on register file. Has 8-channel, 10-bit A/D converter, four 16-bit software timers, PWM output, five 8-bit I/O ports, full-duplex serial port, and high-speed pulse I/O ports. At 12-MHz clock, 16-bit addition takes 1 μsec, 16×16 multiply or 32/16 divide takes 6.5 μsec. Average instruction-execution time equals 1 to 2 μsec. HMOS III ion-implanted, depletion-load, silicon-gate circuitry requires 5V and 0.8W. In 48-pin DIP, 68-pin PLCC, or 68-pin grid array.
809XBH enhancements over 809XAH include 8- or 16-bit system bus and the addition of sample-and-hold circuitry for A/D.

HARDWARE — SUPPORT — SOFTWARE

From Intel: Low-cost development kit ($2695) includes iSBE-96 emulator board and ASM-96 macroassembler and runs on IBM PC host as well as Intellec Series III and IV. Real-time emulation to 12 MHz. VLSICE-96P advanced emulator provides real-time emulation up to 10 MHz and is hosted on IBM PC as well as Intellec Series III and IV.
Programming support for EPROM versions supplied through Intel's line of Universal PROM programmers.

From Intel: Macroassembler (ASM-96) and software simulator available along with PL/M-96 and C-96 compilers. Each software package includes relocation/linkage utility, library creation utility, and FPAL-96, a 32-bit floating-point utility. Software runs on IBM PC and Intellec Series III/IV and is priced at $750 for single-user license.
Cybernetic Micro Systems (San Gregorio, CA) has graphic programming and simulation aids that run on IBM PC ($295 and $995).

HPC 16040

16-BIT CMOS

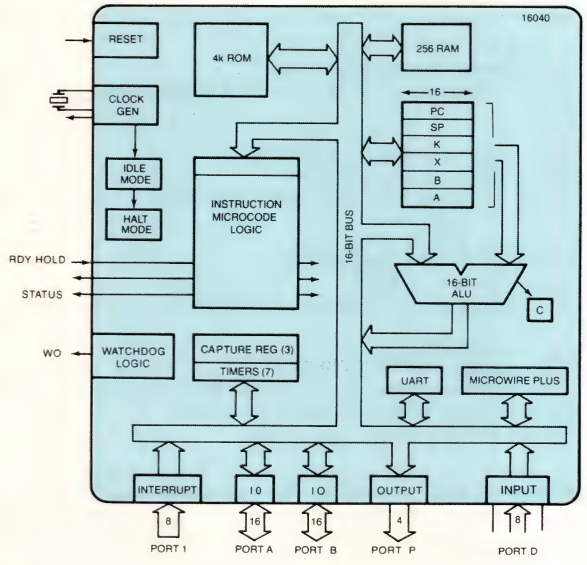
AVAILABILITY: Now for 17-MHz parts
COST: Less than $10 in volume
SECOND SOURCE: To be announced
CORE: Will be standard cell in supplier's semicustom library

Description: 16-bit CMOS microcontroller family with basic version having 4k bytes of onboard ROM, 256 bytes of RAM, extensive I/O, and onboard peripherals. First parts have 16.8-MHz clock with 240-nsec register instruction execution; future parts are projected to reach 20 MHz with shrink.

National Semiconductor Corp
Microcontroller Marketing
M/S 16-174
2900 Semiconductor Dr
Santa Clara, CA 95051
Phone (408) 721-5882

Status: Supplier says its HPC 16040 is the first member of what is to be a growing family of industrial controllers. Supplier hopes it will have high enough performance to compete with many other similar 16-bit controllers such as the Intel 8096, Mostek 68200, and NEC 783XX. Supplier hopes it will have low enough cost to also compete with high-end 8-bit controllers such as the Motorola 68HC11, 8052, NEC 78XX, Zilog Super8, Hitachi 64180, and TI 7000. This family is from the same group at National that has produced the company's most successful microprocessor, the 4-bit COP family.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Family is designed around common μP core for instruction-set consistency, with various models having various assortments of on-chip peripheral functions. Onboard peripheral functions planned are A/D, gate arrays for customization, dual-port RAMs for efficient interprocessor communication (download/uploading), and EEPROMs. Also planned are HDLC, CRT , DMA, SCSI, and Ethernet controllers.
2. Microwire/Plus is used for synchronous serial data communications with supplier's Microwire peripherals (A/D, display drivers, EEPROM), COPs 4-bit μCs, 8050 8-bit μCs, and other 16040s for multiprocessing.
3. Watchdog logic monitors operations and signals upon the occurrence of any illegal activity such as infinite loops.
4. Halt and Idle modes provide additional power savings by stopping clock or disconnecting it.
5. An emulator part for 16040 and a port expansion and recreation logic (PEARL) chip will be available in first quarter '87.

I—DATA-MANIPULATION INSTRUCTIONS
8- and 16-bit arithmetic in binary, including multiply and divide with 32-bit results
Logical AND, OR, XOR, and compares
Bit manipulation of all registers and through all 64k address space.
II—DATA-MOVEMENT INSTRUCTIONS
10 addressing modes: register B indirect, register X indirect, direct, indirect, indexed, immediate, register indirect with autoincrement/decrement, register indirect with autoincrement, and skip
Instructions include load, store, push, pop, and exchange
III—PROGRAM-MANIPULATION INSTR
Calls, jumps, returns, and conditional jumps implementing high-level-type constructs
IV—PROGRAM-STATUS-MANIP INSTR
There is a carry bit and several status registers. These may be manipulated as all bits in registers space, and in 64k address space, may be set, reset, and tested

Specification summary: 16-bit CMOS μC and μP with memory-mapped architecture and 4k-byte ROM and 256-byte RAM on chip. External memory expandable to 64k bytes. The 16-bit-wide architecture includes data bus, ALU, and registers. Has eight programmable 16-bit timers, eight vectored interrupts, full-duplex UART with programmable baud rate, PWM outputs, 10 timer-synchronous outputs, three input capture registers, 52 general-purpose I/O lines. Performance at initial 16.8-MHz clock is 240 nsec for register operations and 7 μsec for 16×16 multiply and 32/16 divide. Supplier says its "microCMOS" process will provide low 20-mA power consumption. The Idle instruction is expected to reduce this to 2 mA, and the Halt instruction will drop it to 20 μA. Supply range is projected to be 3 to 5.5V. To be available in industrial (−40 to +85°C) and extended (−55 to +125°C) temperature ranges (MIL-STD-883 in first quarter '87). Packaged in 68-pin PCC, LCC and 68-pin PGA.

HARDWARE — SUPPORT — SOFTWARE

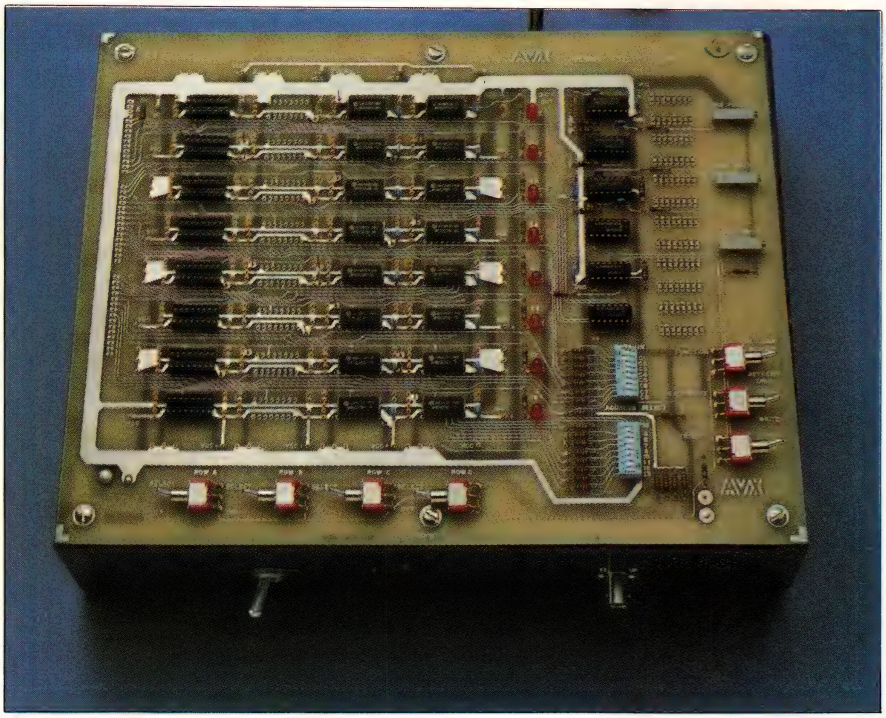
Supplier's MOLE (Microcomputer On-Line Emulator) is a low-cost ($4590) development system for the 16040 family. MOLE consists of brain board and 16040 personality board and optional software. The brain board is common to all National μCs. The personality boards tailor the system to emulate particular μCs. MOLES can be used in conjunction with various host systems like IBM PC/XT/AT, Apple II, Intellec, or VAX (UNIX/VMS).

Crossassembler and C compiler to run on IBM PC and CP/M systems. VAX (UNIX/VMS) support will be available second quarter '87. A symbolic debugger will also be available at that time. Floating-point math and general math packages are currently available.
Dial-A-Helper is a 24-hr on-line computer Bulletin board serviced by National. It provides the latest information on all National μC chips (including development systems) and also specific application support. Phone (408) 739-1162.

Decoupling IV

AVX Techfile Series

TECHNICAL INFORMATION FROM THE LEADER IN MLCs



MLC Decoupling of 256-K Dynamic RAMs

A dynamic RAM's sensitivity to decoupling-induced "soft-errors" (random loss of one or more bits of memory) increases dramatically with higher speeds, higher density, and an increased number of sense amplifiers. The new 256-K DRAM designs have large, instantaneous current demands which must be satisfied by a local current source.

That source is the decoupling capacitor directly adjacent to the RAM package. And the capacitor most often used for this application is a multilayer ceramic capacitor (MLC) because of its low series inductance, low series resistance, and high capacitance in a small size.

Test Results

Tests were conducted by AVX on a 256-K DRAM memory board to determine the noise level obtained with various values of MLC capacitors. Figure 1 compares the results obtained using 256-K DRAMs with those from similar board tests on 64-K DRAMs. As indicated, 0.33-μfd capacitors are required on the 256-K DRAM board to obtain a noise level equivalent to that obtained using 0.1-μfd capacitors on the 64-K DRAM board. Performance improvements on the 256-K DRAM

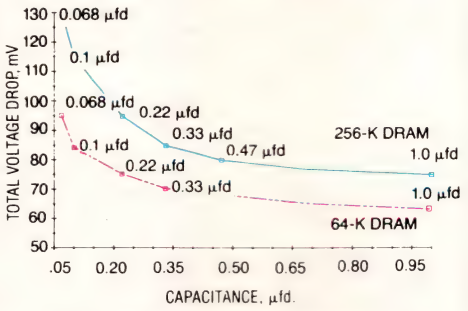


Fig. 1. Decoupling characteristics for 64-K and 256-K DRAMs with AVX MLC capacitors (including V-bump and V-droop).

test board leveled off between 0.33-μfd and 1.0-μfd, indicating that the preferred value for decoupling is about 0.33-μfd.

Figure 2 shows the scope traces obtained during refresh cycle on the 256-K DRAM test board with a 0.33-μfd AVX MLC. In all tests, the general decoupling scheme used was one MLC capacitor for each DRAM, with no board-level bulk capacitors.

Discussion

General-application ceramic formulations, such as Z5U, show considerable change in capacitance with temperature. However, this change has

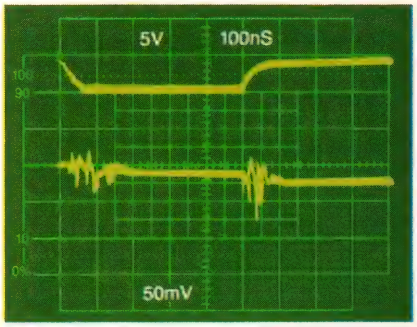


Fig. 2. Scope traces for refresh cycle on 256-K DRAM test board with 0.33-μfd AVX MLCs.

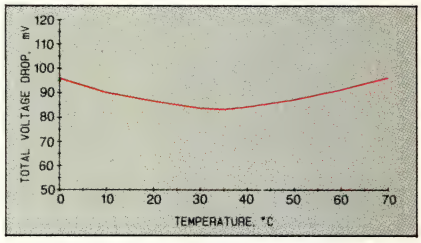


Fig. 3. Effect of temperature on 256-K DRAM decoupling with 0.33-μfd AVX MLCs (Z5U).

little affect on the total noise level for 256-K DRAM when the correct value is chosen. Thus, the 0.33-μfd value is high enough to meet the 256-K DRAM's current requirements over its full operating temperature range, as shown in Fig. 3.

For a complete technical paper describing these tests in detail, complete and return the coupon below.

AVAILABILITY: Now. Accepting code on masked-ROM devices (see Note 3)
COST: 10k qty, $12.50; expected to go under $10
SECOND SOURCE: None yet
CORE: The supplier has been using cell-library concepts in house all along

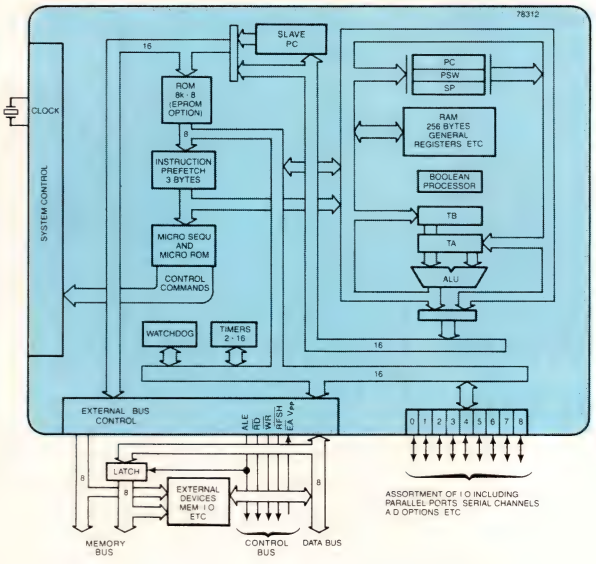
NEC Electronics Inc
(Corporate Headquarters)
401 Ellis St
Mountain View, CA 94039
Phone (415) 960-6000

NEC Electronics USA Inc
(Application Help)
1 Natick Executive Park
Natick, MA 01760
Phone (617) 655-8833

Description: Intended for high-end controller-type applications, 783XX combines a fairly fast, powerful, 16-bit ALU with many peripheral functions on one chip. Although there is some architectural resemblance to supplier's existing 7811 (see Note 3) and new V Series (especially V25), this is said to be an original design with its own unique instruction set.

Status: The supplier says the 78312 is the first in a new family that is expected to bridge the gap between 8-bit 1-chip controllers and 16-bit minicomputer-like chips. The emphasis is on economic high-speed processing of real-time events. It will compete with Intel 8089, Mostek 68200, and National 16040. Supplier says future chips in family will have same core architecture, but peripherals on chip will be aimed at specific applications, such as engine control (ie, the "ASIC" approach). Future chips will include master-slave bus interfaces, possibly similar to Intel 8041 and 87C452.

HARDWARE CHARACTERISTICS SOFTWARE



Notes:
1. The on-chip RAM contains eight banks of general-purpose registers and also eight "Macro Service Channels" that can perform DMA in response to interrupts.
2. The eight peripheral blocks at bottom of diagram are for the following functions: Two 4-bit real-time output ports; external interrupts; serial communication; two 16-bit up/down counters; two 16-bit capture registers; two PWM outputs; an 8-bit, 4-channel A/D converter; two 16-bit timers; and six 8-bit ports.
3. NEC's "parent" family, the 78XX, is still going strong. Dataquest showed 11½ million units shipped in '85, or 7% of the 8-bit-μC market. The 7811 is the most popular member of that family and will now be offered in CMOS as well as NMOS.

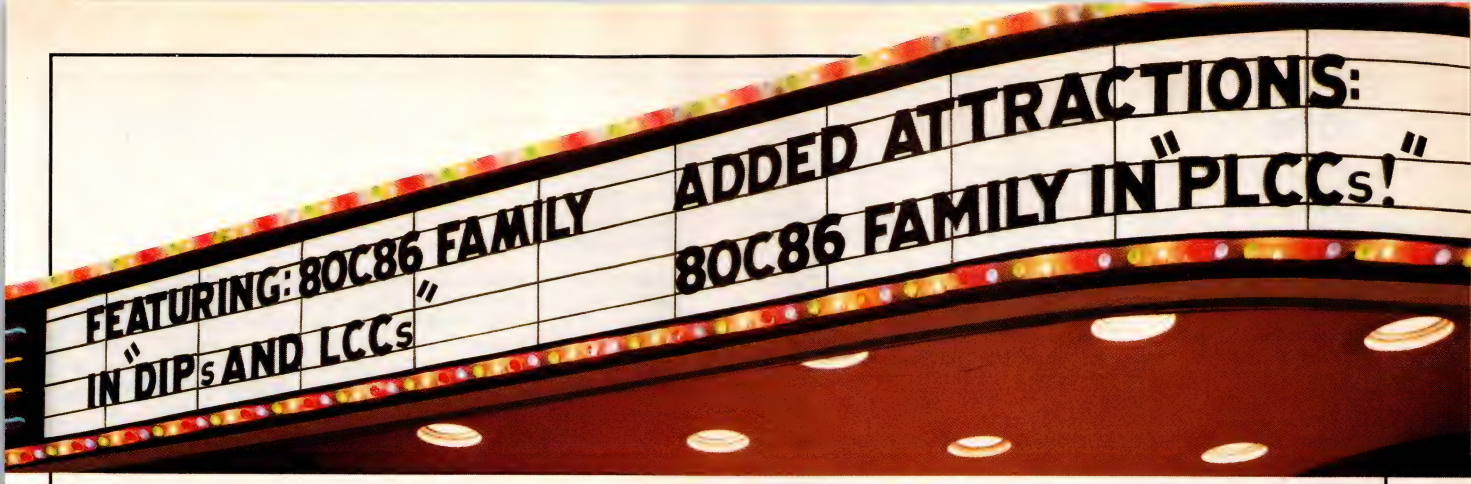
I—DATA-MANIPULATION INSTRUCTIONS
Most operations 8 and 16 bit, including adds and subtracts, shifts and rotates, decimal adjust, and increment and decrement
Multiply 8×8 in 3.0 μsec and 16×16 in 3.167 μsec
Divide 16/8 in 3.0 μsec and 32/16 in 8.333 μsec
II—DATA-MOVEMENT INSTRUCTIONS
Addressing modes include immediate, register-register, indirect (including base and base-index), and direct (including direct-indexed). The direct addressing of internal RAM can accommodate 8 or 16 bits. (Though external data is restricted to 8 bits, internal RAM can be addressed on an 8- or 16-bit basis)
Block instructions move from or exchange or compare with accumulator as much as 256 bytes of data
8- and 16-bit moves and exchanges between the accumulator or extended accumulator and general register or memory
Push and pop on or off stack
III—PROGRAM-MANIPULATION INSTR
Call, call table (1-byte call), branch, branch relative, branch register, branch register indirect, branch on condition, branch on bit, software break, return, return from interrupt
IV—PROGRQAM-STATUS-MANIP INSTR
Enable and disable interrupts, break with context switch, select register bank, increment/decrement stack pointer. Software control of standby modes, watchdog timer, and on-chip peripherals

Specification summary: A new high-performance, single-chip architecture that features eight switchable register banks to handle the demands of real-time control. This CMOS processor uses the IEEE standard mnemonics. The 12-MHz (max frequency) oscillator is divided by 2 to create a 167-nsec system clock. Minimum instruction time is 500 nsec. A 3-byte instruction prefetch queue further speeds processing. Chip can access 64k bytes of memory, including 8k bytes of on-chip ROM, 156 bytes of on-chip RAM, and a 256-byte special-function register area that communicates with on-chip and off-chip peripherals. On-chip peripherals include a 4-channel, 8-bit A/D converter, a full-duplex UART, and an extensive timer/counter system. There are two 16-bit up/down counters, two 16-bit timers, two pulse-width modulated outputs, a 16-bit time-base counter, and a free-running counter with two 16-bit capture registers. The 48 I/O lines include two 4-bit real-time output ports. There are four external interrupt lines and 11 internal interrupt sources. Eight macroservice channels can perform DMA in response to various interrupt sources. The CMOS device is packaged in 64-pin flat pack, QUIP, shrink DIP, or PLCC.

HARDWARE SUPPORT SOFTWARE

Supported on the NEC MD-086 CP/M-86-based development system. An emulation board, the IE-78CSV, will be available from NEC. Hookup of the emulation board to IBM PC and other popular computers is also supported. Additional third-party support, from Sophia Systems (Santa Clara, CA) and Orim (Redwood City, CA) is being developed.

Software to run on the MD-086 and on other CP/M-based systems includes relocatable assembler. Other third-party support (such as from Sophia) is expected to follow. C compiler from Lattice.



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80C86: 16-Bit Static CPU	82C88: Bus Controller
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82C50A: Serial Datacomm	82C84A: Clock Generator
82C52: Programmable UART	82C82/82C83H: Data Bus Latch
82C54: Timer/Counter	82C55A: Parallel I/O
82C59A: Interrupt Controller	82C86H/82C87H: Data Bus Transceivers
82C85: Static Clock Controller	

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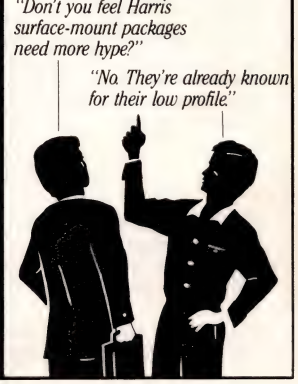


68200

16-BIT NMOS AND CMOS

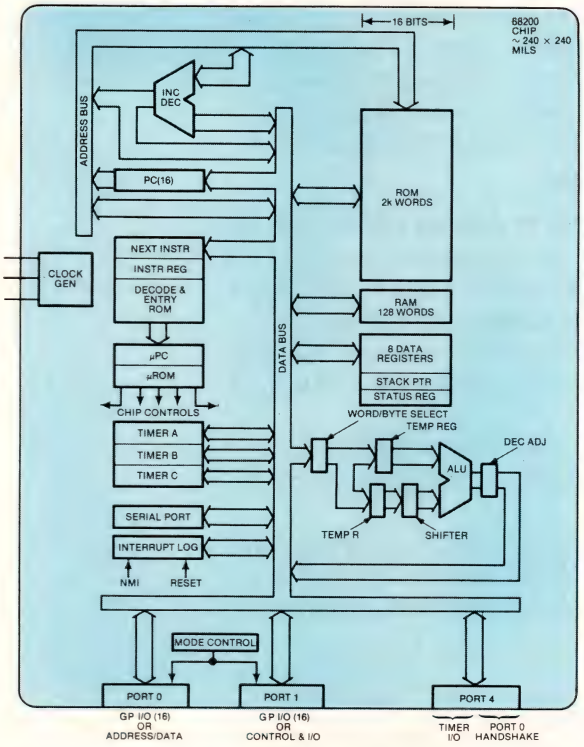
AVAILABILITY: 6-MHz NMOS in production. CMOS samples by fourth quarter '86
COST: In 10k qty, $12 for 4 MHz, $19.95 for 6 MHz. Expect NMOS price to go below $10 in volume for ROMless version. CMOS price not determined
SECOND SOURCE: None so far, but expect announcement of one (USA) by end of '86

Description: Single-chip microcontroller based on internal architecture of 68000, but not object-code compatible. Goal was to retain some similarity to 68000 but not to carry along the wasteful features for addressing very large (megabyte) memory spaces. Also has only 16-bit-wide registers vs the 32-bit-wide registers of the 68000. Represents a trend predicted by EDN towards μPs and μCs that have the 16-bit-wide words and fast 16×16=32 multiplies necessary for real-time closed-loop control. Supplier also sees it as general-purpose peripheral controller for 16-bit buses. Otherwise, more similarity to host of new high-end controllers such as the Intel 8096, Zilog Super8, and National 16040.

Thomson Components—Mostek Corp
1310 Electronic Dr
Carrollton, TX 75006
Phone (214) 466-6000

Status: This 16-bit controller nearly dissapeared when Mostek shut its doors last year. However, the large French company, Thomson, who purchased the assets of Mostek, has backed the continuation of the 68200 and says that the CMOS 68HC200 should be available shortly after this directory appears and a second source should be announced. It claims that it has retained most of the 50 designs won by Mostek.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Diagram applies to 48-pin ROM version. The 84-pin ROMless version uses its additional pins to bring out the internal bus, which is associated with the program ROM shown on diagram.
2. Port 0 is used for 16 bits of general-purpose bidirectional I/O in the single-chip mode. In the expansion mode, it is used as a multiplexed 16-bit address/data bus.
3. Port 1 may also be used for 16 bits of general-purpose bidirectional I/O in the single-chip mode. When the expanded bus mode is selected via the mode pin, eight bits of port 1 are assigned to provide one of two possible sets of control signals (UPC or GP selected by mask option) for the multiplexed address/data bus.
4. Special-function I/O pins (ie, X12, SI, TAO) may be software-selected to perform designated operations. Alternatively, special-function pins on port 1 may serve as general-purpose I/O and those on port 4 as simple inputs or outputs.

I—DATA-MANIPULATION INSTRUCTIONS
8- and 16-bit signed and unsigned arithmetic in binary, including 16×16=32 multiply and 32/16=16 divide
8- and 16-bit BCD arithmetic (byte or word)
Logicals
Bit-manipulation instructions that test the specified bit before acting on it
II—DATA-MOVEMENT INSTRUCTIONS
Data-transfer instructions include register-to-register, register-to-memory, memory-to-register, and memory-to-memory
Addressing modes include register direct, register indirect with optional postincrement, predecrement, and 16-bit displacement, pc relative, memory direct, immediate, port direct, and implied reference
III—PROGRAM-MANIPULATION INSTR
Call, conditional call, jump, conditional jump, and return
Conditional jumps allow 8- or 16-bit displacement. Conditional calls allow 12- or 16-bit displacement. Loop control (DJNZ) on byte or word count operand
Move, push, and pop instructions
Move multiple saves CPU context-interrupt service routines. Full 16-bit stack pointer register sets no fixed limit on subroutine/interrupt nesting
IV—PROGRAM-STATUS-MANIP INSTR
Status register includes carry, overflow, zero-negative, and interrupt-enable flags; four user-defined flags are also included
Bit manipulation, logical, rotate instructions can use status register as destination

Specification summary: 16-bit μC with unified-memory architecture. Register set includes eight 16-bit data-only registers (which may also be selected as 16 8-bit, data-only registers), six 16-bit address registers, 16-bit program counter, 16-bit stack pointer and status register. ROM version has 2k×16-bit masked ROM as well as the 128×16-bit RAM in memory space. Expandable to 64k bytes of external memory, with on-chip bus arbitration logic to support multiprocessor parallel-bus interfaces. A full duplex USART supports async and byte-synchronous communications; hardware also supports address recognition in multi-drop serial network protocols. Three 16-bit timers. With a 6-MHz clock, a 16×16 multiply executes in 3.5 μsec, a 32/16 divide in 3.8 μsec. Average instruction execution in 0.5, 1.0, or 1.5 μsec. Implemented on approx 240-mil² chip in 3-μm NMOS process, the 68200 is a 5V-only device. ROM version in 48-pin DIP, ROMless version in 84-pin leadless chip carrier. CMOS version is in 2-μm process (with some features down to 1.2 μm) and is projected to run at 10-MHz clock.

HARDWARE — SUPPORT — SOFTWARE

EVAL-68200 ($989) provides a low-cost evaluation board with onboard monitor, assembler/disassembler, and wire-wrapping area. INICE 68200 is an upgraded version of EVAL-68200 providing inexpensive in-circuit emulation ($1185). It can be used with IBM PC via a RS-232C port.
Note that the hardware support has been temporarily moved to France. Third-party support being explored.

Structured macro crossassembler ASM-68200 ($1990) is available now for VAX and PDP-11. Supports high-level structured statements (For, While, Repeat) as well as macro capability. A version of ASM-68200 ($415) is available for CP/M systems and for IBM PC. The lower-cost versions do not support macros or structured statements. Full C compiler ($1990) available for VAX/VMS and IBM PC.
Note that the software support has been temporarily moved to France.

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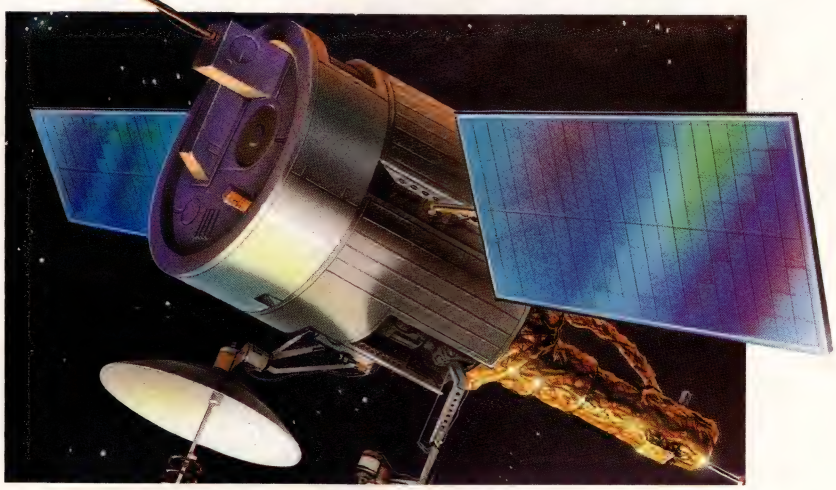
- **Selection of rad-hard CMOS RAMs:**

Organization	Part Number	Access Time (Typ.)
Synchronous		
1K x 1	HS-6508RH	160 ns
256 x 4	HS-6551RH	160 ns
4K x 1	HS-6504RH	150 ns
1K x 4	HS-6514RH	150 ns
64K Module 8K x 8 16K x 4	HS-6564RH	250 ns
Asynchronous		
16K x 1	**HS-65262RH**	**100 ns**
2K x 8*	HS-65162RH	100 ns

*Samples available 4 Qtr. 1986

For more information on the HS-65262RH RAM and the complete Harris rad-hard family of Memories, MUXes, Op Amps, μPs, Analog Switches and Gate Arrays, just ask us.

Contact: Harris/MHS Semiconductor Sales Ltd., Eskdale Road, Winnersh, Wokingham, Berks, RG11 5TR, England.



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V Series

16- AND 32-BIT CMOS

AVAILABILITY: V20 and V30 now. V40 and V50, engineering samples now with production fourth quarter '86. V60 and V70 are scheduled for fourth quarter '86 and third quarter '87 sampling, respectively
COST (All prices 100 qty:) V20 and V30, $10.60 and $12.25; V40 samples $47, $31.70, and $30.50 in PGA, PLCC, and mini-flat packages, respectively. V60 samples, $49, $34, and $33 in PGA, PLCC and miniflat
SECOND SOURCE: Zilog and Sony (both by agreement) and Sharp

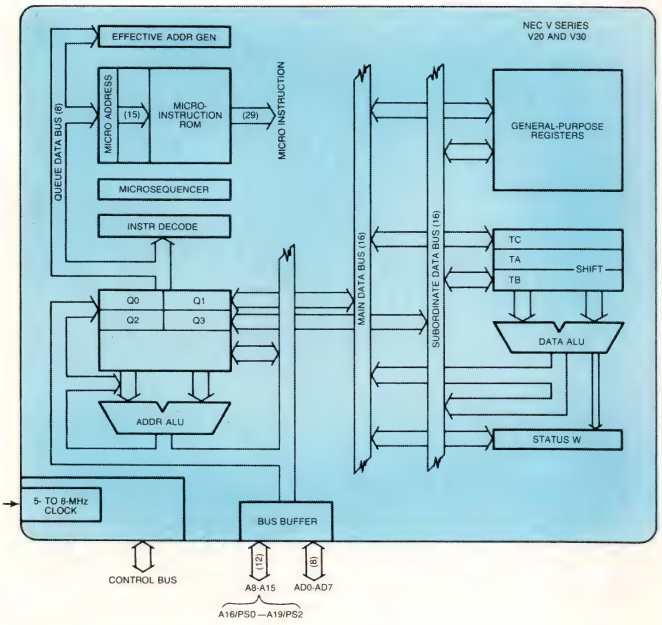
NEC Electronics Inc
Corporate Headquarters
401 Ellis St
Mountain View, CA 94039
Phone (415) 960-6000

NEC Electronics USA Inc
(Application Help)
1 Natick Executive Park
Natick, MA 01760
Phone (617) 655-8833

Description: Stretched versions of Intel 8086 family. They obtain increased performance via such enhancements as dual internal 16-bit data buses, dedicated hardware for address generation, loop counters for block transfers, 16/32-bit temporary register/shifters for fast multiplication and division, and a prefetch register. Parts contain an enhanced 8088/8066 instruction set, and all except V25 can even do 8080 instructions in an emulation mode. Note that these parts don't stop with 8086/88 enhancements but go on to enhancements of 80186/88, 80286, and 80386. V40 and V50 are extensions of V20 and V30. They are 16-bit high-integration CMOS μPs. They have the V20/V30 as core and incorporate several peripheral devices such as 4-channel DMA, interrupt controller, three 16-bit timers, wait-state generator, serial I/O, DRAM refresh controller, clock generator, and bus controller. V40 has 8-bit external data bus, and V50 has a 16-bit external data bus.
V60 and V70 are 32-bit enhancements of 16-bit family members, presumably somewhat like 80386 is enhancement of 16-bit 8086 family predecessors.

Status: This family represents a strategy used by several major Japanese suppliers—NEC and Hitachi—of basing a new μP family upon familiar, established software, in this case the 8086, and then enhancing the core software and adding features to hardware to produce parts that hopefully will outflank corresponding parts from prime US sources. Unfortunately for NEC, Intel has sued, claiming that NEC copied Intel 8086-family microcode in violation of US Copyright law. This has slowed acceptance of these parts, which may mean that the market window has passed the company by. At the time of this writing, Intel has won the first part of lawsuit—that microcode can be protected as software. According to an NEC source, there is the possibility that if NEC loses suit, NEC will abandon further efforts on V Series, perhaps cancelling the 32-bit V60 and V70 members, even though they are about to be realized in silicon. NEC might instead turn its talents towards developing a more powerful 32-bit μP for the open "UNIX box" market. (NEC has, by mask exchange, an agreement with Zilog on the Z80000.)

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Architecture similar to 8088/8086, but supplier says use of dual data buses and temporary registers results in fewer execution steps.
2. Effective address (EA) done in only two machine cycles through effective address generator.
3. Separate program counter and prefetch pointer registers result in more efficient execution of branch, call, return, and break instructions.
4. Not shown are supplier's CMOS support chips: 71051 serial control, 71054 timer/counter, 71055 parallel interface, 71059 interrupt controller, 71071 DMA, 71082/83 latch, 71084 clock generator, 71086/87 bus driver, and 71088 bus controller.

Specification summary: 16-bit CPU with dual-bus internal architecture and dedicated addressing hardware can reach 1M-byte memory locations. Multiplication and division take 6 to 8 μsec at 5-MHz clock rate. Data-block transfer rate to 625k bytes/sec at 5-MHz clock rate. Implemented in 2-μm CMOS, devices dissipate 500 mW max at 5 MHz, 50 mW in standby, and operate over −40 to +85°C. Housed in 40-pin DIP, which is pin-for-pin compatible with 8088 (V20) and 8086 (V30). The V25, V40, and V50 chips are in 1.6-μm CMOS, initially with 8-MHz clocks.

I—DATA-MANIPULATION INSTRUCTIONS
Added instructions for multiply, shift, and rotate registers by immediate value; add, subtract, and compare packed decimal strings. Also included are a large number of variations on bit manipulation, like insert or extract bit; rotate left or right on one BCD digit; test, invert, clear, or set specified bit
II—DATA-MOVEMENT INSTRUCTIONS
Various memory-addressing modes are derived from four segment registers, pointers, and index registers. In addition to MOV instructions for transferring data between CPU registers and memory, there are instructions for moving a string of data between memory and I/O port
III—PROGRAM-MANIPULATION INSTR
In addition to call, jump, and return instructions, stack operations such as push immediate data or 8 general registers onto stack, pop 8 general registers from stack; allocate/free an area for a stack frame on a procedure; and enter/exit. Also includes an instruction to check array index against designated boundary and an instruction for floating-point-processor call procedure
IV—PROGRAM-STATUS-MANIP INSTR
In addition to 8086-type status and control flags, an extra mode flag for indication of 8080 emulation mode or a native mode
Notes:
1. V Series instruction sets are supersets of 8088/8086 and can execute MS-DOS-type programs.
2. 8080 instruction-emulation mode can execute CP/M-80-type programs. Not available on V25 except as option in ROM.
3. 101 instructions, some of which are designed to support high-level languages like Pascal. On V25, added controller instructions.

PART NUMBERS (CORRESPONDING INTEL 8086 FAMILY PART)	μP SPEED (MHz)	EXTERNAL ADDR BUS	EXTERNAL DATA BUS	ON-CHIP		ON-CHIP PERIPHERALS	PACKAGE PINS	AVAILABILITY
V20 70108 (8088)	5	20 (1M)	8	0	0	NONE	40 DIP	NOW
V25 70320 (80188)	5	20 (1M)	8	0	256	2-CHAN DMA INTER CONT 2×UART 2×16 C/T	80 FLAT 84 LCC	2 QTR '86
70322				16k				
V30 70116 (8086)	5	20 (1M)	16	0	0	NONE	40 DIP	NOW
V40 70208 (80188)	8	20 (1M)	8	0	0	4-CHAN DMA INTER CONT 3×16 C/T UART CLOCK GEN	68 PGA 68 80 FLAT	1 QTR '86
V50 70216 (80186)	8	20 (1M)	16	0	0			
V60 NA (80286?)	16	32 (4G)	16	0	0	FLOAT PT MMU, CACHE	NA	4 QTR '86
V70 NA (80386?)	16	32 (4G)	32	0	0	FLOAT PT MMU, CACHE	NA	3 QTR '87

HARDWARE — SUPPORT — SOFTWARE

Hardware debugging support provided with NEC MD-086 μP development system, and stand-alone in-circuit emulation provided via IE-V20/V30 and IE-V40/V50 emulators, all said to be available
Third-party hardware available from Zax and Sophia Systems.

Software for NEC MD-086 includes relocatable assembler, and C and Pascal compilers. Compatible cross software for IBM PC/XT, Intel Intellec Series III development systems, VAX minicomputers for both VMS and UNIX operating systems. There is a real-time operating system that supplier says will feature high-speed task switching as well as functions for synchronization, communication, and prioritizing of tasks. Third-party software from Microtec Research Systems & Software, etc.

8086/8088/80186/80188

8/16-BIT, 16-BIT NMOS AND CMOS

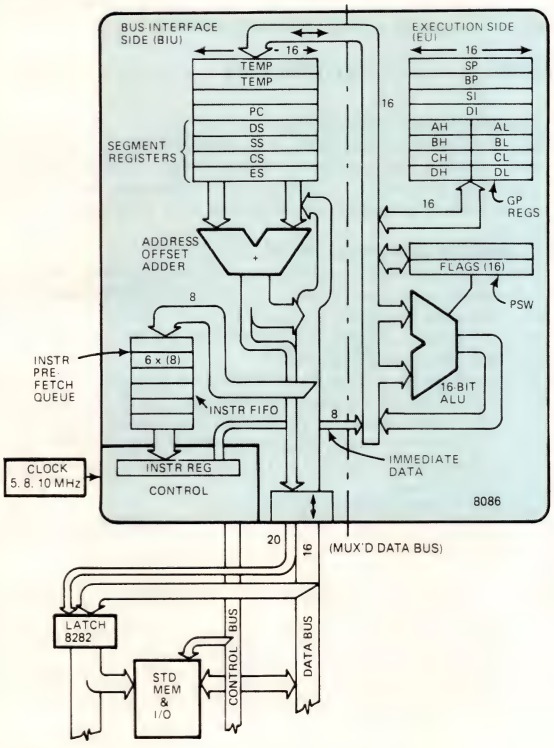
AVAILABILITY: Now for both NMOS and CMOS 8086/88. Now for 8-, 10-, and 12.5-MHz 80186. Now for 6-, 8-, and 10-MHz 80188
COST: Prices dropped drastically during recession in semiconductors, with quotes running under $10 for 8086/8088. Now said to be stabilizing
SECOND SOURCE: For 8086/8088: AMD, Harris, Matra-Harris, Fujitsu, Siemens, and Oki. For 80186/8188: AMD, Fujitsu, Siemens
CORE: Intel's newly formed ASIC groups says it will be incorporating 8066 family members in its cell library.

Description: Supplier's objective when 8086 was introduced back in '78 was to offer machine that matches performance of latest midrange minis but retains some upward compatibility with widely used 8080/85. 8088 intended as highest performance 8-bit μP. Floating-point math coprocessor (8087) available to enhance performance. The 80186 and 80188 were intended as higher-integration counterparts of 8086 and 8088. They incorporate some of the often-used support-chip functions on CPU chip, somewhat in anticipation of the current ASIC standard-cell trend (and in fact Intel plans to add 8086 family members to its ASIC cell library to give customers a chance to design their own higher-integration combinations).

Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080

Status: First of the "second-generation" 16-bit μPs, 8086/88 and its family—80186/188 and 80286—have largest share of 16-bit market (Dataquest '85 figures show 59%). Only the Motorola 68000 family comes close (Dataquest gives the 68000 25% of '85 16-bit market). Older 8086 and 8088 have been displaced by 80186 and 80188 for low-end applications and 80286 at high end. IBM's choice of 8086 family for its personal computers has solidified the 8086 family's position and given it the leading amount of third-party hardware and software support. Harris's and Oki's timely introductions of CMOS parts have helped the family penetrate even wider applications. NEC V Series (70108, 70116) had been planned as superset of 8086 family, but there is legal action between Intel and NEC.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Diagram is for initial family member, 8086 itself.
2. 8088 is downgraded version of 8086. It has only 8-bit-wide external data output bus (only 8 lower bits of address bus are multiplexed for data). Some pins functions have been changed. Prefetch queue is only four bytes (to prevent overuse of bus). Instruction execution is slower because all 16-bit fetches and writes take four extra cycles.
3. 80186/88 integrate support functions on chip to reduce system costs. Functions added are: clock generation, 2-channel DMA, interrupt controller, three 16-bit timers, memory and peripheral chip select logic, and wait-state generator. 80188 is 8-bit external data-bus version of 80186 and, like 8088 version of 8086, has shortened prefetch queue.
4. Math coprocessors implementing IEEE-754 floating-point standard are part of family. For the 8086/88 there is the 8087 coprocessor; for the 80186/188 there is the 80187 coprocessor. Prices are $100 and up.

I—DATA-MANIPULATION INSTRUCTIONS
8- and 16-bit signed and unsigned arithmetic in binary or decimal, including multiply and divide
Logicals
Bit, byte, word, and block operations
II—DATA-MOVEMENT INSTRUCTIONS
Addressing modes include Literal, Relative (to register and to segment), Register, Base Plus Index, and Base Relative Indexed
Use of segment registers: Programmer can, through software, set up four areas in memory with four segment registers—a program area, a stack area, and two data areas. These areas need not be full 64k, and they can overlap. Programmer can alter the four area locations by modifying the segment-register contents
III—PROGRAM-MANIPULATION INSTR
Has call, jump, and return instructions both inside program segments and to different segments. Intrasegment call and jump use self-relative displacement for position-independent code. Conditional jump upon Boolean functions of flags within ±128 bytes of instruction. Iteration control of loops, a repeat prefix for rapid iteration in hardware-repeated string operations
Note: Jumps can occupy varying amounts of execution time because with BIU's instruction prefetch the program counter could be ahead of itself
IV—PROGRAM-STATUS-MANIP INSTR
In addition to 8080/85 flags: overflow, interrupt enable, direction (for strings), and single-step trap flags
Notes:
1. Instructions include those of the 8080/85, but op code patterns differ.
2. Devices are object-code compatible with 8086/88 software.
3. Enhanced CPU in 80186/188 includes new instructions: PUSHA, POPA handle all registers at once; Immediate mode for PUSH and IMUL; INS and OUTS for strings; BOUND for address ranging; ENTER and LEAVE for stack-frame saving and restoration.

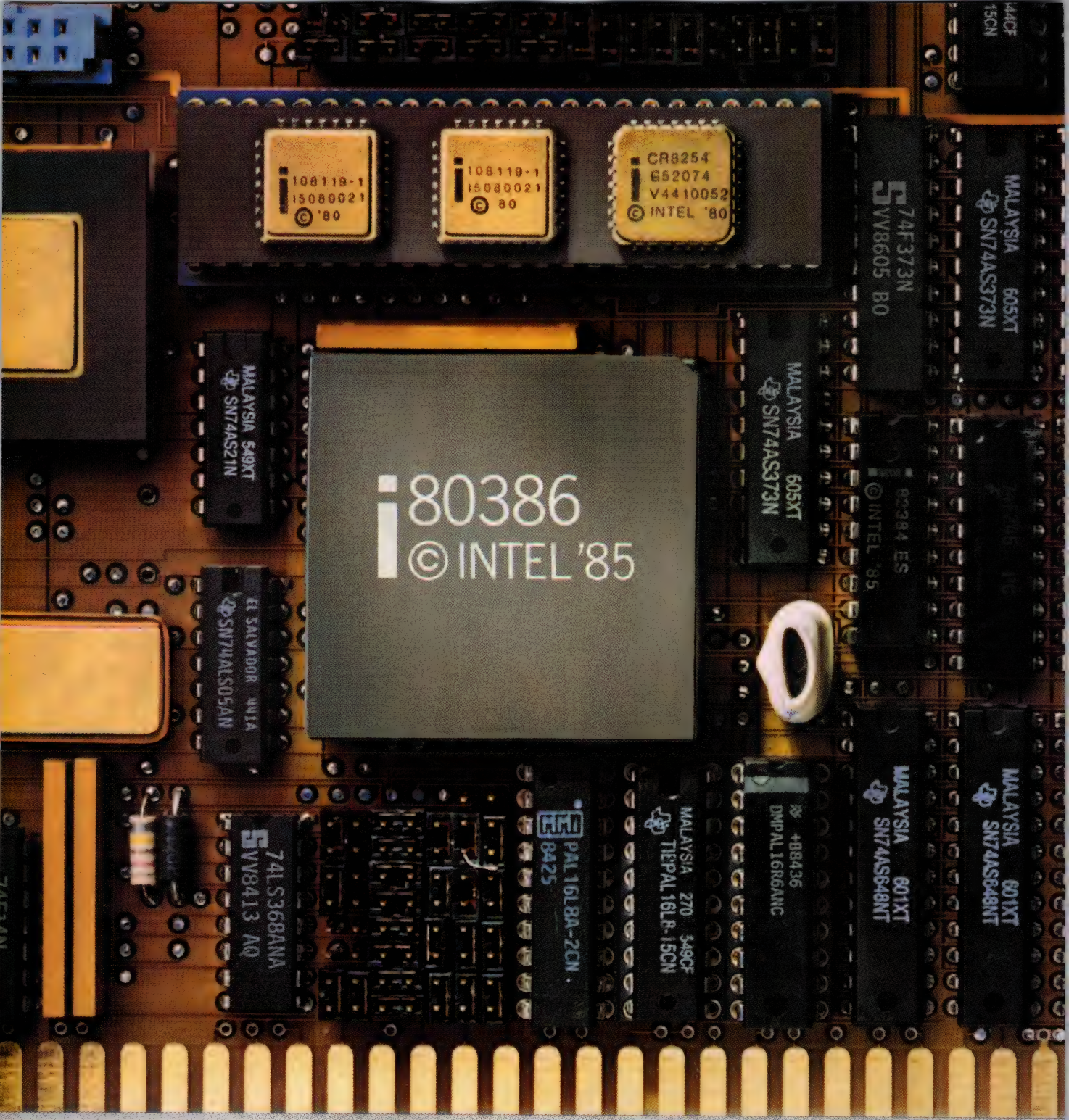
Specification summary for 8086/88: 16-bit CPU that can reach 1M byte using "segment" address-extension registers. Register-to-register operations execute at 0.6 μsec with 5-MHz clock (0.37 μsec with 8-MHz clock). HMOS ion-implanted, depletion-load, silicon-gate circuitry; requires 5V at 340 mA (substrate bias generated on chip). In 40-pin DIP, device is pin programmed to switch eight pins from minimum to maximum external system mode. Harris CMOS 8086 dissipates only 10 mA/MHz when running, and clock can be stopped for 500 μA standby.
Specification summary for 80186/188: Highly integrated μPs that combine the functions of the most common iAPX 86 system components onto one chip. Have same memory reach as 8086/88 but with improved execution times on some instructions. HMOS II ion-implanted, depletion-load, silicon-gate circuitry requires 5V at 300 mA. Housed in 68-pin JEDEC Type A ceramic leadless chip carrier and a ceramic pin grid array. A plastic leaded chip carrier is scheduled.

HARDWARE — SUPPORT — SOFTWARE

From Intel: ICE emulation system, available for IBM PC (XT and AT), in addition to Intellec Series IV. Emulation speeds to 10 MHz. SDK-86 single-board kits for low-cost evaluation and familiarization. EMV-88 for 8088, supported on iPDS Personal Development System.
iPAT Performance Analysis Tool, said to give designer maximum control of design's performance and reliability. Consists of hardware base unit, an interface to I²ICE and software for host processor (which can be IBM PC AT/XT or Intellec Series III/IV). iPAT provides high-level access to target system performance analysis and test case code coverage analysis.

From Intel: Macroassembler including relocation/linkage utility, 8087 numerics emulator, and an obj/hex converter for IBM PC, VAX/VMS, and Intellec Series III/IV. High-level languages available include PL/M-86, C-86, Pascal-86, and Fortran-86. A configurable end-user operating system (iRMX-86) available for OEMs to embed in their products.
From others: Because wide base of 8086/8088-based systems and in particular the IBM PC, there's a very wide body of third-party software of all sorts, enough to fill whole catalogues. Check with Intel and various trade journals.

NOW MULTIBUS I CAN PROCESS THE BIGGEST NUMBER IN COMPUTING.



The most popular OEM bus in the world now comes equipped with the most powerful 32-bit microprocessor.

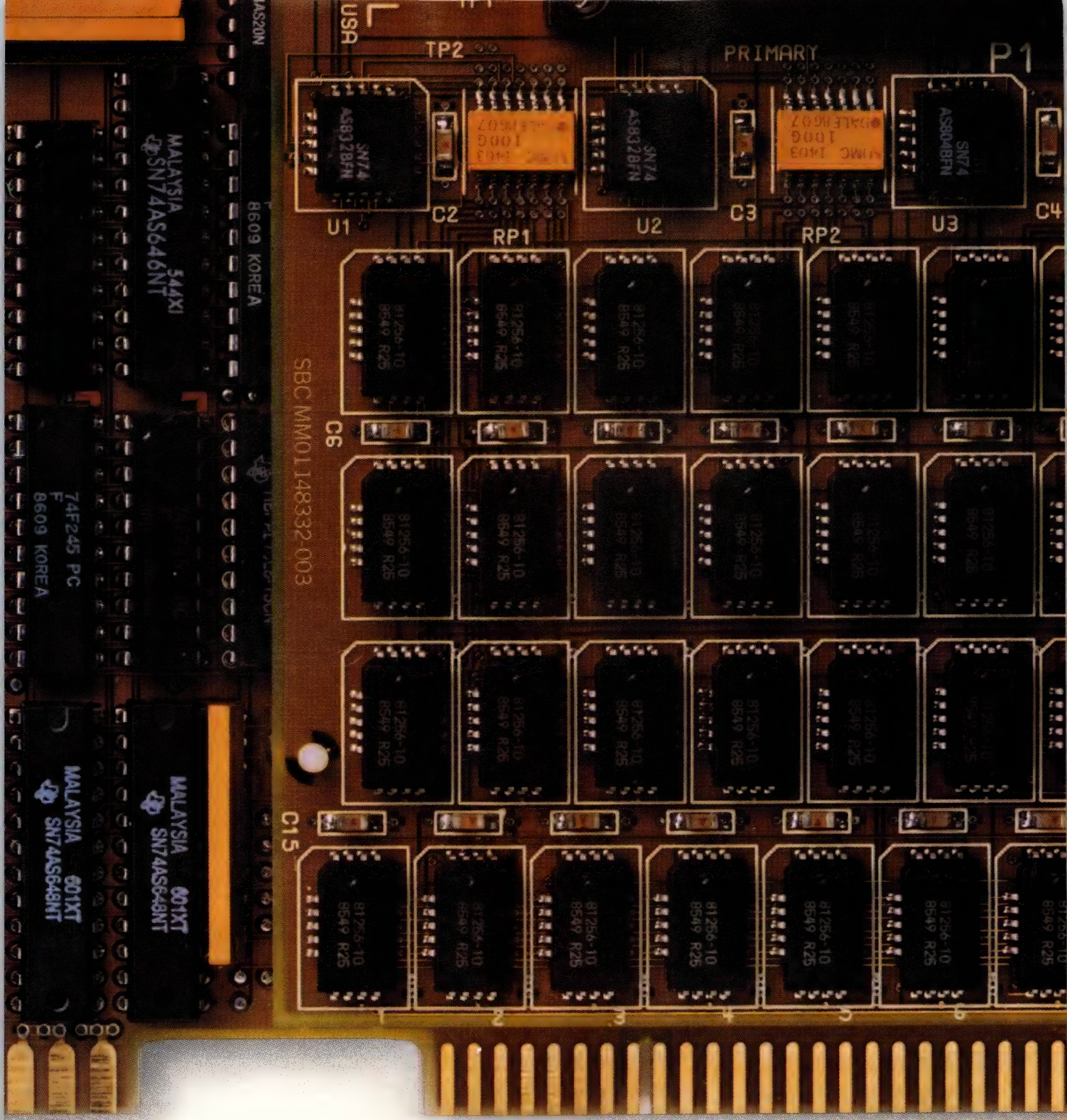
Intel's 80386.

We're talking a full line of boards that give you true 32-bit processing power.

To make all of this happen, we designed a locally accessible 32-bit data path that lets our 16 MHz 80386 execute at absolute maximum speed.

Then we added up to 16 MBytes of memory. And a 64 KByte zero wait state write-through cache for highest performance. Combined with the latest surface mount technology.

The result is a whole family of super-fast 386-based MULTIBUS® I CPU boards and snap-on memory modules



that give you from 1 to 16 MBytes of memory.

So now you can triple performance on your existing system. Or build new ones. And exploit the full capabilities of the 80386 microprocessor, while leveraging your MULTIBUS I investment in existing real time, multi-user and proprietary operating systems.

For further information, call Intel at (800) 548-4725. Ask for Lit. Dept. W335.

And see how MULTIBUS I and the 80386 really add up.

intel®

80286

16-BIT NMOS

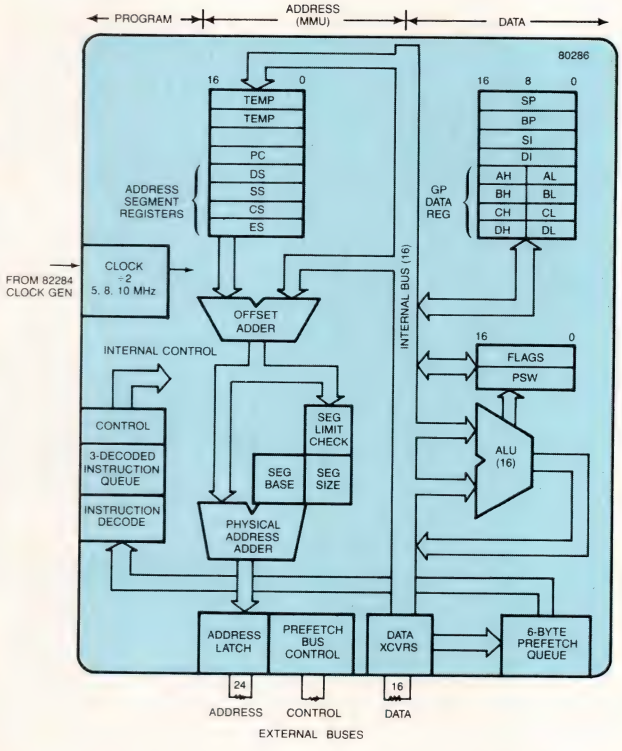
AVAILABILITY: In production with 6-, 8-, 10-, and 12.5-MHz 80286. AMD says it will have 16-MHz version in second quarter '87
COST: $73 for 8 MHz, $85 for 10 MHz, $100 for 12.5 MHz, and $150 forcast for 16 MHz in LCC packages (PGA more). AMD prices in 100 qty
SECOND SOURCE: AMD, Siemens, and Fujitsu

Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080

Description: An evolutionary extension of the 8086 with special capabilities for multiuser and multitasking systems. Has on-chip memory-management and protection functions that support intertask isolation, program and data security, and four levels of privilege within a task. Memory management supports as much as 1G byte of virtual address space per task, mapped into a 16M-byte physical memory. Device is upwardly compatible with 8086/88 software.

Status: According to Dataquest, the 80286 has been most successful. 1985 unit volume was 1,405,000 units, which at going 286 prices represents a very healthy revenue for Intel (who shipped the majority of the volume). Much of this may have been the 286's use in the IBM PC/AT. No plans for CMOS from Intel through '86 but AMD has 80L286 low-power NMOS versions, which company says consume 37% less power.

HARDWARE CHARACTERISTICS SOFTWARE



Support chips for the 286: 82284 clock, 82288 bus controller, 82289 bus arbiter, 80287 floating-point numeric processor ($350 for 10 MHz, 100 qty), and 82258 advanced DMA coprocessor.

I—DATA-MANIPULATION INSTRUCTIONS
8- and 16-bit signed and unsigned arithmetic in binary or decimal, including multiply and divide
Logical operations on bytes, words, and blocks
II—DATA-MOVEMENT INSTRUCTIONS
Addressing modes include Literal, Relative (to register and to segment), Register, Base Plus Index, Base Relative Indexed, and Register Indirect
Programmers can manipulate 16,383 segments in memory by means of memory-base descriptor tables and four segment registers. These segments can be between 1k and 64k bytes in length
III—PROGRAM-MANIPULATION INSTR
Has calls, jumps, and returns within the same protection level, across protection boundaries, and between tasks
Intrasegment calls and jumps use self-relative displacement for position-independent code
Intersegment calls and jumps use the memory-based descriptor tables to provide position-independence of code
Conditional jumps upon Boolean functions of flags within ±128 bytes of instruction
Iteration control of loops
String instructions, including Repeat, for rapid iteration
IV—PROGRAM-STATUS-MANIP INSTR
8085 flags (carry, auxiliary carry, parity, zero, and sign) plus overflow, interrupt enable, direction (strings), trap (single-step), I/O privilege level, and nested task. Flag register is software accessible
Notes:
1. Has high-level-language support instructions.
2. Virtual-address translation, memory management, and protection performed by CPU for faster execution.
3. Trusted instructions can only be executed at highest protection levels.

Specification summary: 16-bit CPU with a 1G-byte virtual address space per user, mapped onto a 16M-byte physical address space. Bus cycles execute in 250 nsec at 8-MHz clock (200 nsec at 10 MHz), requiring 0.25 μsec for register-to-register moves at 8-MHz clock, with 8M-bytes/sec bus bandwidth. HMOS ion-implanted, silicon-gate circuitry, in a large chip (335×339 mils, approximately 134,000 transistors). Requires 5V at 600 mA. Has two operating modes: Real address mode emulates 8086; protected virtual address mode native to 286. Housed in a 68-pin JEDEC Type A leadless chip carrier, PLCC, and PGA.

HARDWARE SUPPORT SOFTWARE

From Intel: I²ICE emulation system is available for the IBM PC (XT and AT) in addition to the Intellec Series IV system. Emulation fully supports 286's protection scheme. Up to 288k bytes of high-speed program memory available via optional high-speed memory (OHS) boards. Optional support for PLCC package.
For maximum control of performance and reliability in 80286-based designs, Intel offers its new iPAT Performance Analysis Tool. iPAT consists of a hardware base unit, an interface to I²ICE, and host software for the PC AT/XT, as well as Intellec Series III/IV. iPAT provides high-level access to target system performance analysis and test case code coverage analysis for the 80286.

From Intel: In addition to macroassembler (ASM 286) and system utilities (BUILD 286, BIND 286, LIB 286), Pascal, PL/M, Fortran, and Ada are available. Real-time operating systems (Intel's iRMX 86 and iRMX 286) available. Support hosts include IBM PC, VAX/VMS, and Intellec Series IV. Prices are $750 for single-user license on PC or Intellec system and $10,000 for multiuser on VAX.
From others: Other operating systems and compilers being developed by third-party software houses include MP/M-286 (Digital Research), Xenix-286 (Microsoft), Coherent 286 (Mark Williams), Concurrent DOS (Digital Research), and Unix System V (Digital Research).

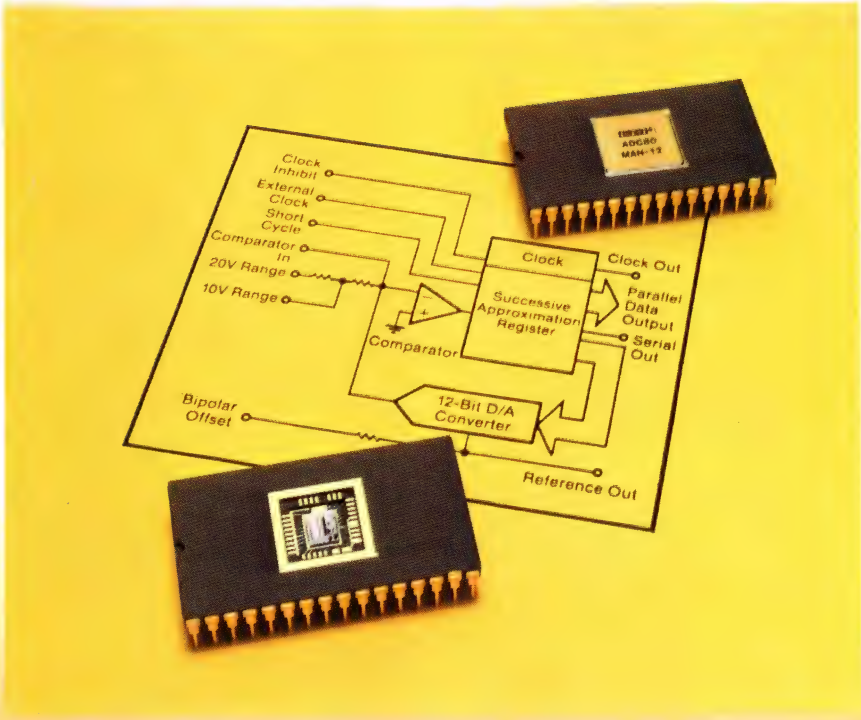
BURR-BROWN

update

product developments

Vol. XII, No. 3

Newest Monolithic ADC80 Is Price/Performance Leader



Circle RS No. 001*

Burr-Brown's new ADC80MAH-12 offers exceptional value as the latest version of this industry-standard 12-bit A/D converter. Its advanced monolithic design and processing provide superior performance and reliability at the industry's lowest prices.

ADC80MAH-12 is a complete device, with comparator, 12-bit DAC, 6.3V laser-trimmed reference, successive approximation register (SAR), clock, and associated logic on a single IC chip. On-chip pull-up resistors eliminate the need for external resistors for the digital inputs. ADC80MAH-12 is packaged in a 32-pin hermetic DIP, compatible with all existing competitive models for easy changeover. An environmentally-screened "/QM" version is also available.

ADC80MAH-12 features true 12-bit accuracy and high speed conversion, allowing system throughput sampling rates up to 40kHz. Input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V are selectable, and all digital input and output signals are TTL/LSTTL-compatible. Both parallel or serial outputs are provided. The new A/D operates equally well with either ±15V or ±12V analog power suplies and a +5V logic supply; no +5V analog supply is needed, an advantage over many competing devices. Power supply dissipation is a low 705mW max, considerably less than many similar ADC80s.

Key ADC80MAH-12 Specifications:

Resolution	12 bits
No missing codes	−25°C/+85°C
Linearity error	±0.012%FSR max
Conversion time	25μs max
Power dissipation	705mW max

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BB

* Circle magazine Reader Service Numbers to obtain additional product information.

Using OPA600 For High Performance PGA and IA Applications

Burr-Brown's new ultra-fast FET op amp (*Update* XII, 2) provides a unique combination of speed, drive, and gain-bandwidth product to boost the performance of many common op amp applications.

PGA For High-Frequency Waveform Digitizer Circuits

The programmable gain amplifier (PGA) in Figure 1 has four non-inverting gain steps corresponding to common oscilloscope vertical sensitivity settings (i.e. 1, 2, 5, and 10). This type of amplifier is ideal for waveform digitizers. The input impedance is set to 1MΩ, and the output can drive 50Ω systems. The feedback networks are switched in one at a time by the SD5000 DMOS FET switches. The SD5000 is chosen because of its low drain and source node capacitances (1.3pF for the drain and 3.5pF for the source).

Any capacitance at the inverting input of the OPA600 can be a cause for instability. The lower this capacitance is, the better the stability is without additional compensation. A small capacitor across the feedback resistor increases the stability at the cost of decreased bandwidth. When the OPA600 is compensated for a gain of one, the bandwidth of the highest gain (Gain = 10) will be around 10MHz. The following chart shows the bandwidths for each gain setting:

Gain	Bandwidth (−3dB)	
	Small Signal	Large Signal
1	98MHz	32MHz
2	60MHz	28MHz
5	22MHz	16MHz
10	12MHz	10MHz

IA Provides High CMR At High Frequencies

The instrumentation amplifier (IA) in Figure 2 can be used to obtain high common mode rejection at high frequencies. This IA is set to a gain of one and can reject common mode frequencies by 75dB up to 5MHz (see the graph in Figure 3).

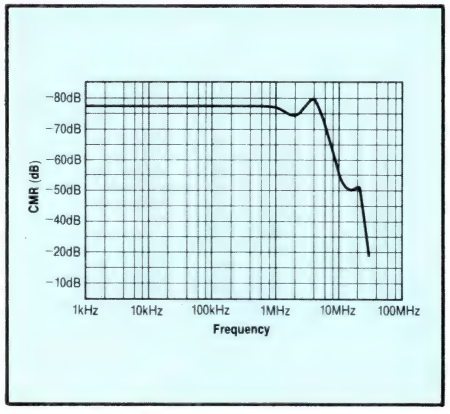
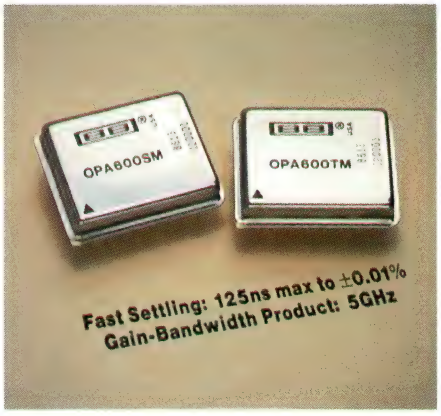


FIGURE 3. CMR vs. Frequency.

To obtain this performance, both input amplifiers must have identical "phase responses". This can be obtained by adjusting the compensation for one of the input amplifiers until it is stable, then adjusting the other until maximum rejection is achieved at the output of the IA.

Key OPA600 Specifications:

Settling time
(0.01%, 10V steps) ..... 125ns max
Gain-bandwidth product (G = 1k)... 5GHz
Closed-loop bandwidth (G = +1V/V,
−3dB compensated) 125MHz
Slew rate (G = 1V/V) ..... ±400V/μs min
Output voltage (R_L = 50Ω) ..... ±10V



Circle RS No. 002

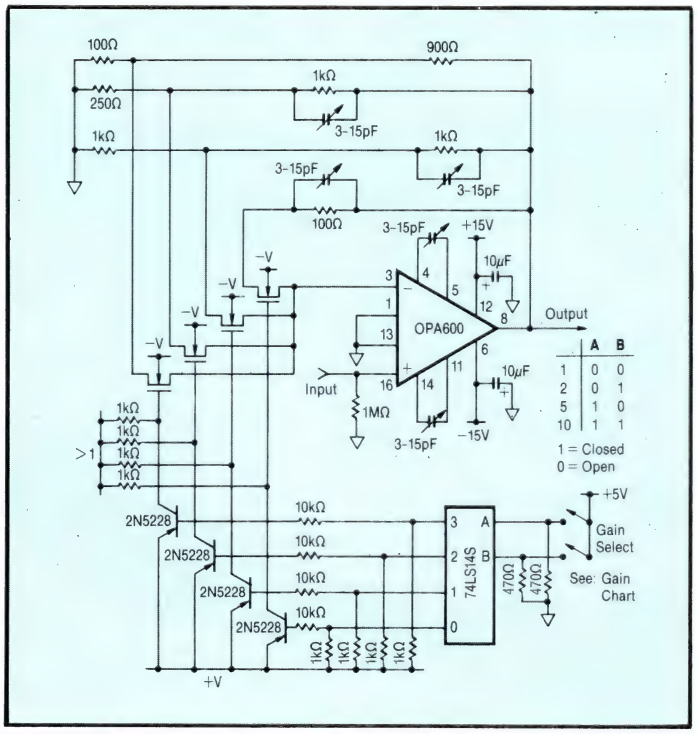


FIGURE 1. High-Speed Programmable-Gain Amplifier.

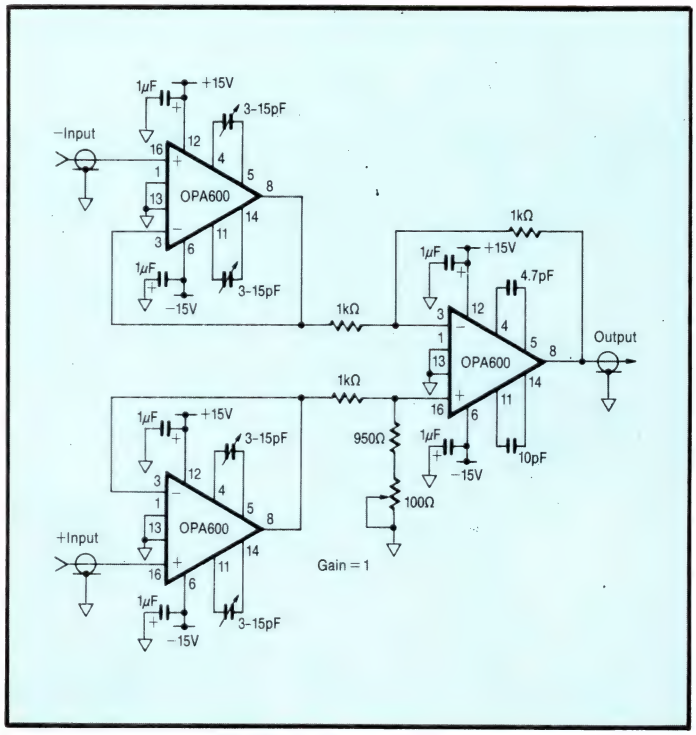


FIGURE 2. Instrumentation Amplifier.

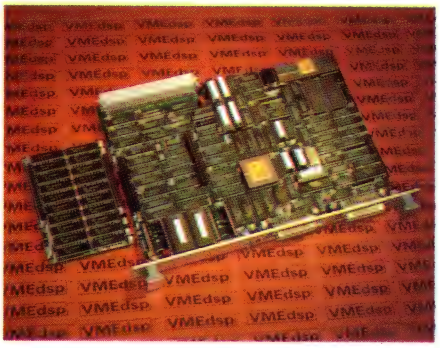
Versatile VME Board For High-Speed DSP

The new SPV120 is a fast, multi-function board suitable for a wide range of VMEbus-based digital signal processing applications. A powerful TMS32020 processor chip and two high-speed parallel I/O ports under DMA control achieve data transfer rates up to 4Mbytes/sec with minimum burden to the VMEbus.

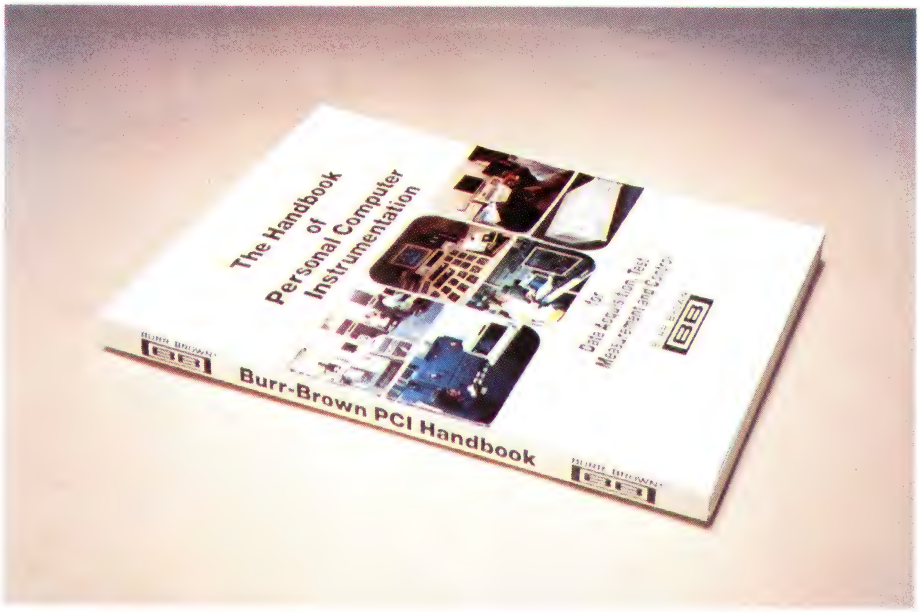
Onboard program memory consists of 16kbytes of EPROM and 16kbytes of zero-wait-state PROM, expandable to 32 or 128kbytes of fast static RAM. Local and global data memories are of 32kbytes each, expandable to 64kbytes. An optional ACX120 plug-in memory expansion module adds sufficient memory to complete address capability for the TMS32020.

For customized software development, the ACX120 allows TMS32020 object code to be down-loaded from the development system to the board's program memory for execution and debugging under control of a software monitor. The proven software may then be executed from RAM or, alternatively may be loaded into PROM and fitted to the SPV120 as non-volatile code.

Extensive software support will soon be available for the SPV120, including a TMS32020 cross assembler, a monitor/debugger, and a selection of DSP applications programs.



Circle RS No. 003



Free PC Data Acquisition Handbook, and Demo Diskettes

The Handbook of Personal Computer Instrumentation for Data Acquisition, Test, Measurement and Control is an industry first. Amost 200 pages contain everything you ever wanted to know—and then some. Here's a sample of what's included:

- A tutorial section describing, in practical terms, the theory and philosophy of using personal computer instrumentation (PCI).
- An applications section, complete with dozens of diagrams.
- A software section that describes and references the wide range of packages that are readily available.

The PCI Handbook
Burr-Brown International Publications
and Distributors Co.
P.O. Box 7735
1117 ZL Schiphol
The Netherlands

Demonstration Disks

Designed to show product capabilities, specifications and applications for the PCI-20000 system, this demo disk runs on the IBM PC and compatible computers that contain a graphics card.

It's yours for the asking. Just contact the Burr-Brown sales office or sales representative nearest you.

How BURR-BROWN Create The High Resolution

Helped Nicolet Industry's Fastest Digital Storage Oscilloscope

The new ADC600 gives Nicolet's 4094 DSO System 12-bit resolution with 8-bit speed

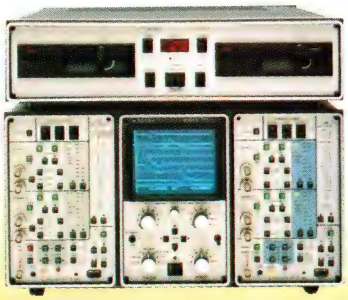
When Nicolet wanted both high resolution and ultra-high speed for its new DSO digitizer module, they brought their specs to Burr-Brown, the leader in high performance analog-to-digital conversion technology. They left with a handshake commitment to solve their problem. They got the ADC600 12-bit, 10MHz sampling A/D converter.

"... more than we asked for."

"We subjected the Burr-Brown ADC600 to a series of tests including noise, distortion, linearity (differential and integral), and bandwidth at frequencies from DC to above 10MHz. The results of these tests, plus the straightforward interface to our system, convinced us to select the ADC600 for our application. They gave us more than we asked for."

Jim Hyatt
Product Design Manager
Nicolet Test Instruments Division

ADC600 is the first high resolution, ultra-high-speed sampling converter to combine small size, low power dissipation, and straightforward interfacing in a reliable, low cost design. It's complete with sample/hold, encoders, reference DAC, and timing circuits on a space-saving, 17-square-inch printed-circuit card. And it's easy to use, requiring only external power supplies and CONVERT command for operation.



Key ADC600 Specifications

Resolution	12 bits
Sampling rate	10MHz min
Linearity error (200Hz)	±1.25LSB max
Harmonic distortion (F_{IN} = 1MHz to 5MHz)	65dB
Input range	±1.25V
Signal-to-Noise Ratio	70dB
Power dissipation	8.5W
No missing codes	0 to +70°C

With ADC600, Burr-Brown continues a thirty-year tradition of solving customer problems through innovative designs, high quality manufacturing, and dedicated customer service and assistance.

"Customer response has been excellent."

"The ADC600 provides state-of-the-art high-resolution digitizer performance in our already powerful 4094 digital scope. Many applications require 12-bit precision but also 8-bit speed; the Burr-Brown modules do both. Customer response has been excellent."

Dale Baldwin
Marketing Manager
Nicolet Test Instruments Division

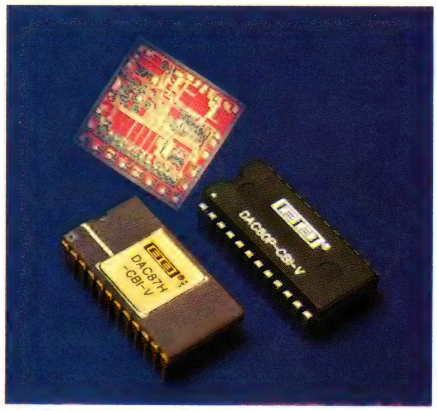
If you have a data conversion problem, we invite you to contact Burr-Brown. You may be only a handshake away from the solution.

Burr-Brown Corporation
P.O. Box 11400, Tucson, AZ 85734
602/746-1111

Circle RS No. 004

BURR-BROWN®

Improving Data Conversion Productivity



Circle RS No. 005

New Monolithic DAC80s With Improved Performance, Lower Prices

Burr-Brown invented this industry standard 12-bit D/A converter twelve years ago as an eleven-chip hybrid. Now, Burr-Brown's new, monolithic DAC80, DAC85H, and DAC87H offer the same speed and precision as the hybrids, plus 50% lower power dissipation (345mW vs. 975mW max), higher reliability (7.39×10^8 hours MTTF at +25°C), and lower prices, up to 50% reductions for some models.

Monotonicity is guaranteed across the specified temperature ranges for these models: DAC80, 0°C to +70°C; DAC85H, −25°C to +85°C; DAC87H, −55°C to +125°C. Inputs are TTL- and CMOS-compatible. All DACs operate over the full 11.4V to 16.5V power supply range.

DAC80, 85H, and 87H are offered in 24-pin hermetic (Method 1014, Conditions A1, A2, and C) side-brazed DIPs. DAC80 is also available in a very low cost, molded plastic DIP with the exact same specifications. The new devices use the industry standard pinout, compatible with competitive models, including DAC80D.

DAC85H and 87H are available with additional "/QM" environmental screening including pre-cap visual, stabilization bake, temperature cycling, burn-in, and constant acceleration.

Key DAC80, 85H, 87H Specifications:

Resolution	12 bits
Linearity error	±1/2LSB max
Settling time (±0.01%FSR)	3μs (V_{OUT}), 300ns (I_{OUT})
Power dissipation	345mW

Unit prices, in 100-249 quantities, range from $13.25 (DAC80P-CBI-I) to $55 (DAC87H-CBI-V), more for /QM screened models.

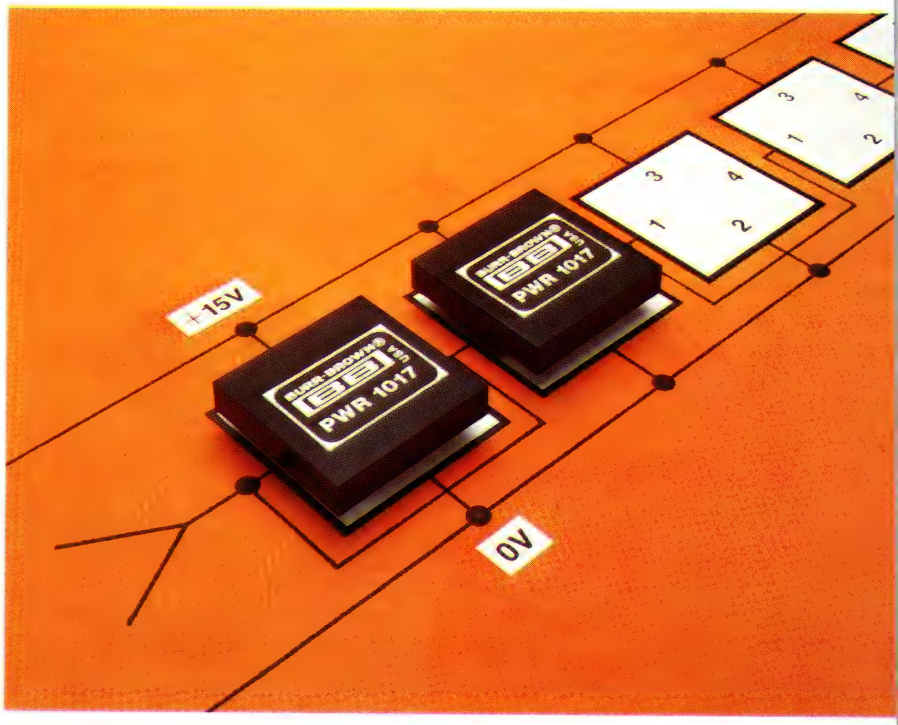
Unique Synchronizable DC/DC Converter Solves Switching Noise Problems

When multiple power supplies are needed for a system, their beat-frequency switching noise can mask signals and cause major problems. Burr-Brown's new PWR 1017 solves the problem with a unique Master/Slave design. Slave pins on multiple units can be connected to a Master pin on one unit, synchronizing all switching frequencies to the Master converter and eliminating all beat-frequency noise. For even greater design flexibility, multiple PWR 1017s can be driven by an external system clock.

PWR 1017 accepts +15VDC inputs and provides four ±15VDC outputs, with 1000VDC isolation channel-to-channel a output-to-input. Other features include s sided shielding, input and output filterin and a low 0.4" profile package. Each PW 1017 is tested in compliance with UL544, VDE750, and CSAC22.2 dielectric withsta specifications, plus 100% barrier leakage current testing.

Key PWR 1017 Specifications:

Input/output ranges	10/18VD ±16/18V
Rated output current	25mA r
Output power	3W m
Switching frequency range	200-350k
Free-running switching frequency	250k
Specified temp range	−25/+85



Circle RS No.

Free Tips on Photodiode Amplifier Circuit Design

A new Application Note, *Designing Photodiode Amplifier Circuits With OPA128*, is now available. The note, AN-151, describes in detail how to minimize the trade-offs, improve the performance, and avoid the pitfalls of these transimpedanc designs. Highlighted are high-sensitivity, wide-temp-range, and wide-bandwidth photodiode amplifier circuits. Advantage of using Burr-Brown's new, monolithic OPA128 with low noise, low drift, and ultr low 75fA max bias current are also discussed.

Circle RS No. 0

ore Fiber Optic ata-Comm Products

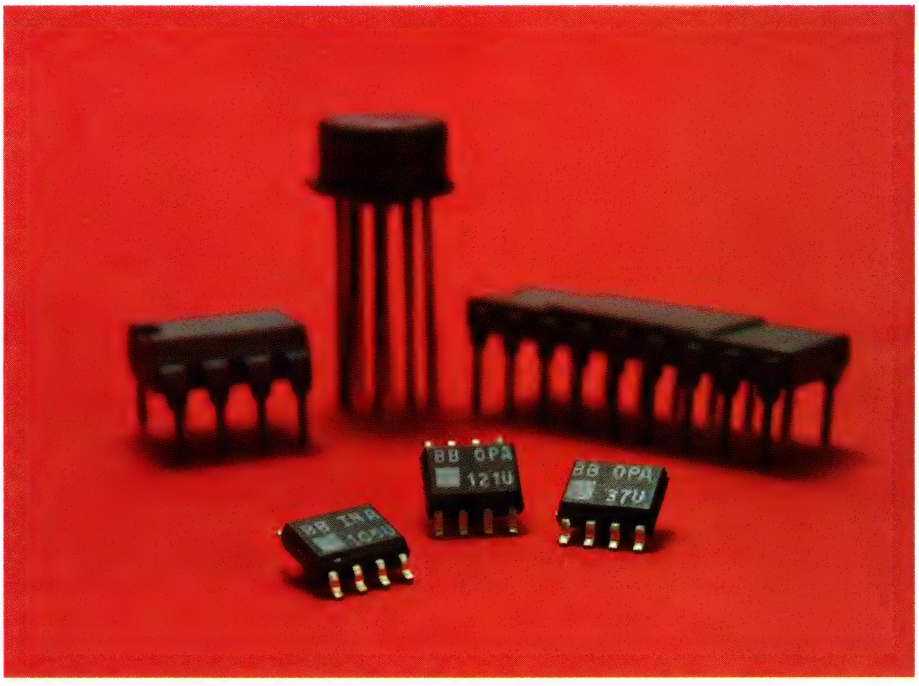
rr-Brown's family of fiber optic products s been expanded to include an RS-232-to- er optic multiplexer/demultiplexer, IX800, and a low cost, signal powered er optic modem, LDM80. These products d the existing LDM85 fiber optic modem ow the implementation of complete fiber tic local area networks.

single FMX800 enclosure contains a wer supply and motherboard which cepts plug-in cards. It is designed to cept a high speed, fiber optic module, 1 16 RS-232 cards, and an expansion card. annels may have baud rates as high as 2 kilobaud. Future cards will allow fiber tic local connections and a coaxial high eed link. Size is 16.5 X 4.5 X 6 inches. A ndard 19-inch rack adapter is available.

M80 fiber optic modem communicates at to 19.2 kilobaud for distances of up to 2 ometers. It is totally powered by the -232 port to which it connects. Size is X2.1 X 0.85 inches.

per optic cable may be ordered with nnectors installed.

Circle RS No. 008



Circle RS No. 009

Miniature Surface Mount High Peformance Op Amps

Burr-Brown introduces OPA121U, OPA27/37U, and INA105U, the first high performance operational amplifiers available in miniature, small outline IC packages (SOICs) measuring approximately .2 X .15 X .1 inches with eight "gull-wing" leads on 50-mil centers. They can be surface-mounted on one or both sides of a PC board and save designers 50% or more of the space normally required for these analog circuits. The new SOICs will also fit inside many transducer cavities and can be used on modules or even hybrid circuits. They will be particularly useful for miniature transducer, portable instrumentation, and many automotive applications.

OPA121U is a precision *Difet*® op amp featuring low 10pA max bias current, 3mV max offset voltage, and 3μV/°C drift. OPA27/37U is a SOIC version of the standard, ultra-low noise op amp featuring 3.2nV/$\sqrt{Hz}$ noise (1kHz), and low 100μV max offset. INA105U is a popular new precision unity gain differential amp with 0.001% max nonlinearity, 0.025% max gain error, and 72dB min CMR over temp.

Difet® Burr-Brown Corp.

update

Coming Soon

Isolated Analog/Digital VMEbus I/O Board

MPV906 will provide 32/64 software-programmable analog input channels and 32 channels of programmable digital I/O; features 12-bit resolution, 25μs conversions, and optical isolation between I/O and VMEbus.

More PWR 1017 Input Voltage Models

In addition to the standard +15V model, 5, 12, 24, 28, and 48 input volt models will also be available soon.

Ultra-Stable, Precision 18-Bit D/A Converter

DAC729 will be a complete device featuring ±0.00075% max linearity error, 0.5ppm/°C max linearity drift, and 20ppm/1000hr max long-term reference stability. It will be the industry's most accurate and stable hybrid DAC for about half the price of larger, discrete modules providing similar performance.

Dual 16-Bit μP-Compatible D/A Converter

DAC725 will provide two 16-bit DACs with double-buffered, 8-bit bus-compatible input logic, packaged in compact, 28-pin hermetic ceramic or plastic DIPs. DAC725 will be complete with separate gain and offset adjust lines, address and reset control logic, fast, low-noise output op amps, and precision buried-zener references.

New 12-Bit A/D Converters Will Break The 1μs Barrier

ADC801 and ADC802 will have guaranteed 900ns performance in the ADC803 pinout and package. Also lower power dissipation and chip count for greater reliability.

1.5μs 12-Bit A/D Converter Sets New Price/Performance Level

ADC806 will match the speed and pinout of the ADC803 with lower power and lower price. Reduced chip count and reduced power translate into higher reliability.

Price/Performance Improvements On Industry Standard A/D Converters

ADC84KG, ADC85H, and ADC87H will soon be available with lower chip count, lower power dissipation, and hermetic, ceramic side-brazed packages. In additio prices will come down! And both the ADC85H and the ADC87H will be availab with burn-in and other environmental screening.

Military Applications Seminars In Your Are

The continuing series of applications seminars focusing on Military Products Division products, applications, and capabilities are scheduled in the following cities.

Baltimore, Orlando/St. Petersburg, Huntsville ..... January '8
Phoenix, Tucson, Albuquerque ..... February '8

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Telephone 0923-46759
Telex 922481

Burr-Brown International Publications and Distributors Co.
P.O. Box 7735
1117 ZL Schiphol
The Netherlands
Telephone 020 470 590
Telex 13024

Burr-Brown Ltd. (Scotland manufacturing facility)
Simpson Pkwy., Kirkton Campus
Livingston, West Lothian
EH54 7BG
Telephone 0506-414 445
Telex 727484

AUSTRIA
Niederlassung Osterreich
Burr-Brown Research Gesm.b.H.
Senefeldergasse 11
A-1100 Wien
Telephone 0222/62 63 71
Telex 134777

BELGIUM
Burr-Brown International B.V.
Avenue Coghen 118
B/1180 Bruxelles
Telephone (02) 347-44-30
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THE NETHERLANDS
Burr-Brown International B.V.
P.O. Box 7735
1117 ZL Schiphol, Holland
Telephone 020-470590
Telex 13024

FRANCE
Burr-Brown International S.A.
18 Avenue Dutartre
F-78150 LeChesnay
Telephone (013) 954-3558
Telex 842 6963 72F

ITALY
Burr-Brown International S.r.l.
Via Zante, 14
20138 Milano
Telephone (02) 506 52 28
Telex 316246

JAPAN
Burr-Brown Japan Ltd.
Natural House Building
14-15, 6-chome, Akasaka
Minato-ku, Tokyo
Telephone (03)586-8141

Osaka: Telephone (06)305-3287

SWEDEN
Burr-Brown International AB
Kanalvägen 5
194 61 Upplands Väsby
Telephone 0760-93010
Telex 14489

SWITZERLAND
Burr-Brown AG
Weingartenstr. 9
CH-8803 Rueschlikon/Zürich
Telephone (01)724-0928
Telex 59880

UNITED KINGDOM
Burr-Brown International Ltd.
1 Millfield House
Woodshots Meadow, Watford
Hertfordshire, England WD1 8YX
Telephone 0923-33837
Telex 922481

WEST GERMANY
Burr-Brown International GmbH
Weidacher Strasse 26
D-7024 Filderstadt 1
Telephone 0711/70 10 25
Telex 177111257

Bremen: Tel. 0421/25 39 31

Düsseldorf: Tel. 02154/84 45

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Printed in U.S.A. November, 1986

80386

AVAILABILITY: 12.5, 16, and 20 MHz in production
COST: $299 for 80386, $15 for 82384 clock generator
SECOND SOURCE: None announced

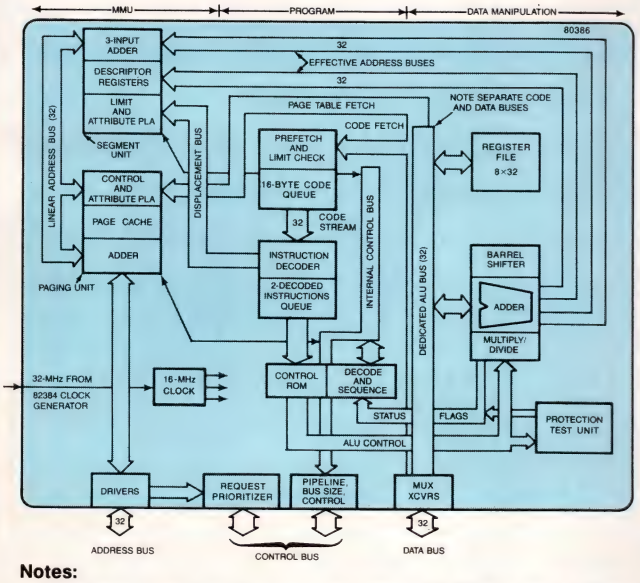
Description: This 32-bit member of the 8086 family contains a full 32-bit, largely uncharacterized register set (some competitors debate this) and an on-chip MMU containing selectable segmentation and paging support with a 32-entry translation lookaside buffer cache. 100% binary compatible with the 8086 and 80286, allowing 8086 and 80286 and 80386 applications to run concurrently. It's fabricated in 1.5-μm CMOS using double-layer metal interconnects and has over 275k transistors.

Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080

32-BIT CMOS

Status: Few μPs have received such public notice: EDN has found that even the lay public is aware of the 386 and realizes how it may soon put the power of a minicomputer in everyone's PC. Competitors say it's only a stretched version of the 80286, but Intel says it has benchmarked the 386 at 6000 to 7000 Dhrystones/sec at 16 MHz, which puts the 386 at the VAX 8600 performance level. Note that sometimes Intel goes outside the 8086 family for these benchmarks, using the Weitek 1167 math chip. At any rate, this machine certainly should give the public what it expects—entry into the higher-performance 32-bit world. The 386 should have a solid success. IBM has yet to announce a PC using the 80386 but a number of hardy companies (Corvus, Compaq) are using the 386 as the basis of 32-bit PCs.

HARDWARE CHARACTERISTICS SOFTWARE



Notes:
1. Intel was going to have instruction cache on the 80386 (see the 1984 directory entry for 80286/80386) but said it subsequently abandoned that when it couldn't squeeze a big enough cache on chip (4k to 8k bytes) to really boost performance. But it's asserted that the 386's fast 2-clock-cycle accesses to external memory allow user to implement effective off-chip caches of arbitrarily large size (for example, to 32k bytes).
2. Having MMU on chip said to allow for memory management with no penalty in bus bandwidth (if off chip, supplier says an extra cycle would be needed). Allows choices of segmentation or paging singly or in combination for multiuser protection and for virtual memory. The hit rate in the MMU cache is said to be 98%.
3. The 80386 will have its own math coprocessor, the 80387, which is scheduled for late '86. Meanwhile, the 386 can use the 80287 math coprocessor meant for the 80286. For yet more performance acceleration, Intel suggests using the Weitek 1167 math chip.
4. Along with the 80387, the 80386 uses the following support chips: the 82384 clock generator and the 8259A interrupt controller, 82786 graphics coprocessor, 82258 DMA controller, 87586 and 82588 LAN controllers, and upcoming 32-bit peripheral combination chips.
5. Supplier says it's working on further enhancements of 386 and has mentioned the part number "80486" to OEMs as assurance that the 386 will not be last in 8086 family line.

I—DATA-MANIPULATION INSTRUCTIONS
Bit manipulation and bit-string manipulation (aided by 64-bit barrel shifter)
Conversion between bytes, words, and double words
Arithmetic including 16- and 32-bit operands and 32-bit signed and unsigned multiply and divide
Forthcoming 80387 math coprocessor will have full IEEE-754 instructions, including all transcendentals
II—DATA MOVEMENT INSTRUCTIONS
String moves and gang push and gang pop of all registers
Instructions to insert and extract bit strings (additional adressing modes for existing instructions allow more flexibility in assignment of registers)
III—PROGRAM-MANIPULATION INSTR
Repeat instructions based on flags
Enter and leave procedure instructions, conditional or unconditional branch to anywhere in 4G-byte memory space
IV—PROGRAM-STATUS-MANIP INSTR
Flag instructions mostly same as on 8086 (contains 4 debug registers, allowing breakpoints on data or code accesses, even when in ROM)
V—HLL AND OS INSTRUCTIONS
Instructions for checking array bounds
Segment assignment instructions
Load and store descriptor tables for protection (processor context switch via one instruction)
Notes:
1. Only those instructions beyond basic 8086 instructions described.
2. 80386 said to be object-code compatible with previous members of 8086 family and can run their operating systems. A "virtual 8086" mode lets 8086 (and 8088) code run within the protected 386 environment.

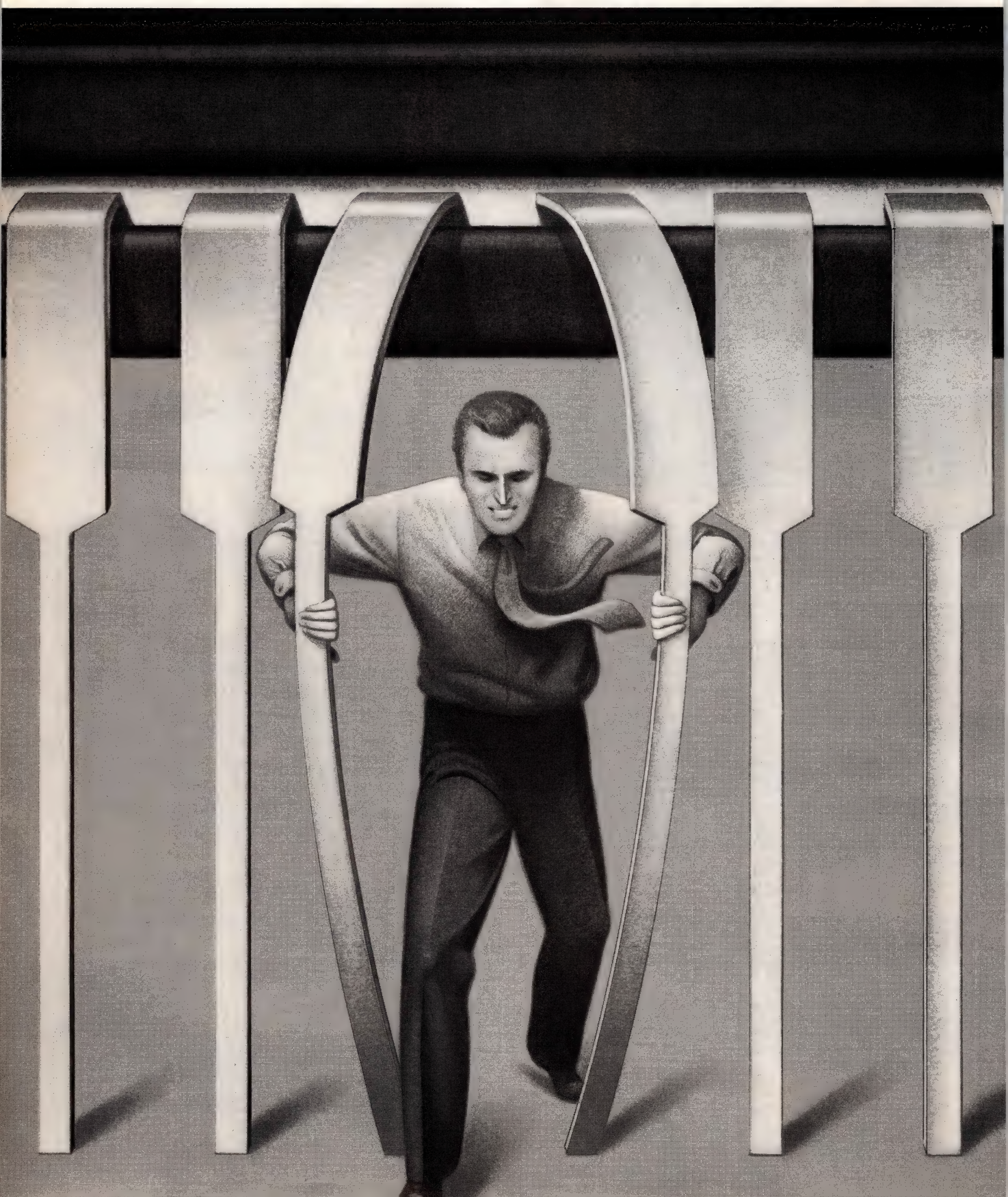
Specification summary: A more or less standard, classical 32-bit minicomputer architecture that has a basic register set similar to the previous 16-bit members of the 8086 family so that it can directly run their machine code. It has added features that make it more general and suited to larger 32-bit environments: data-manipulation instructions that can be applied to almost any register, high-level-language-oriented instructions, operating-system-oriented instructions, and on-chip MMU. Performance projected to be a 3 to 4 MIPS with 8-MIPS burst rate when operating at 16 MHz and with sufficiently fast (80-nsec) memory. Fabricated in 1.5-μm CMOS (supplier calls it CHMOS-III), it's expected to consume no more than 400 mA at 32-MHz external clock (16 MHz internal). Packaged in 132-lead ceramic pin-grid array.

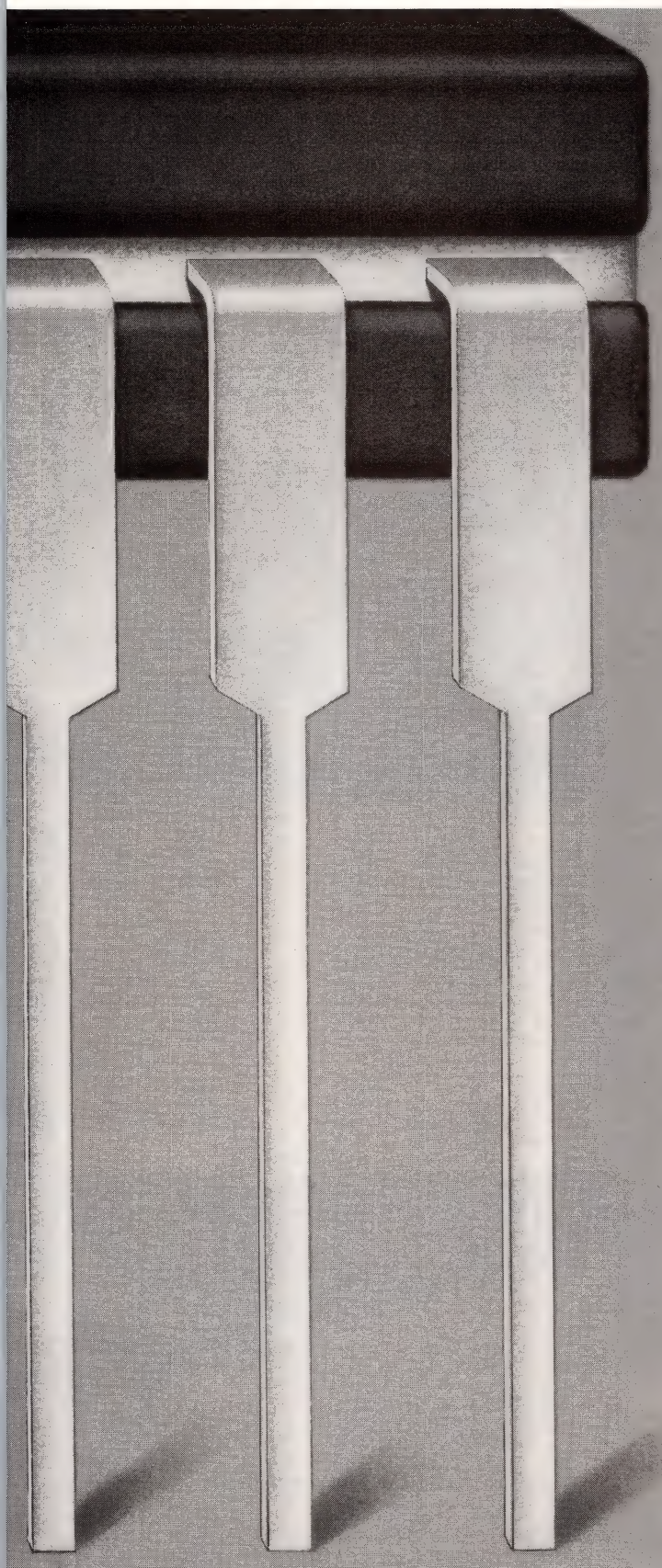
HARDWARE SUPPORT SOFTWARE

ICE-386 in-circuit emulator for 80386 hosted on Intel 286/310. In conjunction with four on-chip breakpoints, it allows full 16-MHz operation in continuous or single-step mode. Can store more than 2000 frames of program-execution history. Has high-level-language symbolics. Can analyze time taken by code. Supports 80287 and 80387 coprocessors.
iSBC 386/20 single-board computer for Multibus I and iSBC 386/100 single-board computer for Multibus II. Along with the usual features expected of supplier's single-board computers, these incorporate 64k-byte caches to permit 16-MHz execution of 386. Starter kits are $9490, $7995, and $3860 (100).

From Intel: PScope Monitor 386, a high-level software debugger for 386 single-board computers. Intel Translator software tools include an assembler ($600), relocation linker and library ($900), and compilers for C ($900), PL/M ($900), Fortran, and Ada. The compilers are said to be optimized for 386 execution speed. The tools are resident on supplier's Xenix-286/310 computer, VAX/VMS, and IBM PC. Said to incorporate easy translation from 6-bit 8086 and 80286 code to 32-bit 80386 code. Also iRMX 86/386 software, which is extension of iRMX 286 real-time operating system.
From others: Available from third parties are UNIX System V, release 3, (fourth quarter '86 from AT&T), virtual DOS monitors (uses virtual 86 mode to run DOS on UNIX), optimizing compilers supporting 80387 and 1167 for C, Fortran, Pascal, Cobol, PL/1, Basic, RPG II.
Contact Intel for names of suppliers of growing body of more specialized software being developed for 386.

BREAKTHROUGH!
THE FIRST AND ONLY 80C51 WITH THREE EXTRA I/O PORTS.





Signetics introduces the 83C451.

It has seven I/O ports—nearly twice as many as you get with the standard 80C51. So you'll never again need to design in two CMOS microcontrollers to have enough I/O; one will do.

What's more, the 83C451 gives you those seven ports in a single package. Which means the board real estate that used to be taken up by that redundant second chip can now be devoted to other concerns.

You don't lose any speed, either. The 83C451 is still as fast as they come—12 MHz.

What else do you want in a CMOS microcontroller? Mailbox Port with Handshake? Done. On-board ROM? It's standard with the 83C451. If you *don't* want ROM, get the 80C451—exactly the same chip as the 83C451, *sans* ROM. Both are available in 64-pin DIP as well as PLCC.

And another thing. Signetics is the only licensed alternate source for Intel's entire line of NMOS and CMOS microcontrollers. Since we have access to Intel's database, timing and instruction compatibility is assured.

Find out more about the 83C451 firsthand. Just send us the coupon, or call 800-227-1817 ext. 961D, and we'll send you a free sample, along with more detailed information.

The new 83C451 CMOS microcontroller, only from Signetics.

If you want more freedom, a little more I/O is a great way to get it.

Pass the ports! Yes, I want to know more about the 83C451. Please send me a free sample, as well as more detailed specs.

Name_____ Position_____

Company_____

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CIRCLE NO 88

3 MORE KEPCO/TDK SWITCHERS PROVE THAT LOW-PRICED DOESN'T HAVE TO MEAN CHEAP.

Our popular Series MRM — compact, multi output, PC Card switching power supplies for the logic, display, communications, and disk drive requirements of CRT terminals and microcomputers — now has five TÜV-certified members. The power range of the series has been extended to 120 Watts, as the 40-Watt MRM 144KV and the 60-Watt MRM 250KV are joined by the 80-Watt MRM 260KV and the 120-Watt MRM 270KV and MRM 280KV.

Like all Kepco/TDK switching power supplies, their prices are surprisingly low. But they offer all the most-needed features and possess all these well-known Kepco/TDK hallmarks of quality:

Hybrid microcircuits, designed and manufactured in-house, provide control, OVP, current limit, and start-up functions. They greatly reduce parts count and improve MTBF.

8mm primary-secondary, 4mm primary-to-ground spacing for the safety requirements of IEC 380/VDE 0806. All these power supplies have been certified by TÜV Rheinland, and are UL Recognized, CSA Certified.

Transformers of TDK H7C1 ferrite meet the 3750V withstand test of VDE 0806/IEC 380. All chokes also have TDK H7C1 cores.

100KHz switching for fast response, lower EMI, high efficiency, and smaller transformers and chokes.

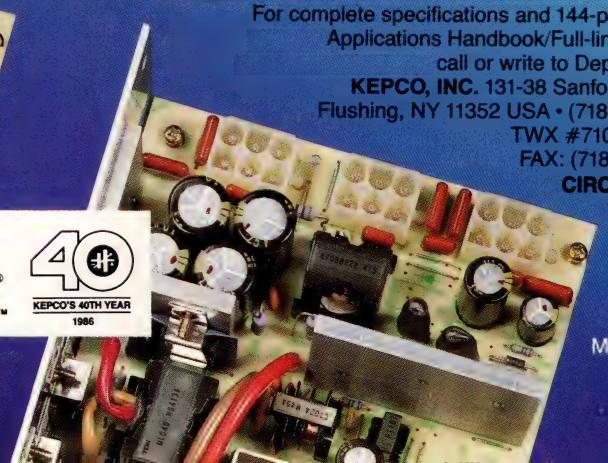
105°C input capacitors, which store enough energy for at least 20 milliseconds holding time.

Input filters of our design and manufacture attenuate conducted EMI below FCC 20780 Class B.

All components mounted on PC board by machines developed in-house.

MODEL	MRM 144KV	MRM 250KV	NEW! MRM 260KV	NEW! MRM 270KV	NEW! MRM 280KV
a-c inputs	115/230	115/230	115/230	115/230	115/230
d-c outputs					
+5V	0.45-5.0A[1]	2.0-6.0A (I_1)[2]	3.0-8.0A	3.0-15A	3.0-11A
+12V	0.3-2.5A[1]	0.5-3.0A (I_2)[2]	0.5-3.0A	0.5-5.0A[3]	0.5-5.0A
−12V	0-0.5A[1]	0-1.0A	0-0.7A	0-0.7A	0-0.5A
−5V	—	0-0.5A	0-0.3A	0-0.3A	—
+24V	—	—	—	—	0.3-1.3A (1.7A peak)
Prices*	$80	$99	$130	$185	$185

(1) The maximum combined power for all three outputs is 40W (0-50°C).
(2) Maximum current, $I_1 + I_2 = 8A$. (3) 8.0A peak.
*Substantial OEM discounts available.



For complete specifications and 144-page Kepco Applications Handbook/Full-line Catalog, call or write to Dept. HRF-12.

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THE POWER SUPPLIER™

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34010 GRAPHICS μP

32-BIT GRAPHICS

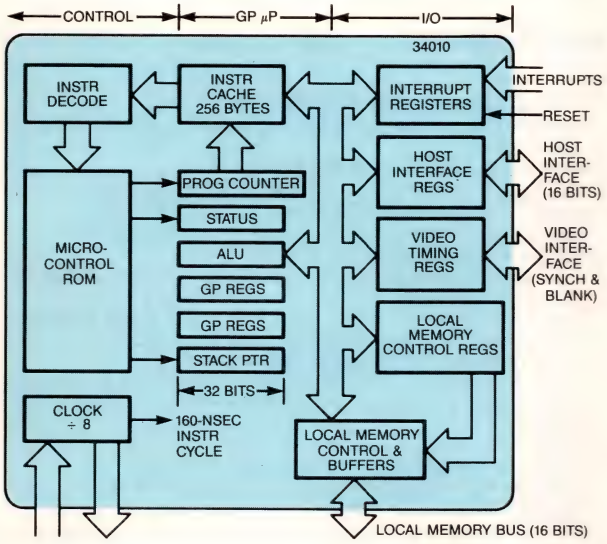
AVAILABILITY: Now for engineering samples. Production quantities scheduled for first quarter '87
COST: $155, qty 1. $50, qty 25k in '87
SECOND SOURCE: Under consideration

Texas Instruments Inc
MMP Graphics Dept
Box 1443, M/S 6410
Houston, TX 77001
Phone (713) 879-2034

Description: 32-bit CMOS μP optimized for graphics display systems but with true general-purpose von Neumann architecture so that it can be used for other applications that need the same bit manipulations necessary for pixel manipulation of CRT-type raster graphics. Features built-in instruction cache and ability to simultaneously access memory and registers. In addition to regular μP instructions, it has specialized instructions for pixel manipulation. The 1G-byte address space is bit addressable on bit boundaries using variable-width data fields (1 to 32 bits).

Status: This μP is included in directory despite its obviously specialized slant towards CRT graphics because it has a general-purpose von Neumann architecture and instruction set and some of its attributes can be equally applied to other, nongraphic applications. In particular, its ability to do rapid bit manipulation of a large local address field. TI claims there is a "great" amount of design-in activity because the 34010 is the only graphics processor that can operate totally independent from the host μP. TI applications engineers are exploring nongraphic applications.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
General-purpose μP instructions: add and subtract, multiply and divide, rotate and shift, compare and logicals
Special graphics instructions: add, subtract, and comparisons relating to XY coordinates
II—DATA-MOVEMENT INSTRUCTIONS
General purpose: move byte, move field, move register
Special graphics instructions: move X half of register, move Y half of register, pixel transfer, pixel block transfer
III—PROGRAM-MANIPULATION INSTR
Call subroutine, conditional decrement and skip, push/pop, software interrupt, return from interrupt
IV—PROGRAM-STATUS-MANIP INSTR
Has 32-bit status register (not all bits used) that can be accessed and used for program-manipulation decisions

Specification summary: A 32-bit general-purpose CMOS processor with added hardware and software features to support CRT raster graphics. Chip contains two 16×(32) registers files, a hardware stack pointer and 256-byte instruction cache. One of the 16-word register files contains the stack pointer and 15 general-purpose registers (the equivalent of the GP registers found regular nonspecialized μPs). The addressing modes of these registers is tuned to support high-level languages. The other register file is dedicated for CRT control as will be further described below in section on special graphics features.
ALU provides single-cycle, 160-nsec execution of the common integer arithmetic and Boolean operations from 256-byte instruction cache (using LRU (least-recently-used updating) algorithm). More complex instructions take multiple cycles, with signed multiply taking 20 and divide taking 40 cycles. Has 32-bit-wide barrel shifter that provides a single-cycle bidirectional shift and rotate function for 1 to 32 bits.
Has 32-bit-wide address-data bus to support a gigabyte off-chip "local" memory space. Interfaces directly to dynamic RAMs and video RAMs (including dual-port RAMs). A microcoded local memory controller supports pipelined memory write operations of variable-size fields that may be executed in parallel with ALU operations. Has separate 16-bit-wide data bus and associated control pins to interface with host μP.
The added graphics features are embodied in the second 16×(32) register file and among 28 16-bit I/O control registers. They allow programmable pixel and pixel-array processing for both monochrome and color systems of variable pixel sizes. Hardware incorporates 2-operand raster operations with Boolean and arithmetic operations, X-Y addressing, window clipping, window "pick" operations, 1- to n-bits per pixel transforms, transparency, and plane masking. Fabricated in 5V CMOS and packaged in 68-pin PLCC.

HARDWARE — SUPPORT — SOFTWARE

From TI: TMS34010 Software Development Board ($3995), which plugs into IBM PC or compatible personal computers. Used for evaluation, familiarization, and software development and comes with user interface and debug software. TMS34010 XDS/22 emulator box ($14,995) operates as a stand-alone unit with dumb terminal or with IBM PC or compatible personal computer as host.
From others: Number Nine Computer Corp (Cambridge, MA) and Vermont Microsystems Inc (Winooski, VT).

From TI: TMS34010 assembler package ($500) for IBM PC and compatibles using MS-DOS 2.11 or higher operating system and for VAX ($3000) using VMS, Unix Berkeley 4.2, or Unix System V. Includes macroassembler/linker, a source/object code archiver, and a ROM utility. The MS-DOS version also has a 34010 simulator.
A C compiler supporting full Kernighan & Ritchie C with extensions for in-line assembly code and enumerated data types. $1000 for PC; $6000 for VAX.
A graphics/math function library ($1000 for source code) provides graphics primitives, transcendental functions using double-precision floating point, matrix operations for 3-D transformations, text generation, etc.
From others: CGI standards support from Graphic Software Systems (Beaverton, OR) and Novographics International (Austin, TX).

VL 86C010 ARM

32-BIT CMOS

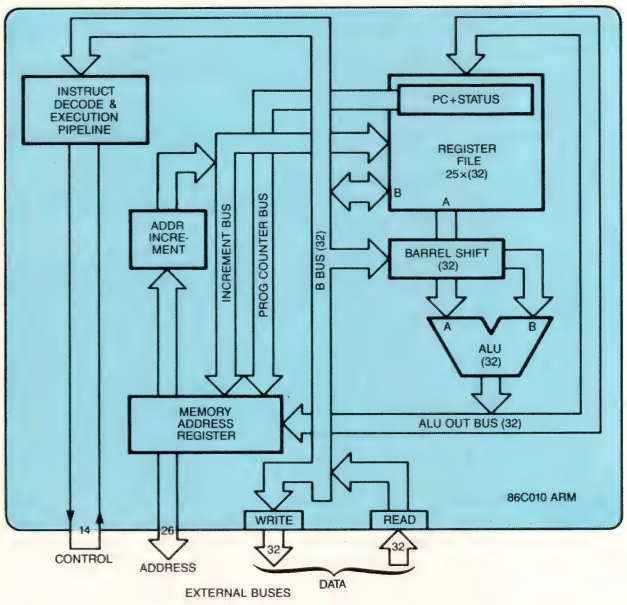
AVAILABILITY: Now
COST: $99 for samples. If successful, volume price expected to drop to $20 to $30
SECOND SOURCE: None announced
CORE: Part of VLSI's cell library. (Was in fact designed by customer Acorn Computers using VLSI semicustom tools)

Description: ARM stands for Acorn-RISC-Machine (RISC stands for reduced-instruction-set computer). The RISC architecture philosophy is that by leaving out seldom-used instructions, designers can make chips smaller and faster. Then when complex instructions are needed, they can be generated by a compiler, which in turn is supposed to be more efficient and easier to write because of the simpler instructions. Probably one of few 32-bit machines where hand-coding of subroutines would be at all feasible.

VLSI Technology Inc
Application Specific Logic Products Div
10220 S 51 St
Phoenix, AZ 85044
Phone (602) 893-8574

Status: VLSI has served as silicon foundry for this pioneering RISC μP for about a year, and in the second quarter '86, it received permission from customer Acorn Computers Ltd (Cambridge, UK) to market it. VLSI is targeting the 86C010 at controller applications because the company realizes that the device would have a slim chance in the 32-bit Unix market against such established μPs as the 68020 and 80386. VLSI hopes the small die size will give the part a price edge. Small die size should also make this a good core for semicustom, VLSI says. The 86C010 executes at 4 MIPS, but initial versions don't have multiply (difficult to implement in classic RISC because instructions aren't done in microcode), so 86C020 may suffer on number-crunching benchmarks.

HARDWARE CHARACTERISTICS SOFTWARE



Notes:
1. In addition to 86C010 μP, VLSI has associated set of chips for memory, video, and I/O (some from other μP families).
2. Note the 25 registers, which is less than on some RISC machines. But they do overlap (common in RISC) to speed interrupt service. Overlap gives automatic saving of data. But this means programmer only sees 16 at most and of those only 15 are general purpose.
3. Some provisions for memory managment including cache and virtual memory through abort signal, mode control bits, etc.

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, logicals, and comparisons. Bit clear. Shifts (barrel shifter with ALU)
II—DATA-MOVEMENT INSTRUCTIONS
Most data movements are by register-to-register instructions with option for multiple-register addressing
Only load and store operations to memory (typical of RISC)
III—PROGRAM-MANIPULATION INSTR
Skip-type decision instructions (though old fashioned, this simple approach can give fastest response in some cases)
Branch instruction has option where combined PC and status register are copied in R14 data register for quick simple return
IV—PROGRAM-STATUS-MANIP INSTR
Usual Status bits are combined with PC and mode-control bits in a 32-bit long register, which allows all three elements to be saved in one fell swoop
Notes:
1. Only 44 instructions in keeping with RISC concept.
2. Simple RISC instructions are said to ease the task of writing efficient high-level-language compilers.
3. User and supervisory modes with supervisory mode being entered by software interrupt.

Specification summary: 32-bit CMOS von Neumann (common memory) μP with RISC-style architecture. Has simple ALU with associated barrel shifter and set of 32 registers on CPU μP chip, of which 16 are accessible to programmer. Has some of the features expected in a large-memory-space machine: instructions and controls to handle virtual memory and caching. 32-bit external data bus and 26-bit external address bus allows linear addressing for external 64M-byte external memory space (can be addressed on 8-bit byte or 32-bit word basis). Only simple load and store instructions for external memory. 8-MHz 2-phase clock gives 250-nsec instruction execution time (4 MIPS) for most register-to-register instructions. Interrupt latency is 2.75 μsec max. No provisions for separate I/O addressing so I/O must be memory mapped. Fabricated in 2- to 3-μm CMOS with chip 210 mils on side. 0 to 70°C temperature range. Packaged in 88-pin JEDEC Type B leadless ceramic chip carrier and plastic leadless chip carrier.

HARDWARE SUPPORT SOFTWARE

Evaluation kit (to be available from VLSI by end of '86) and developments system available from Acorn.

From VLSI and Acorn.

IMS T212, T414, TRANSPUTER

16/32-BIT CMOS

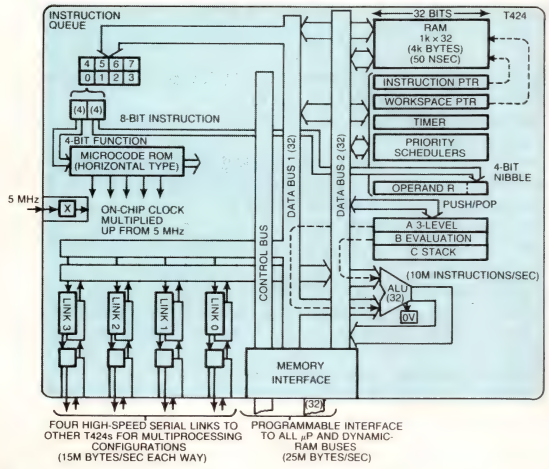
AVAILABILITY: Now for production quantities of T414 (15 and 20 MHz), T212 (17 and 22 MHz)
COST: T414-15 is $195 (100 qty), T212-17 is $156 (100 qty)
SECOND SOURCE: Negotiations with US and Japanese companies said to be in progress. Meanwhile supplier says Inmos NMB Semiconductor, Japan, can be considered an alternate source

Description: A different architecture, the Transputer is a small RISC-like machine. It has very frugal operation and operand codes made possible by heavy use of implied and indirect/relative addressing. This is said to provide fast execution of the most frequent instructions and facilitate compilation of HLLs. The ALU is fed from a shallow 3-deep stack, and the memory addressing is performed relative to a workspace pointer (with only 16 locations reached). Address offsets and literals are brought in only 4 bits at a time, which supplier says reflects the frequency of small values. Supplier claims resulting speed of local accesses more than makes up for additional instruction cycles that must occasionally be used (to load stack, set up workspace pointer, build up distant addresses, and shift in long literals).

Inmos Corp
Box 16000
Colorado Springs, CO 80935
Phone (303) 630-4000
(Designed, processed, Bristol, UK)

Status: Supplier says it has been delivering the 32-bit T414 for over a year now and that both the 15- and 20-MHz versions are available in production quantities. The 16-bit T212 has been introduced, and 17-MHz parts are being delivered. Inmos says that a number of engineering laboratories are evaluating the Transputer's potential, and that a some have committed to using it in product designs. However, some observers believe that the Transputer may be a bit ahead of its time and see its use mainly in R&D labs, where major investigations of parallel systems are receiving top priorioty. The family is still growing; Inmos announced the M212 Winchester processor, which is 16-bit 212 with Winchester/floppy controller.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Diagram is for 424. 414 same except has only 2k bytes RAM. 212 is 16-bit version. RAMless versions and μP bus adapters also.
2. Unlike most other 32-bit machines, there's no group of general-purpose registers. Instead, the substantial on-chip RAM plays an equivalent role.
3. ALU fed from small 3-deep stack, allowing implied addressing.
4. Unusually compact instruction word, especially for 32-bit machine, showing emphasis placed on short, fast instructions.
5. The four serial links allow checkerboard and pipeline arrays of Transputers in multiprocessing with no bus saturation.

Specification summary: 32-bit high-level-language-oriented μP that can be used alone but is really intended to be paralleled in multiprocessor networks. 2k-byte RAM on chip, which occupies the bottom 2k of a full 4G-byte linear address space. Four full-duplex 20M-bps serial links driven by on-chip 8-channel DMA engine for interprocessor communication in parallel networks. Also an on chip DRAM controller and a pair of timers. One 5-MHz external clock is multiplied on chip (by a PLL) to transparently generate high-speed (40-MHz) on-chip clocks, giving 50-nsec instruction cycle (also 67 and 80 nsec with different strapping). Many instructions just one cycle. Most others take no more than two cycles, except for multiply and divide and special communications and process-scheduling instructions. Multiply takes 39 cycles or 1.95 μsec, and divide takes 40 cycles or 2 μsec. Floating-point operations take from 300 to 580 cycles. T414 runs at 647k Whetstones.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic, including multiply and divide and support for floating point.
Logicals, shifts, and comparisons
II—DATA-MOVEMENT INSTRUCTIONS
Local addressing done relative to workspace pointer. Workspaces may be any size and on or off chip
Nonlocal addressing takes longer, because it must first set up
A register (in evaluation stack) as base pointer
Immediate data movement done in 4-bit nibbles, so full words will take multiple instructions and shifts
Communications instructions provide full memory bandwidth block moves and initialize on-chip DMA controllers
III—PROGRAM-MANIPULATION INSTR
Relative and conditional jumps (result of comparison instructions)
Subroutine call and return
Process creation and deletion
Process scheduling on time and comms instructions (using hardware queue pointers)
1-level interrupt (two priorities of process queue)
IV—PROGRAM-STATUS-MANIP INSTR
Test error and stop on error detect array bounds overflow and divide by zero
Process status is stored in workspace automatically with context switching via changing workspace pointer (as in TI 9000)

Notes:
1. Frugal 4-bit operation code allows only 16 basic instructions. Most of these are movement types (category II) involving one workspace-pointer-relative 4-bit address and used to push and pop data on and off evaluation stack. The prefix and negative prefix instructions allow longer words to be built up in the operand register. The operate instruction causes the data in data field to be interpreted as the opcode for zero-address instructions that manipulate stack-held data. The prefix instructions provide longer op codes for less frequent instructions.
2. Two priority-ordered process queues are each supported by front and back registers indicating a linked list containing any number of waiting processes. Real-time multitasking is directly supported in the instruction set.
3. Systems have been demonstrated in which over 100 Transputers have been running in parallel, and are said to indicate that there is linear speedup of execution as more Transputers are added. Supplier's Occam language said to facilitate programming such multiple Transputer systems, but programmer must still study out how best to partition task.

HARDWARE — SUPPORT — SOFTWARE

T414 is available as either discrete component or on a range of evaluation boards. B004 evaluation board plugs into IBM PC family machines, runs development tools, and may be used for single and multiprocessor evaluation (the T414 links for paralleling are brought out to the back panel). B007 color-graphics board simplifies output of results from evaluation system; B003 card has four T414-15s, each with 256k of memory and ideal for multiprocessor investigations and algorithm development. Item 300 and 400 are evaluation modules providing up to 400 MIPS from 10 B003 cards into 10-slot card cage.
The T212 and M212 are available on evaluation cards (B006 and B005, respectively).
Prices range from $1750 (B006-1) to $6500 (B005, including disk).
Transputer development system (TDS) for IBM PC and VAX now being shipped. Sun workstations will be supported by first quarter '87.

Inmos supplies its Occam language for transputers in lieu of assembly language. Occam is a concurrent programming language, able to make effective use of transputer's unique hardware features by directly representing multitasking, intertask messages, and interprocessor communication. Occam compilers provide close to 100% efficiency, according to Inmos because of the design of Transputer instruction set; in most applications there is no need for assembly language programming (and in fact supplier does not provide an assembler).
Inmos is delivering mixed-language development systems, allowing mixing of C and Occam at procedural level. Pascal and Fortran will be available by end of '86.
Inmos has Compuserve account that includes a electronic bulletin board and programs and documents for downloading.

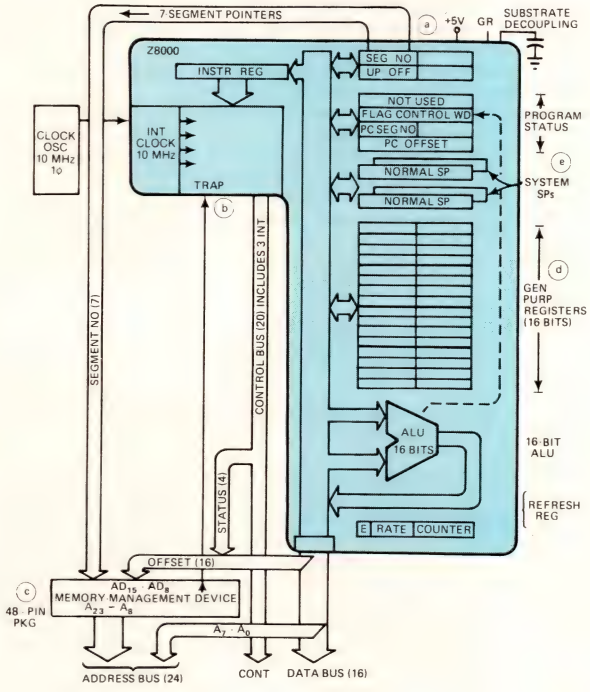
AVAILABILITY: Now for Z8000; 4, 6, 10, and 12 MHz. Fourth quarter '86 for samples of Z80000. CMOS versions in planning for '87 availability
COST: $6 to $12 for Z8000 in 1k qty. (MIL-spec versions typically run in hundreds of dollars). $165 for Z80000 samples
SECOND SOURCE: AMD (licensed), SGS (Italy and Arizona), and Sharp for Z8000. NEC for Z80000, by mask exchange

Zilog Inc
1315 Dell Ave
Campbell, CA 95008
Phone (408) 370-8000

Description: Has architecture of large mini (PDP-11) and mainframe (IBM 360/370) machines. Original 16-bit Z8000 comes in 40-pin package for addressing 64k-byte memory or 48-pin package for addressing 8M-byte memory. Said by many industry observers to be architecturally more powerful than 8086 but less powerful than 68000. Supplier says military has found it to be highest performance 16-bit μP, offering best CPU speed, interrupt-handling, and character-string search. 32-bit version, Z80000, is one of the most advanced NMOS μPs. It has many features formerly associated only with superminicomputers and mainframes.

Status: The Z8000 has, according to Zilog, found most acceptance in real-time control applications, particularly military. Dataquest figures for '85 show the Z8000 reached a unit volume of 372k units, or about 4½% of the 16-bit-μP market. This was greater than the National 32016's unit volume, though much less than either the 8086 or 68000 families. The Z80000 is a much-delayed, full 32-bit enhancement of the Z8000 that remains object-code compatible with the Z8000. Supplier has run silicon on Z80000 but says it needs more iterations to achieve speeds competitive with other 32-bit μPs. The supplier expects the Z80000 to follow the Z8000 in the military and control markets. Supplier says it's committed to having CMOS versions but doesn't expect them to appear before '87 or '88.

HARDWARE — SUPPORT — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic including add, subtract, decimal adjust, increment, decrement, multiply (signed), divide (signed)
Logical including AND, OR, exclusive OR, compare, test, complement, rotate, and shift (by n)
Operations can be on bit, BCD nibble, byte, 16-bit word, or 32-bit double word and can use any of the 16 general-purpose registers as accumulator

The Z8070 floating-point processor will do IEEE-754 operations
II—DATA-MOVEMENT INSTRUCTIONS
Eight addressing modes using general-purpose registers as indexers and stack pointers
Comprehensive set of block-transfer and string-manipulation macro-equivalents, including many dedicated to I/O space
III—PROGRAM-MANIPULATION INSTR
Call and call relative (±4096 bytes)
System call using special system stack pointer
Jump conditionals
IV—PROGRAM-STATUS-MANIP INSTR
Set and reset flags, complement flags. Set-multiple-interrupt modes
Tests for the Micro In and Micro Out lines for multiple-microprocessor configurations
V—SYSTEM-CONTROL INSTRUCTIONS
The 80000 has priveleged instruction for exclusive use by an operating system

Specification summary: Common-memory architecture with optional separate I/O space and separate "systems" stack. The 16-bit 8000 μP has directly addressable memory space of 8M bytes (8001, 8003) using segment pointers, expandable to 48M bytes using the six available memory spaces and an MMU. Executes 110 basic instructions with 410 combinations at speeds ranging from 0.30 μsec through 1 or 2 μsec to 7 μsec for 16-bit multiply, all at 10-MHz system clock (4 and 6 MHz also available). Eight large-computer-style addressing modes plus unusually large repertoire of block and string operations. NMOS device requires one 5V supply (plus substrate-decoupling capacitor) in either 40- or 48-pin package. The Z80000 is a 32-bit upward-compatible version of Z8000 and can run same software. 6-stage pipelining of instruction fetch/execute cycle and 256-byte on-chip associative cache for instructions and data for improved performance (and use of 100- to 120-nsec memories). Also on-chip MMU for virtual memory with address bus a full 32 bits for 4G-byte memory space. Expected to use 25-MHz clock for 12.5-MHz (80-nsec) instruction cycles, which will give 12.5-MIPS burst rate (when doing loops out of cache). Expected to run at 5 MIPS continuously (4 MIPS with MMU virtual memory translation). 16×16 multiply in 1.2 μsec and 32×32 in 1.9 μsec. 2-μm NMOS dissipating 3 to 4W. Will be in 68-pin leadless chip carrier or PGA. (Japanese sources, NEC and Sharp, may help with future introduction of CMOS version.) Companion Z8070 floating-point coprocessor will implement the IEEE-P754 format. The 8070 is pipelined so 80000 CPU can continue to be bus master and feed in data while 8070 is computing.

HARDWARE — CHARACTERISTICS — SOFTWARE

From Zilog: System 8000 development system with 32M-byte hard disk and 17M-byte cartridge tape drive ($27,000), Z-Scan 8000 in-circuit emulator ($5500), EMS 8000 in-circuit-emulator subsystem ($13,000), Z8000/Z8001 DM (development module) stand-alone board ($1500/$1795). 500-pg Z8000 technical manual available.

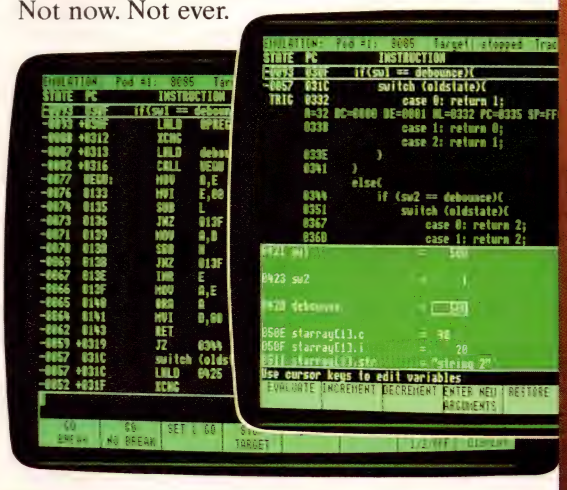
From Zilog: Zeus multiuser operating system for System 8000. This is Zilog's enhanced Unix (Bell Labs) operating system and comes with more than 100 utilities, including screen editor, Fortran, Pascal, C, and PLZ/SYS compilers.
From others: A real-time executive from Hunter & Ready (Palo Alto, CA), VRTX/8002, suited to embedded applications, and an Ada compiler developed by Irvine Computer Science Corp (Irvine, CA) for Zilog, selling for $8000 to $14,000 per copy.

Echo: What high level source code debugging should have been from the beginning.

Nobody does what our μP development system does: lets you debug in high level while emulating at full speed; then a single keystroke gets you down to gut level to view C *and* assembly language.

It's what you should have been able to do from the beginning but couldn't until Arium Echo redefined microprocessor development systems in terms of performance and price. That's why, at $9980, this 16-bit, true multitasking, UNIX-compatible system delivers more power, more speed and more menu-driven features than the HP 64000 system costing four times as much. Features like on-screen time stamping, super high speed C and Pascal compilers, and Arium's Proprietary Code Preview™ that lets you see where your code is going, as well as where it's been.

Echo is a multi-user system; but so affordable, every engineer could have his own. No sharing, no waiting, no lost man-hours. Just all the resources you need at your fingertips. One call now to the Arium Hot Line, **(800) 862-7486,** will give you all the reasons why when it comes to performance and price, nobody echoes Echo. Not from the beginning. Not now. Not ever.



CIRCLE NO 90

ARIUM CORPORATION

1931 Wright Circle
Anaheim, CA 92806
(714) 978-9531

68000 — 8/32-BIT, 16/32-BIT, 32/32-BIT NMOS AND CMOS

AVAILABILITY: Now for 12.5-MHz 68000, 68010, 68012, 68020, 68881 (floating point), and the 68851 (memory unit). Now for 16.67-MHz 68020, 68881, and 68851. Now for 20-MHz 68020 and 68881. Now for 25-MHz 68020. 68008 with 8-bit external data bus is also available

COST: In 100 qty, $11 for 8-MHz 68008; $10 for 8-MHz 68000; $23 for 8-MHz 68010; $306 for 12.5-MHz 68020; $240 for 12.5-MHz 68881; $306 for 12.5 MHz 68851. $771 for 20 MHz 68020

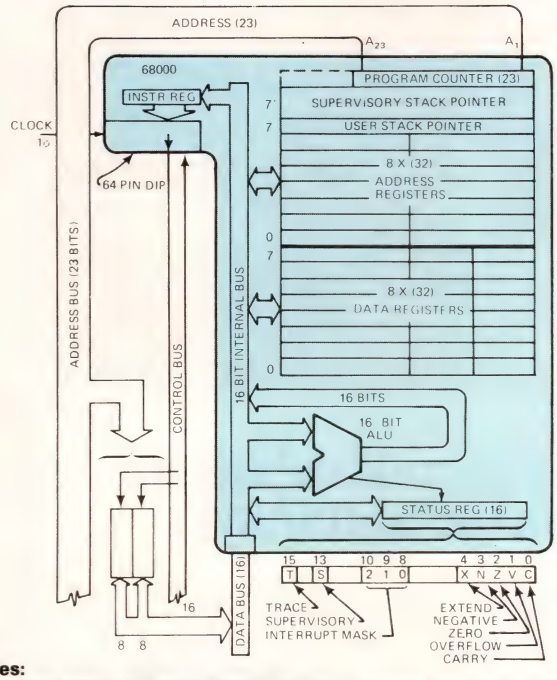
SECOND SOURCE: Rockwell, Hitachi, Mostek, Signetics/Philips, and Thompson Semiconducteurs, all licensed with mask interchange for 16-bit parts. Thompson Semiconducteurs, initial second source for 32-bit 68020, is scheduled to have parts in '87. (Hitachi R&D has made a 32-bit device similar to the 68020 but has not announced plans to market it)

Description: Family based on a modern minicomputer architecture using a basic group of 16 fairly general, 32-bit registers. The members of the family have various addresses and data-bus widths and different ALU widths. The bottom of the line, the 68008, has a narrow 8-bit data bus. The middle member, the 68000, has a midsized 16-bit data bus and ALU and 24-bit addressing. The top-of-the-line 68020 is full 32 bits throughout.

Motorola Integrated Circuits Div
3501 Ed Bluestein Blvd
Austin, TX 78721
Phone (512) 928-6000

Status: The 32-bit 68020 has been (along with DEC's VAXs) the target for comparisons for all 32-bit μPs. As of late summer '86, 100k units of the 68020 have been shipped (according to Motorola and Dataquest), which gives the 68020 the leading position in the 32-bit-μP race. Only the Intel 80386 can project a customer base that will be close to the 68020's 1-year-plus head start. Motorola is working hard to maintain its lead over the 80386 by upgrading 68020 performance (the 68020 is now at 25 MHz) and by planning future enhanced models, the 68030 and 68040, which will have larger, more sophisticated on-chip caches and will solve the problem of limited bus bandwidth by either separate address and data buses or perhaps by using a large 64-bit bus. Meanwhile, the reportedly growing success of the Apple Macintosh personal computer gives the whole 68000 family a higher volume production base that will assure its longevity, just as the huge success of the IBM PC has given the 8086 family assured longevity. Most of the early 68020 customers are designing workstations.

HARDWARE — SUPPORT — SOFTWARE



Notes:
1. Diagram favors the basic 68000, which—although it has 32-bit wide registers—has 16-bit-wide ALU and data buses and only 23-bit-wide address bus. It comes in 64-pin DIP, 68-pin grid array, or TCC.
2. Bottom-of-the-line 68008 has only 8-bit data bus and 20-bit or 22-bit address bus. It comes in 48-pin DIP or 52-pin LQP.
3. Upper-range 68010 and 68012 are similar to 68000 but support virtual memory. The 68010 has 24-bit address bus and comes in a 64-pin DIP or 68-pin grid array. The 68012 has full 32 bits of address and comes in 84-pin grid array.
4. Top-of-the-line 68020 is full 32 bits throughout, including ALU and address and data paths. Additionally, it has 256-byte instruction cache on chip. It's fabricated in CMOS and comes in 144-pin grid array.
5. Two important support chips, not shown, are the 68881 floating-point coprocessor and the 68851 memory-management unit. Both are in CMOS.
6. The 68070 by Philips/Signetics includes various support functions on chip. It's scheduled for fourth quarter '86 or first quarter '87.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic including multiply and divide (signed and unsigned)
Logicals and rotates and shifts
Can handle bits, BCD nibbles, bytes, short (16 bits) and long (32 bits) words

II—DATA-MOVEMENT INSTRUCTIONS
Five basic address modes are register direct, register indirect, immediate, absolute, and program-counter relative. To these modes can be added postincrementing, predecrementing, offsetting, and indexing
Can use eight 32-bit address registers as indexers or stack pointers. The eight 32-bit data registers can also serve as indexers

III—PROGRAM-MANIPULATION INSTR
Branch and jump to subroutine. Branch conditionally
Link and unlink instructions invoking one address register as frame pointer (used to establish temporary local environments in structured programming)
Seven levels of priority interrupts, including nonmaskable, with 256 possible interrupt vectors

IV—PROGRAM-STATUS-MANIP INSTR
16-bit status register is software accessible
Sophisticated trap operations help user debug programs
Trace mode

V—SYSTEM-CONTROL INSTRUCTIONS
Privileged instructions for operating systems and multiprocessor communication

Specification summary: 68020: full 32-bit CPU version of the 68000 family that's object-code compatible with all members. Has 16 32-bit general-purpose data and address registers, 32-bit ALU with barrel shifter, and 32-bit data bus. Also has full 32-bit address bus that can reach 4G bytes of direct linear external memory. Supports instruction-continuation-type virtual memory. Has 256-byte instruction cache on chip and 3-stage pipelining. At 25-MHz maximum clock, executes 5 MIPS. For tight inner loops with so few instructions that they can be contained in cache, and when data can be contained in registers, will operate at burst modes to 12 MIPS. With 68881, it can run at 1.25M Whetstones. Has 18 addressing modes and instructions to support structured high-level languages and sophisticated operating systems. Fabricated in 2-μm CMOS with 1.5W power dissipation and packaged in 144-pin grid array.

HARDWARE — CHARACTERISTICS — SOFTWARE

VME/10 OEM μC system that can be configured as a software-development workstation or an OEM system. Benchmark-20 System package, a 32-bit package that provides the first-time user of 68020 a tool to evaluate 68020 and start writing code. HDS-300 hardware/software development station provides real-time emulation of the 68000 family μPs with bus-state-analyzer support and source-level debug. MEX68KECB educational computer board is based on 68000. VM04 is a 68020-based 32-bit Versamodule interconnected within a target system using the 32-bit, asynchronous, Versabus interconnect standard. VME130 is a 68020-based 32-bit VME module using Eurocard mechanical format.

VersaDOS real-time operating system, System V/68 operating system, CP/M-68K operating system, concurrent DOS-68K operating system, and VRTX real-time operating system. Unix support from Motorola includes direct ports of Unix V, AT&T. X-assembler for Exormacs and VME/10, X-"C" compiler VME/10, and Exormacs for VAX/780 are available.
Considerable third-party software support is available for family. For example UniPlus+ Unix V from Unisoft (Berkeley, CA) and 68000 family symbolic debugger from Boston Systems Office (Waltham, MA). Motorola Microprocessor Software Catalog BR126 describes the software available and vendors that support the 68000 family.

SERIES 32000

8/32-BIT, 16/32-BIT, 32/32-BIT NMOS AND CMOS

AVAILABILITY: Most devices now available in production quantities at 6, 10, and 15 MHz. CMOS versions of most devices are also available, except for the 32532 CMOS enhancement of NMOS 32332, which is still promised for '87
COST: In 100 qty, $195 for 10-MHz 32332; $30.95 for 6-MHz 32032; $14.95 for 6-MHz 32016; $12.50 for 6-MHz 32008; $17.75 for 6-MHz 32081 FPU; $13.55 for 6-MHz 32082 MMU
SECOND SOURCE: Texas Instruments (TI has cut back on its 32000 effort, dropping plans to do CMOS versions and no longer wishing to be listed for hardware and software support)

Description: A core 32-bit μP in which various models bring out different sized address and data buses. The core processor has acquired reputation even among competitors for being "elegant" in its symmetry: ie, its instructions and addressing apply quite regularly to all registers, which supplier claims makes high-level-language compilers easier to write. It is intended to match the needs of operating systems like Unix and to have big-computer features expected of 32-bit systems, such as demand-paged virtual memory, protection of operating system from users, and protection of one user from another user.

National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95051
Phone (408) 749-7432

Status: The "only 32-bit μP around" status that this early supermini-like machine has enjoyed is now over. Not only has Motorola's 68020 been out for over two years, but Motorola has announced its more powerful 68030. Perhaps equally troublesome for National, Intel's 80386 is finally real. Then there are the 32-bit machines from AT&T, Fairchild, Zilog, and Inmos. All these competitors are in CMOS, while the full 32-bit 32332 (32-bit data and 32-bit address) is still in NMOS. They are also faster; the 25-MHz 68020 is much faster, and by Intel's claims, the 80386 also is faster. But National has used its early lead with the 32000 to advantage and has a number of design commitments, many in Unix-based engineering-workstation applications. A comparison of National's prices against the prices for the competing 32-bit devices shows that National does offer the lowest cost components for 32-bit systems.

HARDWARE — CHARACTERISTICS — SOFTWARE

SEE EDN, NOVEMBER 28, 1985, PG 180, FOR BLOCK DIAGRAM AND NOTES.

5 CHIP SET	PART NO.	DESCRIPTION	BUS WIDTH			TECHNOLOGY	AVAILABILITY	COMMENTS
			INTERNAL	EXTERNAL ADDR	EXTERNAL DATA			
	32008	CPU	32	24	8	NMOS	NOW	
1	32016	CPU	32	24	16	NMOS	NOW	
	32C016	CPU	32	24	16	CMOS	SAMPLES	FIRST CMOS PART
	32032	CPU	32	24	32	NMOS	NOW	
	32C032	CPU	32	24	32	CMOS	SAMPLES	
	32132	CPU	32	24	32	NMOS	NOW	DUAL PROCESSOR 2 SETS REGS, 1 ALU
	32332	CPU	32	32	32	NMOS	NOW	FAMILY FLAGSHIP
	32C532	CPU	32	32	32	CMOS	'87	NEXT GEN WITH CACHES, MMU, ICU
4	32081	FPU	64	—	16	NMOS	NOW	FLOAT-PT SLAVE
3	32082	MMU	—	24	16	NMOS	NOW	MEM-MAN SLAVE
2	32201	TCU	—	—	—	BIPOLAR	NOW	SYSTEM CLOCK
	32C201	TCU	—	—	—	CMOS	NOW	SYSTEM CLOCK
5	32202	ICU	—	—	8/16	NMOS	NOW	INTERRUPT
	32382	MMU	—	32	32	NMOS	NOW	2ND-GEN MMU
	32381	FPU	64	—	32	CMOS	1Q'87	CMOS FPU WORKS WITH 332 AND 532 CPUs
	32C081	FPU	64	—	16	CMOS	1Q'87	CMOS FPU
	32301	TCU	—	—	—	CMOS	1Q'87	2ND-GENERATION SYSTEM CLOCK

I—DATA-MANIPULATION INSTRUCTIONS
All instructions operate on either 8-, 16-, or 32-bit data and can be accessed by any appropriate addressing mode. Multiply and divide, BCD arithmetic, logicals, and bit manipulation throughout memory space and CPU registers
II—DATA-MOVEMENT INSTRUCTIONS
Intelligent string operations and bit-field handling allow efficient movements
III—PROGRAM-MANIPULATION INSTR
Stack- and frame-pointer instructions suitable for high-level languages (including Polish notation). Modular software support via special CPU hardware (Mod register) and tables automatically implemented for indirect addressing of position-independent ROMs, etc. Array instructions
IV—PROGRAM-STATUS-MANIP INSTR
Status registers in slave processors and MMU as well as in CPU, with both privileged and user access

Specification summary: 32-bit "maxi-mini"-type pipelined architecture implemented in multichip NMOS VLSI. Uniform addressing of up to 4G memory locations. Instruction set chosen to match operations needed by high-level-language compilers. All instructions can symmetrically apply to all data types (8, 16, and 32 bits, etc) and all register and memory locations. 10-MHz bipolar clock drives CPU directly, giving 100-nsec machine cycles, with instructions requiring 0.3 to 7.6 μsec (most in 1- to 2-μsec range). With floating-point CPU extension, can perform 32×32 multiply in 9 μsec. XMOS 2.4-μm-gate processing with relatively large (250 to 300 mil^2) chips, requiring one 5V supply. Housed in packages with 24 to 48 pins. The 32032 is housed in a 68-contact leadless chip carrier.

HARDWARE — SUPPORT — SOFTWARE

From National: Series 32000-based native development system, VR32. Target/Development system with Unix System V/Series 32000 operating system ($14,450) has been well accepted, supplier says. Also a PC add-on development solution (SYS32/20) that will convert IBM XT/AT into a Series 32000-based native development environment (complete kits from $3500). In-system emulation by ISE32 ($12,900) to run on VAX/VMS, VAX/Unix (4.2), VR32/Unix (System V) and SYS32/20 (System V). Development/evaluation boards based on 32016, 32032, and 32332 are also available from National and from other suppliers (contact National for list) from $695 to $9,900.
National is offering very-low-cost evaluation kits: one containing 32016 μP for $59 and one containing 32032 μP for $75. In addition to other support devices, these kits contain a "tiny development system (TDS)" in PROM and Pascal program listing that will let users download from personal computers.

From National: Supplier's 405-pg *Series 3200 Software Catalog*, Summer 86, is best guide to available software support. Among others it lists compilers for C, Pascal, Fortran, Cobol, Forth, Modula-2, Lisp, Prolog, Algol, Basic, BCPL, AVL, SMPL, and ISIL. Supplier has a Genix 4.2 based on Berkeley 4.2 and Genix V.3 based on AT&T System V. Also for tool support the supplier offers the GNX language tools, which contain C, Fortran 77, and Pascal compilers for VAX/Unix or VAX/VMS or environments. Available for real-time multitasking applications, VRTX/Series 32000 and Exel for multiple environments.

WE32 FAMILY

32-BIT CMOS

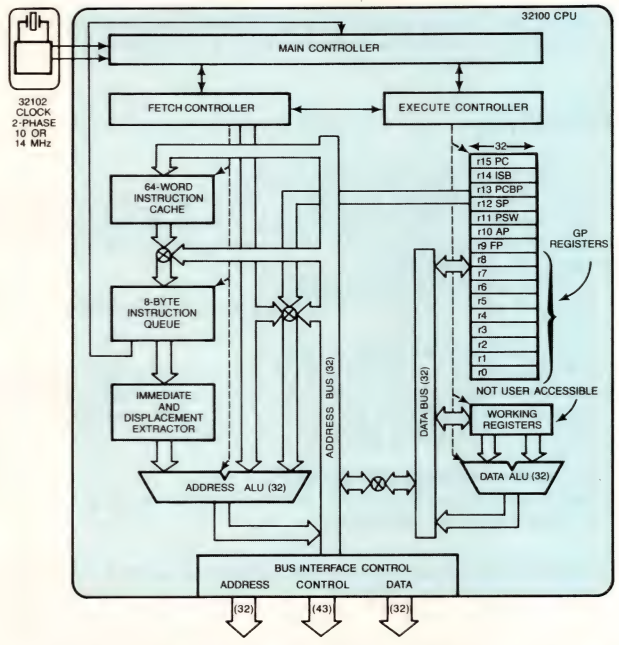
AVAILABILITY: Now for WE32100. 1987 for WE32200 (see table)
COST: $120 for 10-MHz 32100 CPU, 1k qty (see table for others)
SECOND SOURCE: Zilog for 32100. To be announced for WE32200

Description: CMOS chip set for building top-of-the-line, minicomputer-like computing systems. Provided with depth of Unix operating-system support, so it should be suited to multiuser/multitasking applications. Forthcoming family upgrade (32200) to have higher performance.

AT&T Technologies Inc
Dept KB
555 Union Blvd
Allentown, PA 18103
Phone (899) 372-2447

Status: This chip set is worth studying because it represents what a major, broad-based technology leader considers the correct direction to go for future large μP-based computing systems, especially those centered on the Unix operating system. AT&T says it develops the newest versions of UNIX on the chip set. So far there's been no indication that this chip set will displace the leaders among 32-bit μPs—Motorola's 68020/30 and Intel's 80386—but the WE32 chip set has been given a nice start by AT&T using it internally (in the "tens of thousands") for the company's 3B computers and embedding the chips in AT&T telecomm equipment.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Fairly complete arithmetic, logical, and bit-manipulation instructions (including 2- and 3-operand instructions)

II—DATA-MOVEMENT INSTRUCTIONS
Wide variety of addressing modes that support high-level language constructs (eg, arrays, structures) and allow manipulation of byte, halfword, word (32-bit), floating-point, BCD, and string data types. Also supports bit field manipulation. All instructions can be used in any addressing mode with any data type allowing programming and compiler design flexibility

III—PROGRAM-MANIPULATION INSTR
Large selection of conditional branches. Conditional returns from subroutines. Call and return from procedures, which automatically update execution stack, providing efficient procedure linkage

IV—PROGRAM-STATUS-MANIP INSTR
The 32-bit status register contains 26 bits of status information that covers not only the ALU condition codes of smaller μPs but information that relates to exceptions, interrupt mask level, execution level, cache control, etc

V—SYSTEM-CONTROL INSTRUCTIONS
Operating system instructions that allow efficient process switching and system calls (privileged and nonprivileged). Breakpoint, trap, and cache flush instructions

Notes:
1. Software compatible with AT&T's previous 32-bit μP, the WE 32000.
2. There are four levels of execution privilege: kernel, executive, supervisory, and user.

PART NUMBER	TYPE	DESCRIPTION	SPEED MHz	PACK-AGE PINS	AVAIL-ABILITY	COST (1k QTY)
WE 32100	CPU	32-BIT MICROPROCESSOR	10 14 18	132	NOW NOW NOW	$120
WE 32101	MMU	MEMORY-MANAGEMENT UNIT	10 14 18	132	NOW NOW NOW	$115
WE 32102	CLOCK	2-PHASE CLOCK	10 14 18	16	NOW NOW	$27
WE 32103	DRAMC	DYNAMIC RAM CONTROLLER	10 14 18	132	NOW NOW NOW	$55
WE 32104	DMAC	DIRECT MEMORY ACCESS CONTROLLER	10 14 18	132	NOW NOW NOW	$125
WE 32106	MAU	MATH-ACCELERATION UNIT	10 14 18	100	NOW NOW NOW	$120
WE 32200	CPU	32-BIT MICROPROCESSOR	20 24 28		1Q'87 1Q'87 1987	
WE 32201	MMU	MEMORY-MANAGEMENT UNIT	20 24 28		1Q'87 1Q'87 1987	
WE 32206	MAU	MATH-ACCELERATION UNIT	20 24 28		1Q'87 1Q'87 1987	

Specification summary: Set of 5 devices (see table) intended for large-memory, minicomputer-like, 32-bit systems. The 32100 CPU features separate addressing and data execution sections each with 32-bit wide buses. A 64-word instruction cache followed by an 8-byte instruction queue control a 3-deep pipelined execution unit. Performance can be maintained at 3 to 4 MIPS. The 32100 CPU is augmented by four VLSI support chips (see table): The 32101 MMU provides support for 4G bytes of virtual memory and incorporates both demand-paged and -segmented approaches. The 32103 DRAMC addresses 16M bytes of dynamic RAM, supporting the newest 1M-bit devices and incorporates refresh control, etc. The 32104 DMAC handles 32-bit address generation for rapid memory-to-memory data transfers (13.1M bytes/sec) and has additional 8-bit-wide bus for efficient transfers to slower peripherals. The 32106 MAU is a coprocessor that executes IEEE floating-point math, allowing the 32100 system to achieve 1.4M Whetstones/sec. Chip set is fabricated in 1.5-μm twin-tub CMOS (32100 CPU consumes 0.8W) and comes in ceramic grid array packages (see table).
The 32200 chip set provides a system solution for board designs in the 20- to 30-MHz range. Performance up to 8 MIPS and 4M Whetstones/sec.

HARDWARE — SUPPORT — SOFTWARE

WE321DS development system that includes WE321AP analysis pod ($22,500 for 10 MHz) in-circuit emulation of 32100 and 32101. 14 MHz also avaialble. WE321 device monitor provides signal observation of high-speed 32100 systems. WE321EB evaluation board ($5500 at 10 MHz, $6500 at 14 MHz) with 32101 MMU and 32106 math accelerator. WE321SB single-board computer with VME Bus. Runs latest version of Unix V, operates at 14 MHz, and contains CPU, MMU, and MAU.

WE321SG software-generation programs run on host Unix systems. Includes C compiler, assembler, linking editor, and optimizer. Prices range from $500 to $7,000. Also compilers for Fortran, Cobol, Lisp, Basic, and Ada. Over 1000 end-user programs including Informix, dBASE II, and Multiplan have been developed for the chip set, according to AT&T.
AT&T provides a range of Unix licensing arrangements from $60 for binary sublicense for a 1- or 2-user situation to $43,000 for an initial license for source code (substantial discounts for educational users).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OR SECOND
IN THE MARKET...

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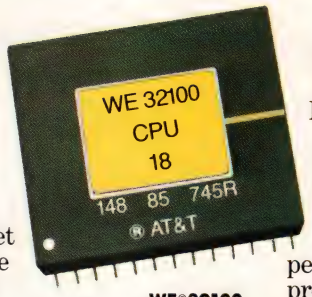

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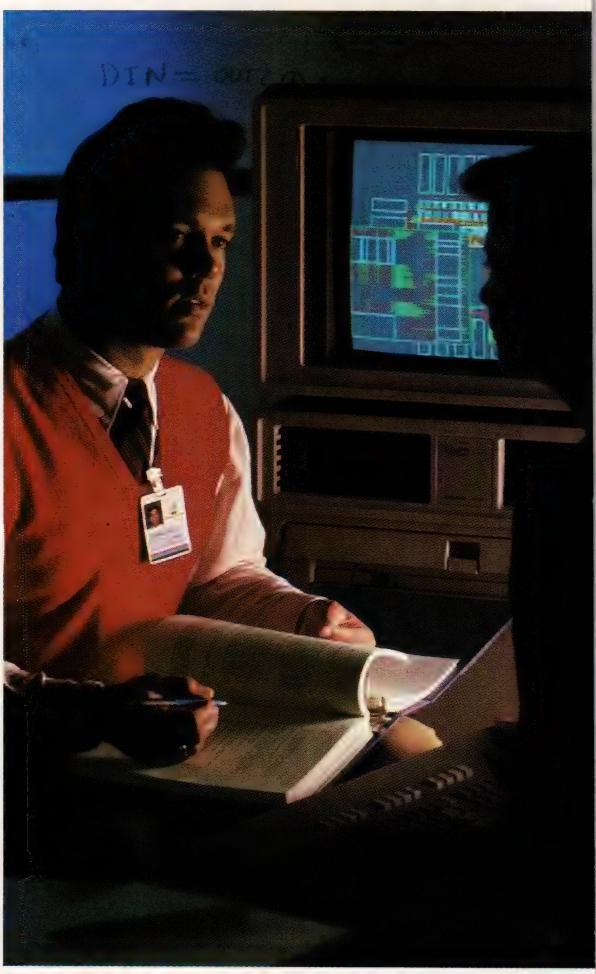

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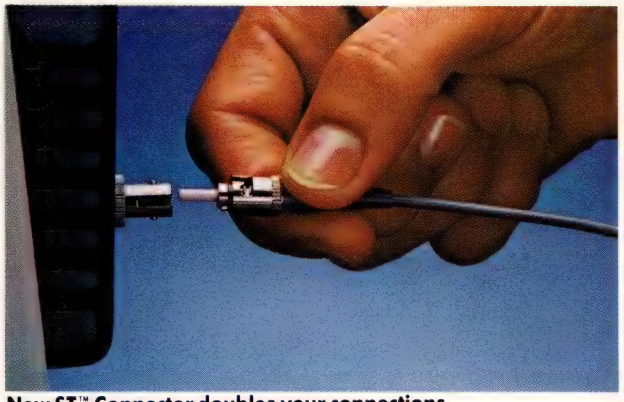

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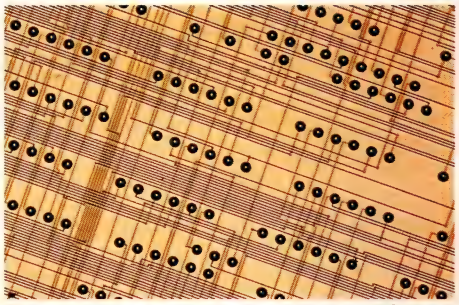

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CIRCLE NO 92

CLIPPER

32-BIT CMOS

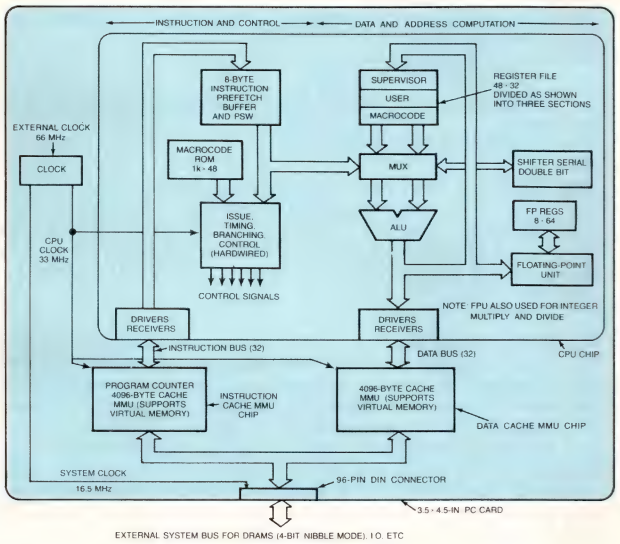
AVAILABILITY: Now
COST: $1200, 1000 qty for basic 3-chip set on card with clock. Chips will be sold separately in '87, with some price reductions should volume grow
SECOND SOURCE: None announced

Description: CMOS chip set intended to run Unix-based software at state-of-the-art speeds (5 to 33 MIPS). CPU has a RISC flavor with streamlined instruction set and a large number of registers. But the basic RISC frugality is augmented with on-chip floating point and two cache/MMU chips: one for instructions and one for data. Because the dual caches are large (for μPs), the Clipper is said to achieve 90% hit rates and sustain 5-MIPS average performance at 33-MHz clock. With 100% cache hits, bursts of 33-MIPS can be achieved.

Fairchild Advanced Processor Div
Fairchild Semiconductor Corp
4001 Miranda Ave
Palo Alto, CA 94304
Phone (415) 858-4249

Status: Reception for this chip set has been favorable. Even some of the competitors have acknowledged that it represents about the best of 32-bit state of the art. Designer and project leader Howard Sachs says that interest has come from designers of workstations, communication controllers, and factory automation equipment who need a performance edge to differentiate their products. Regarding Clipper's viability, Sachs says he hopes to achieve a 100k sets/year volume, which at $500 per chip set will produce the $75M to $100M annual revenues a 32-bit project needs to keep advancing. The general public may be introduced to the Clipper in '87 via plug-in cards for the IBM AT. Several OEMs are working on such boards. Sachs says the Clipper chip set produces the lowest cost, general-purpose 5-MIPS accelerator; competing μPs such as Intel 80386 or Motorola 68020/30 need more external help from larger caches and floating-point-math units, elements that are built into the Clipper chip set. By the time 4M- to 16M-bytes local memory (150-nsec DRAMs) are added, only a Clipper system could fit on a single PC board, he says.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Clipper will initially consist of three CMOS chips, all approximately 440×440 mils. They will be fabricated in 2-μm CMOS with two levels of metallization.
2. The CPU chip has what Fairchild calls a streamlined instruction set architecture—it will decode its instructions by hardwired logic rather than the more usual microcode ROM. It has an usually large number of registers on chip (48×32). But because some instructions are not suited to the RISC approach, it has a 1k×48 microcode ROM for sequences of instructions such as string moves.
3. The other two chips will be identical pin-programmable cache/MMU chips, so one can be used for instruction caching and the other for data caching. The instruction cache will carry the CPU's PC (instruction program counter). The 4096-byte capacity of each cache (large for μPs) plus the sophisticated caching control (2-way set associative) gives the Clipper a high hit ratio (over 90%), a key factor for sustained execution speed.
4. Each cache will support virtual memory via the on-chip MMU. The caches (especially the data cache) will operate on a physical memory basis, so less flushing is needed.
5. Sophisticated pipelining (upper pipe including prefetch, fetch, decode, and resource menanagment) and lower pipe, including a 3-stage pipelined execution unit, is used on CPU, but with provision for bypassing so that an instruction can obtain the result of a preceding instruction without delay.

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, multiply, and divide (both 32-bit integer and 32- and 64-bit IEEE floating point done in floating-point unit), floating-point converts, negate, compare, logicals, including AND, OR, EXCL OR, and NOT
32- and 64-bit shifts and rotates, including floating point
II—DATA-MOVEMENT INSTRUCTIONS
Architecture favors register-to-register operations and avoids operations on memory other than register-to-memory movements. Nine addressing modes, including absolute, relative (with and without displacements), relative indexed, and PC indexed. Despite streamlined instruction set, architecture provides efficient string moves, because execution control is switched over to macrocode ROM
III-PROGRAM-MANIPULATION INSTR
Macrocode ROM is used for context switching save and restore instructions that support entry and exit from interrupt and trap routines
PUSH, POP, supervisor, and user stacks (any register can be used as pointer)
IV—PROGRAM-STATUS-MANIP INSTR
Two status words, a user program status word and a privileged system status word (which can only be written in supervisory mode)
V—SPECIAL INSTRUCTIONS
Supervisory mode commands. Hardware supports 18 hardware traps and 128 supervisory calls. Software semiphores are supported for multitasking
Notes:
Architecture is based on a balance between RISC and CISC concepts. There are 168 instructions. The macrocode ROM contains some of the more desirable complex instructions found in regular microcoded μPs, such as floating/integer conversion, character string manipulation, save and restore registers, and trap/interrupt entry and return sequences.

Specification summary: Modified RISC-type architecture in which the basic frugal RISC instruction set is supplemented with boost from microcode ROM, giving 168 instructions. The bus-bandwidth bottleneck is solved by having separate buses for instruction and data and putting a cache/MMU chip on each bus. Putting the caches on separate chips allows them to be large enough to generate high hit rates (greater than 90%). Partitioning also allows IEEE 64-bit floating point to be incorporated on CPU chip so there is no off-chip delay (as when going to an external coprocessor). CPU doesn't need to have a separate multiply-divide hardware because these operations can be done in the floating-point unit. Performance is projected to be 5 MIPS average with 33-MHz CPU clock (33 MIPS peak). The three chips are fabricated in 2-μm CMOS and may be sold mounted on a 3.5×4.5-in. PC card with 96-pin DIN connector.

HARDWARE — SUPPORT — SOFTWARE

The Clipper Module card integrates the three Clipper chips into a functioning CPU. It provides the clock and PC wiring and a 96-pin DIN connector. User must provide the bus buffers externally. Manual on module specifications and architecture.
Also to be available, by end of '86 from third parties, a functioning Clipper system, complete with memory, on a plug-in card for IBM AT.

Clipper Cross Support Package that runs on VAX ($8000) and MicroVAX-II ($6000). Consists of three elements: standard Unix System V development tools; optimized C, Fortran, and Pascal compilers, assembler, linker, and debugger; and a complete simulation environment including software simulator, timing analyzer, and instruction profiler.
Clipper Cross Support Package Reference Manual (which includes C implementation manual), user's manual, CLIX operating system manual, and Fortran and Pascal manuals.

8X305, 8X400 MICROCONTROLLER

8-BIT BIPOLAR

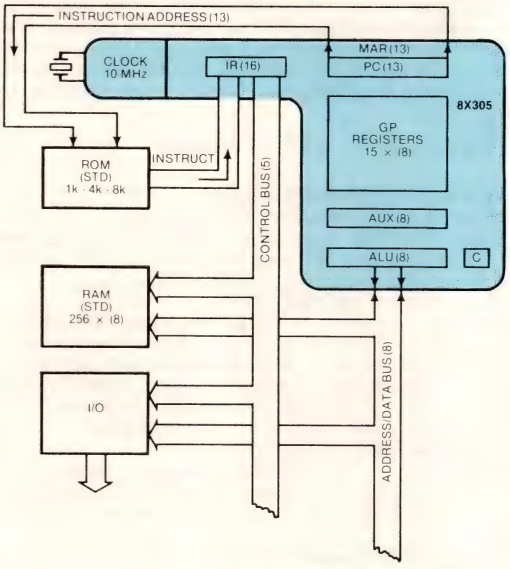
AVAILABILITY: Now for all 8X305 parts and for some 8X400 parts
COST: $22 (100 qty) for 8X305A ($29.70 in ceramic package), $75 for 8X401
SECOND SOURCE: AMD (has announced availability of 8X305 numbered as 29X305A)

Description: The 8X305 is upwardly compatible with the original 8X300 and housed in the same oversized package, but with its 200-nsec cycle time, this single-chip, 8-bit bipolar processor can work in real time in high-speed data paths such as those in floppy disks, digital communications, and some industrial control. Newest family member, the 8X400, has 100-nsec instruction cycle. It gets its speed from new oxide-isolated 3-μm bipolar process with ECL internal circuitry.

Signetics Corp
811 E Arques Ave
Sunnyvale, CA 94086
Phone (408) 739-7700

Status: This 13-year-old μP is finding continued use. Supplier believes it will remain active for at least the next few years because it has not received direct competition from other bipolar μPs. Original 8X300 has been upgraded to 8X305 and then to 8X400. Supplier says the 8X400 is "much more programmable" than 8X305. Note that second-source AMD is using "29" prefixes, presumably to incorporate 8X305 within large and diverse 2900 bit-slice family. Will there be a CMOS version of the 8X300?

HARDWARE — CHARACTERISTICS — SOFTWARE



PART	DESCRIPTION	PACKAGE	PRICE (100 QTY)
8X305	8-BIT μC (900 MILS WIDE)	50-PIN PLASTIC	$22
8X300	8-BIT μC	50-PIN CERAMIC	$40.10
8X310	INTERRUPT CONTROLLER	40-PIN PLASTIC	$15
8X320	8/16-BIT BUS INTERFACE	40-PIN PLASTIC	$26.10
8X330	FLOPPY-DISK CONTROLLER	40-PIN PLASTIC	$30
8X350	256×8 RAM	22-PIN PLASTIC	$42
8X360	MEMORY-ADDRESS DIRECTOR	40-PIN PLASTIC	$28.25
8X371	TRANSPARENT I/O PORT	24-PIN PLASTIC	$3.15
8X372	ADDRESSABLE I/O PORT	24-PIN PLASTIC	$3.15
8X374	ADDRESSABLE I/O PORT	28-PIN PLASTIC	$5.75
8X376	ADDRESSABLE I/O PORT	24-PIN PLASTIC	$3.15
8X382	ADDRESSABLE I/O PORT	24-PIN PLASTIC	$3.15
8X401	8-BIT μC	64-PIN	NA
8X450	256×8 RAM	NA	NA
8X470	I/O PORT	NA	NA

I—DATA-MANIPULATION INSTRUCTIONS
ADD is the sole arithmetic command. AND and XOR are two logical commands. However, the CPU can shift and bit test, mask and merge while executing instructions. Thus, it can examine and operate on I/O bits in 200 nsec
II—DATA-MOVEMENT INSTRUCTIONS
Move data between source and destination (MOVE)
Send literal value (part of instruction) to destination (TRANSMIT)
III—PROGRAM-MANIPULATION INSTR
Indexing by jamming offset into PC (EXECUTE)
Branch if data is not zero (NZT)
Software polling can be performed rapidly; hardware interrupt controller available
IV—PROGRAM-STATUS-MANIP INSTR
None
Note: Simplified instruction set emphasizes control functions rather than general-purpose computation. Each instruction specifies source of data, operation to be performed on data, and destination for data. Sources and destinations can be I/O ports—a feature that accounts for the machine's superiority as high-speed controller. The 8X400 has additional instructions.

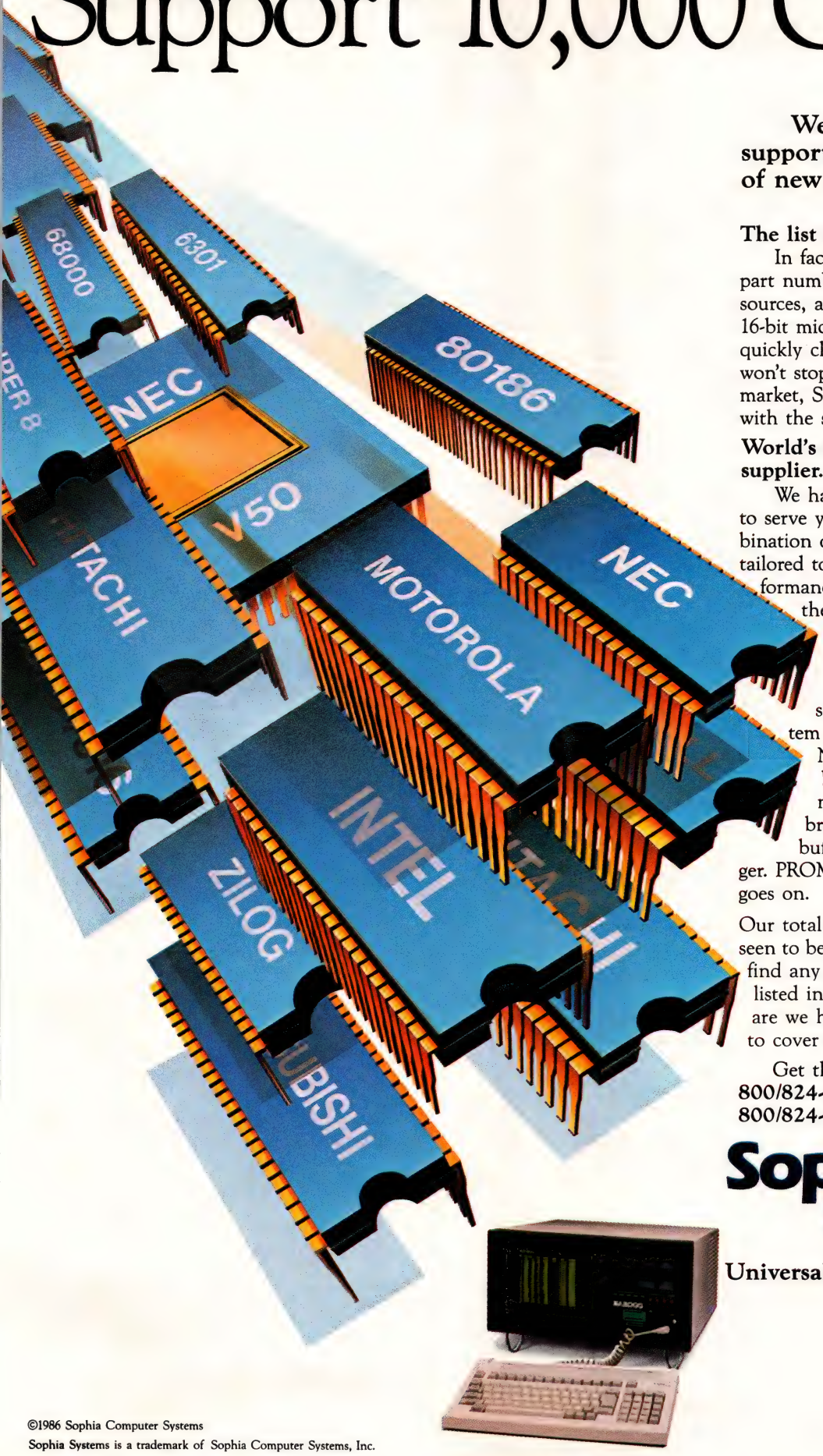
Specification summary: Split-memory architecture with 8-bit data word and 16-bit instruction word. Each minicomputer-sized instruction word allows performance of complete data movement plus manipulation operations in one cycle or 200 nsec at 10-MHz clock. Because I/O ports are in data space, I/O data can be turned around in 200 nsec. μCs built from 8X305 are considerably simpler than those built from other bipolar μPs. Simple instruction set allows placement of complete Schottky bipolar CPU on 225-mil² die. In addition to 5V supply (150 mA), needs external transistor to develop 3V (300 mA) for internal logic. The 8X400 uses ECL internal circuitry to achieve 100-nsec instruction cycles.

HARDWARE — SUPPORT — SOFTWARE

From Signetics: 8X305 and 8X400 prototyping system includes CPU, support components, and wire-wrapping breadboard space. Has PROM-resident monitor, debugging program, and RS-232C interface ($500).
From American Automation (Tustin, CA): EZ Pro, a development system with relocating crossassembler and full-speed in-circuit-emulation capability. Supports 8X305 and other μPs.
From Sigen (Santa Clara, CA): 8X305 ICE Pack, a full-speed in-circuit-emulation module for use with Sigen CP/M-based computer or Intel Intellec. CP/M crossassembler also available.
From Data I/O (Redmond, WA): Plug-in modules that program I/O-port addresses on Data I/O systems.
From Step Engineering (Sunnyvale, CA): Step 3, a higher speed ROM/PROM simulator.

MCCAP microcontroller crossassembler, written in Fortran, produces 8X300 and 8X305 object code in form suitable for most PROM programmers. Comes on 9-track tape for mainframes or minicomputers or on diskette for Intellec systems ($200). For 8X400, Fortress symbolic crossassembler. Step Engineering provides Step 2 firmware.

Support 10,000 Chips



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CIRCLE NO 99

2900, 29C00, 29G00 BIT SLICE

AVAILABILITY: Now for older original bipolar parts and many new CMOS variations on 2900 theme. But varies for latest highest speed and widest word versions.
COST: $6.65 for 2901A/B/C in 100 qty; $21 for 2903A in 100 qty. See table for others. Prices for CMOS similar
SECOND SOURCE: For original bipolar 2900: Raytheon and Thomson Semiconducteurs, though Raytheon not active. For new CMOS versions: IDT, Cypress, Waferscale Integration, and others including Asian companies. For GaAs versions: Vitesse (29G01) and possibly McDonnell Douglas
CORE: Most of the sources for CMOS 2900 also have the family parts in their cell library or intend to have them. In addition, there are companies that may not necessarily have 2900 parts off the shelf but still have them in their cell libraries, such as GE/RCA, Gould, VTC and VLSI Technology

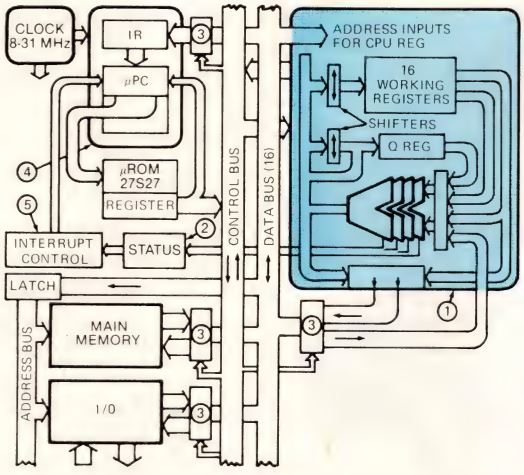
Description: Ever-growing and changing family of mostly TTL-bus-compatible, bit-slice building blocks. By now almost all possible semiconductor technologies are being used: bipolar (both TTL and ECL internally), CMOS, and even GaAs (gallium arsenide). Family is intended for microprogrammable systems where they can be used to emulate existing computers or be used to build specialized digital controllers. Latest twist for family is the use of these building blocks as macrocells in semicustom libraries. See also entries for AMD 29300, AMD 29500 DSP, TI 74AS88XX, 8X305, and Analog Devices' Word Slice DSP.

4-BIT×N; 16-BIT, 32-BIT BIPOLAR, CMOS AND GaAs

Advanced Micro Devices
901 Thompson Pl
Sunnyvale, CA 94086
Phone (408) 732-2400

Status: This amazing bit-slice family has been around a long time. We've had it in the directory since 1975. Each time we think its life is over, the 2900 is reborn. Right now it's getting new life from CMOS versions from many different sources. These CMOS versions have almost the same speed as the original bipolar—some of their suppliers claim equal or better speed—and only a fraction of the power consumption. Furthermore, in many instances, the CMOS versions are part of macrocell libraries so that they can be assembled (ideally by customer engineer at his workstation) into single- or few-chip semicustom VLSI solutions. It appears the 2900 family will be an important architectural vehicle for engineers exploring new world of ASIC.

HARDWARE — CHARACTERISTICS — SOFTWARE



User defines macroinstruction set by microprogramming μROM. Parts respond to the following instructions:
I—DATA-MANIPULATION INSTRUCTIONS
2901 performs three arithmetic functions on two operands, as well as five logic functions
2903A performs seven arithmetic functions and nine logic operations, as well as multiply and divide. Simultaneous add (or subtract) and shift possible
29203 has floating-point-normalize instruction
II—DATA-MOVEMENT INSTRUCTIONS
16 working registers in RALU RAM can be addressed two at a time for simultaneously supplying the two operands to the ALU
III—PROGRAM-MANIPULATION INSTR
Defined by user in microcode. 2930 program-control unit executes 32 fetch and branch instructions
IV—PROGRAM-STATUS-MANIP INSTR
2904 shift and status-control chip provides two status registers for the 4-bit carry, overflow, zero, and negative. Bits can be set or cleared. Shift through carry or overflow. Borrows can be stored for subtract

Specification summary: TTL-bus-compatible building blocks for creating moderately high-performance computers and controllers. Slices were originally 4 bits wide but now widths come up to 32 bits. Parts include sufficient features for emulating most computer architectures. User defines end product's macroinstruction set by microprogramming μROM. RALUs (2901, 2903, and 29203) respond to eight and 16 basic instructions (2903 and 29203 include multiply and divide and floating-point normalization) within one clock cycle of 50 to 125 nsec (2901C performs 16-bit add in 83 nsec). Original family parts fabricated entirely from Schottky TTL, but higher-speed ECL has been used for internal circuits. Now family is being converted to CMOS because it's being found that modern fine-geometry (near 1 μm) CMOS can produce equivalent speeds at lower power consumption. With CMOS, there's a trend to consolidate multiple 2900 functions on chip and to go to new space-saving packages (as power dissipation lessens).

BASIC 2900 PARTS

PART	# ON DIAGRAM	DESCRIPTION	COST (100 QTY)
2901/B/C	1	ALU	$6.65
29C01			$6.65
29C101			$35
2902A			$1.80
2903/A			$20.50
29203		ALU (BCD)	$20.50
2904	2		$16.95
29705/A		2-PORT RAM	$10.65
2909/A	4	MICROPROGRAM CONTROL UNITS	$5.65
2910/A			$13.35
29C10A			$13.35
2911/A			$4.35
29803A			$4.30
29811A			$3.35
2930		PROGRAM CONTROL UNITS (RELATIVE ADDRESSING)	$19.95
2932			$17.95
2913		INTERRUPT	$2.35
2914	5		$18
2905	3	TRANSCEIVERS	$5.40
2906			$7.45
2907			$4.75
2915A			$5.40
2916A			$7.45
2917A			$4.75

HARDWARE — SUPPORT — SOFTWARE

From AMD: System 29 development station ($17,495) is intended specifically for developing microcode for microprogrammable machines; allows user to build prototypes using universal cards.
From semicustom VLSI houses (see note 3): Various workstation aids for assembling custom chips from 2900-based cell libraries.
From others: Development systems available from HiLevel Technology (Tustin, CA) and Step Engineering (Sunnyvale, CA); for example, the new STEP-40 system from Step.
For ASIC: Silicon compilers for members of 2900 family (2901, 2910, 2913 and 2940) are in VLSI Technology's compiler library ($25,000).

From AMD: AMDASM/29 microprogram assembler available in disk form for System 29. AMDASM written in Fortran available from Microtek (Sunnyvale, CA).
From others: Meta assemblers from HiLevel Technology (Tustin, CA) and Step Engineering (Sunnyvale, CA).
Literature: Textbook, *Bit Slice Microprocessor Design,* by John Mick and Jim Brick, McGraw-Hill, 1980 ($18.50).

29300/400, 29C300

32-BIT BIPOLAR AND CMOS

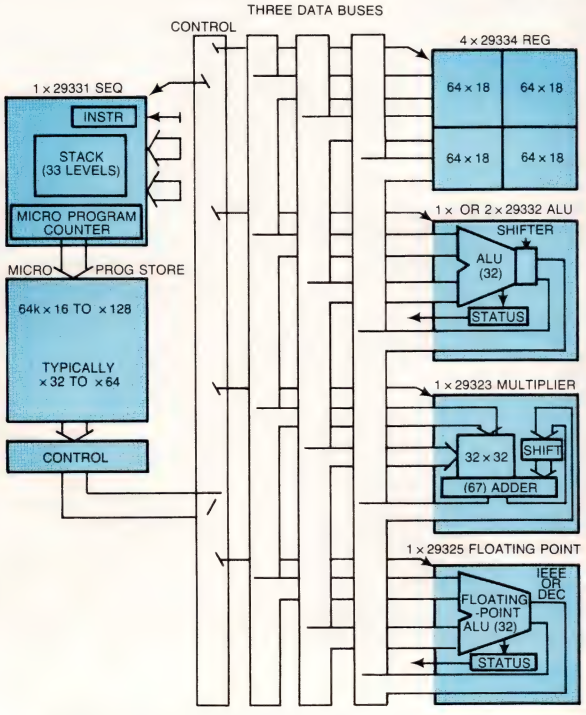
AVAILABILITY: The 29300 core parts are in full production. The 29434 of the ECL family is sampling, and full core-set availability is scheduled for first quarter '87. The 29C323 of the CMOS family is available now, and full set of CMOS parts is expected by fourth quarter '87
COST: As can be seen from table, cost is initially in the hundreds of dollars per part, even at 100 qty
SECOND SOURCE: None directly, but especially for the CMOS parts, quite a few suppliers make functionally similar devices, such as TI, IDT, Weitek, Wafer Scale Integration, etc

Description: 32-bit bipolar and CMOS building-block chip set that follows the concepts established by the 2900 bit-slice family, but with two major differences. First, the family members all have a fixed 32-bit data width. Second, the architecture and the resulting microinstruction set are optimized for easy compiler writing. State-of-the-art performance has been achieved, as indicated by 80- to 90-nsec microinstruction cycle times and a DSP-quality 32×32-bit multiplier that completes within this cycle time. Supplier says it has followed customer advice and left final architectural decisions to users.

Advanced Micro Devices
901 Thompson Pl
Sunnyvale, CA 94086
Phone (408) 732-2400

Status: Supplier has targeted this family at designers of superminis as well as DSP, graphics, and communications. Systems built from chip set could have three to 10 times the performance of a VAX 11/780. Even faster ECL I/O version—the 400—is expected to have 40- to 50-nsec microinstruction cycle. The lower-power CMOS versions (29C300) will have 120-nsec cycle times with speed selections. Meanwhile, TI has introduced a competing chip set, the 74AS88XX, and others (see second-source description) make functionally similar versions of some parts, a factor to consider because many designers mix devices from different families.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
For 332 ALU: includes 64-bit n-bit shift-up/down funnel shifter that can be combined with logic functions. Multiply and divide (one bit at a time). Priority encoding to support floating-point operations and graphics
For 325 floating point: efficient execution of Newton-Raphson division and Horner's method of polynomial evaluation. Both IEEE and DEC formats (addition, subtraction, multiplication) with conversion between two modes
For 323 32×32-bit multiplier: single- or double-precision multiply in one or four cycles, respectively
II—DATA-MOVEMENT INSTRUCTIONS
For 334 64×18-bit register file (cascaded for full word width and desired length and used in conjunction with ALU): individual write for byte, 16-bit half word, or 32-bit full word
III—PROGRAM-MANIPULATION INSTR
For 331 Microprogram Sequencer: instructions designed to support high-level-language constructs
The 33-level stack supports interrupts, loops, subroutine nesting, and multitasking at micro level
Microtrapping for reuse of prior microinstruction
No support for relative addressing, as designers wanted to avoid performance penalty of adder. But decisions and interrupts handled on chip for fastest response
IV—PROGRAM-STATUS-MANIP INSTR
Status registers in ALU, floating point, etc
Notes:
1. Designers say they endeavored to keep instructions orthogonal and symmetrical to ease task of compiler writing and facilitate structured microprogramming.
2. Self-checking implemented by parity bits in register file and by parity in off-chip data paths and ability to parallel units and compare results.

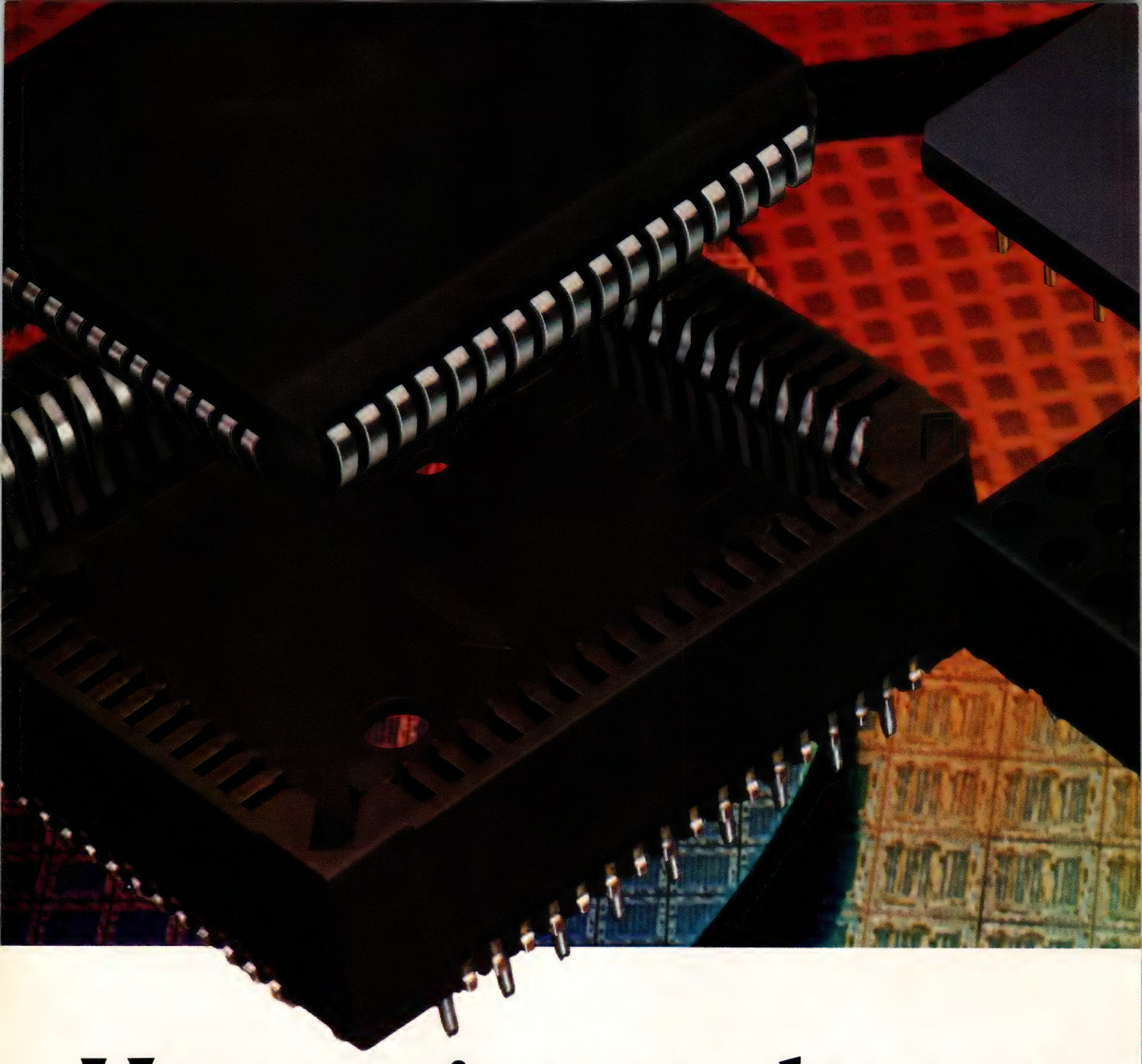
PART NO	DESCRIPTION	PERFOR-MANCE	AVAIL-ABILITY	COST (100)
TTL FAMILY				
29323	32-BIT MULT	90 nSEC	1 QTR87	NA
29331	16-BIT SEQUENCER	90 nSEC	NOW	$195
29325	32-BIT PROCESSOR	90 nSEC	NOW	$695
29332	32-BIT ALU	90 nSEC	NOW	$495
29334	64×18 REG FILE	24 nSEC	NOW	$180
29337	BOUNDS CHECKER	20 nSEC	NOW	$30
29338	BYTE QUEUE	90 nSEC	1 QTR87	NA
ECL FAMILY				
29423	32-BIT MULT	40 nSEC	1 QTR87	NA
29431	16-BIT SEQUENCER	40 nSEC	4 QTR86	NA
29432	32-BIT ALU	40 nSEC	4 QTR86	NA
29434	64×18 REG FILE	20 nSEC	NOW	$200
CMOS FAMILY				
29C323	32-BIT MULT	125 nSEC	NOW	$295
29C325	32-BIT PROCESSOR	125 nSEC	3 QTR87	NA
29C331	16-BIT SEQUENCER	125 nSEC	1 QTR87	NA
29C332	32-BIT ALU	125 nSEC	3 QTR87	NA
29C334	64×18 REG FILE	35 nSEC	1 QTR87	NA

Specification summary: Building blocks for 32-bit-wide microprogrammable computer systems. The core set includes five parts (see table) that can stand alone or be used in mixed systems. Architecture supports the features needed on advanced minicomputers, like parity checking and master/slave functional comparisons. Also suited for direct, very fast execution of high-level languages via compiled microcode. Triple data-bus architecture, with unidirectional buses for minimum speed loss caused by bus turnaround. Parts have 20- to 30-nsec throughputs so that 70- to 80-nsec microinstruction cycles can be accomplished. Architecture sufficiently open to allow inclusion of performance accelerators, and family includes a floating-point unit (125 nsec) and a 1-cycle fixed-point multiplier (80 nsec). Bipolar technology with off-chip TTL interfaces. Packages incorporate three low-profile horizontal fins to handle the 4 to 7W heat dissipation. Fins are horizontally oriented so that cooling air flow can be in any direction and the package height will be low enough (0.4 in.) to allow normal board spacing. Required cooling air flow (300 cfm) is said to be within allowable limits for office environments. CMOS versions will dissipate in the 1W range and will not require heat sinks or cooling air flow.

HARDWARE — SUPPORT — SOFTWARE

Supplier recommends same approach for development systems as that used in 2901 family microprogrammable bit slices. Typically, microcode ROM-simulation systems like those made by Step Engineering (Sunnyvale, CA) and HiLevel Technology (Tustin, CA), and other similar aids, including those made by Hewlett-Packard and Tektronix. Supplier's System-29 development station is being extended for 29300.

Supplier now provides M-29 upgrade of its ADASM general-purpose crossassembler for microcode, written in C to run under UNIX.



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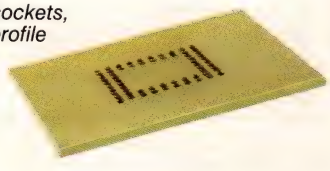

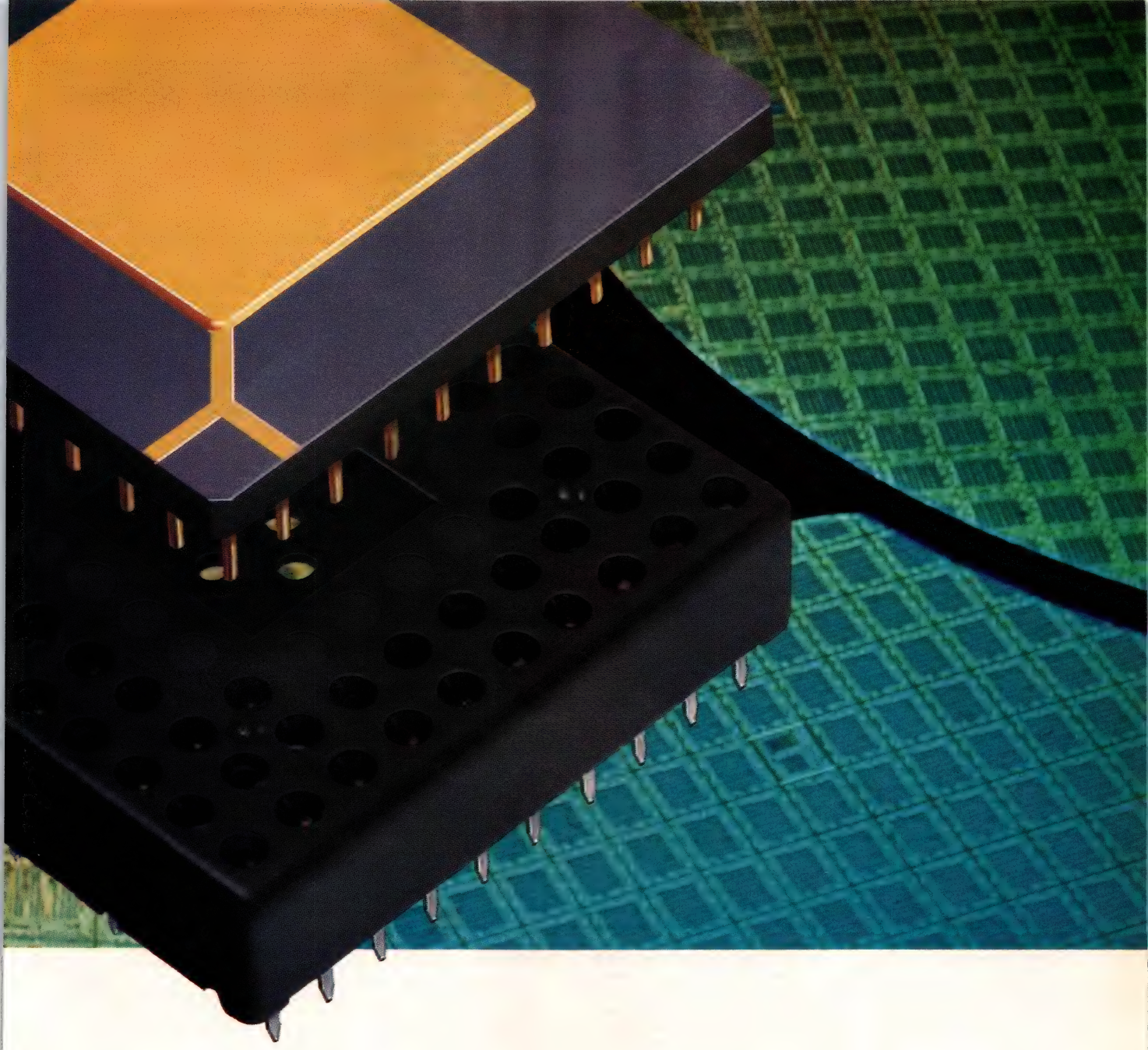

Whichever direction you take in microprocessor technology, AMP makes sure you have the socketing options you need to make it pay off.

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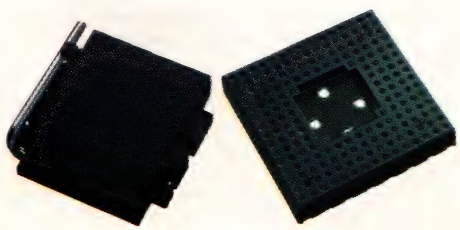
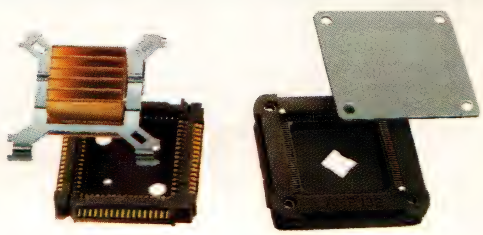
CIRCLE NO 100

AMP Interconnecting ideas



Low-height sockets in all standard sizes (JEDEC A, B, D), with duplex-plated contacts for sure performance. High-speed, surface-mount sockets feature 0.5pF, 1.4nH contact characteristics.



74AS8XX/74AS88XX

8- AND 32-BIT BIPOLAR AND CMOS

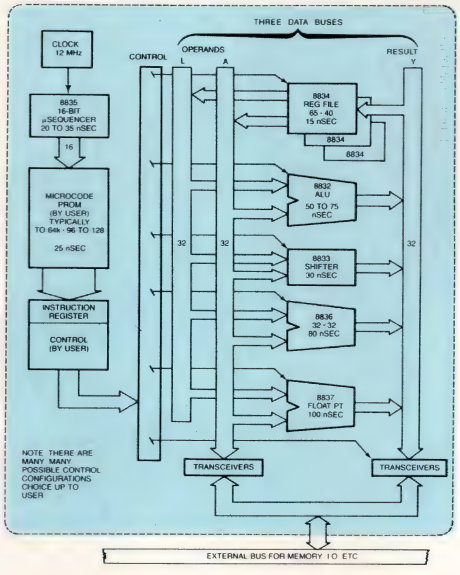
AVAILABILITY: Now for 8XX parts. First 88XX parts (8831 barrel shifter) in first quarter '86; remainder by first quarter '87. Full production scheduled for first quarter '87
COST: See table for 8XX prices. Prices of 88XX to be determined, but expected to be "much more" than 8XX, or in the hundreds of dollars
SECOND SOURCE: None, but see AMD 29300/400 for similar family (often designers mix and match between families)

Description: 8- and 32-bit custom CPU building-block chip sets done in high-performance bipolar and CMOS processes. Cycle times of 50 to 75 nsec worst case said to be accomplished at relatively low power-dissipation levels even for bipolar members, so no heat sinking is required. Family architecture facilitates byte operation, allowing for flexibility in the data-word manipulation and resulting in system throughput in the 10-MIPS range.

Texas Instruments Inc
13536 N Central Expressway
Dallas, TX 75265
Phone (214) 995-4720

Status: Supplier expects to compete with the similar AMD bipolar 29300/400 chip set for applications in high-end workstations, graphic engines, and performance-driven superminis. Supplier's chips may also receive competition from the new fine-geometry CMOS μPs, such as the Fairchild Clipper. These fine-geometry CMOS devices are projected to have MIPS rates similar to those of the supplier's chips, though the CMOS devices don't allow designers the architectural flexibility of bipolars and don't have such features as built-in parity generation and checking.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Family architecture facilitates the high degree of system parallelism possible with "wide" microcoding, allowing designer to operate devices simultaneously for greater throughput.
2. ALU and microsequencer support master/slave operation for tandem processing.
3. All members are 2-μm bipolar except for 8836 and 8837, which will start out in 1-μm CMOS. The bipolars will achieve low (4W) power dissipations because they will use special Schottky transistor logic (STL) that operates at 2V internal supply. Because of their large die size (in order of 100k sq mils) and complex structure (two Schottky barrier metals are used), these circuits are likely to start off with low yields.

PART NO	DESCRIPTION	PERFORM-ANCE (mSEC)	NO OF PINS	AVAIL-ABILITY	COST (100)
74AS888	8-BIT REGISTER ALU	46	68	NOW	$35
74AS890	14-BIT MICRO-CONTROLLER	42	68	NOW	$40
74AS897	16/32-BIT BARREL SHIFTER	50	68	NOW	$40
74AS870	DUAL 16-WORD x4-BIT REGISTER	22	24	NOW	$6.58
74AS8832	32-BIT REGISTER ALU	50-75	208	1 QTR87	NA
74AS8835	16-BIT MICRO-SEQUENCER	20-35	156	1 QTR87	NA
74AS8834	65Wx40-BIT REGISTER FILE	15	156	4 QTR86	NA
74AS8833	BARREL/FUNNEL SHIFTER	30	156	1 QTR87	NA
74AS8831	32/64-BIT BARREL SHIFTER	25	86	NOW	$40
74ACT8836	32x32-BIT MULTIPLIER	80	NA	1 QTR87	NA
74ACT8837	FLOATING-POINT PROCESSOR	100	NA	1 QTR87	NA

I—DATA-MANIPULATION INSTRUCTIONS
For 8800 ALU:
Supports double-precision data format for all instructions. Multiply and divides, 13 arithmetic and logic functions. Eight conditional shifts, normalization (all double and single length). Byte-oriented architecture allows structuring the data word in 8, 16, 24, or 32 bits
For 8833 funnel/barrel shifter:
Priority encoding supports floating-point and graphics applications. 64-bit input can be masked for data manipulation on 32 extracted bits. Supports single clock cycle byte rotation. Circular arithmetic and logical operations on 32-bit fields. On-chip parity generation/check
For 8837 16/32-bit floating point:
Supports IEEE and DEC formats with conversion between the two. Also supports double- and single-precision operations
For 8836 multiplier:
Supports 16- and 32-bit signed and unsigned multiplies. Indicates overflows and supports sign extends
II-DATA-MOVEMENT INSTRUCTIONS
For 8832 RALU:
Three-operand 64W×36-bit register file on chip supports byte-oriented operands for variable data word widths. 36-bit width=32 bits data+4 parity bits. On-chip parity generation/checking
For 8834 register file:
64W×40-bit edge-triggered register file cascadable with 74AS3232 ALU. Three-operand file with output mux for flexibility in data-word manipulation. Also byte oriented. On-chip parity check
III-PROGRAM-MANIPULATION INSTR
For 8835 microsequencer:
Facilitates high-level-language constructs; deep 65×20 stack supports interrupts. Two loop counters support nested loop program routines. On-chip breakpoint comparator for automatic branch routines. On-chip diagnostic registers and 890 upward compatibility for easy microcoding. Executes simultaneous interrupt and trap operations. Select next branch instruction from one of nine locations via output mux. All instructions can be made conditional via externally applied condition-code pin and/or value in internal register
Note: Instructions described are for 88XX family devices. The 8XX instructions are a subset, and the two sets are completely compatible.

Specification summary: Building blocks for microcoded custom CPU architectures. The 8XX family has four parts and the 88XX family will have seven (see table). As the 74AS prefix indicates, the devices meet the specifications of the AS version of the well-known 74 logic family line. Two of the devices with 74ACT prefixes use TI EPIC CMOS process but have TTL-compatible outputs. The architecture is designed to support high-performance minicomputer workstation and graphic machines by incorporating features like parity generation/checking, master/slave operation for tandem processing, and 3-bus architecture (see diagram). Worst-case cycle times of 50 to 75 nsec can be accomplished with relatively low power dissipation (4W), which eliminates the need for device heat sinks. On-chip diagnostic registers on the sequencer and barrel/funnel shifter ease microcode development. Large pin-count devices (see table) are packaged in pin-grid arrays and plastic leaded chip carriers.

HARDWARE — SUPPORT — SOFTWARE

Supplier recommends same approach for development systems as that used with other microcoded building-block chip sets such as the 2900. Third-party support can be obtained from Hewlett-Packard, HiLevel Technology (Tustin, CA), and Step Engineering (Sunnyvale, CA). High-speed microcode ROM emulators from above companies cost $13,000 to $30,000. Supplier's evaluation module (EVM) board incorporates a full Basic interpreter and monitor program that can be accessed through an RS-232C port using a nonintelligent terminal or terminal emulator (a personal computer with appropriate software).

Meta- and crossassemblers will be provided by third-party vendors such as HiLevel Technology ($1400), as well as an OEM version from the supplier. Existing assemblers in place for the 74AS8XX are compatible with the 74AS88XX family.

μPD7720A SIGNAL PROCESSOR

AVAILABILITY: High-volume ROM codes for US customers have been processed for several years. Full-speed EPROM version available in quantity since mid '82. CMOS now available
COST: $15 at 1k qty. $10 in high volume and is headed towards less than $10 by mid '87. CMOS 77C20A costs $15 at 1k qty, less than $12 in high volume, and is also headed towards less than $10 by mid '87. The EPROM 77P20 sells for $25 in 100 qty
SECOND SOURCE: Gould (AMI) and Oki. Gould for earlier 7720 version (not 7720A); Oki for CMOS 77C20 (not 77C20A0). Gould says it will have 77C20 by first quarter '87. Silicon Systems has license for Oki 77C20D

Description: Single-chip microcomputer aimed at fast, fixed-point mathematical (number-crunching) applications, such as speech recognition and synthesis, telecommunications, sonar signal analysis, and graphics. Performs 16×16=31-bit multiplications within its basic 240-nsec instruction cycle; one maskable interrupt; directly handles serial data. Can be used in stand-alone mode or as μP peripheral.

16-BIT NMOS AND CMOS DSP

NEC Electronics Inc
(Corporate Headquarters)
401 Ellis St
Mountain View, CA 94039
(415) 960-6000

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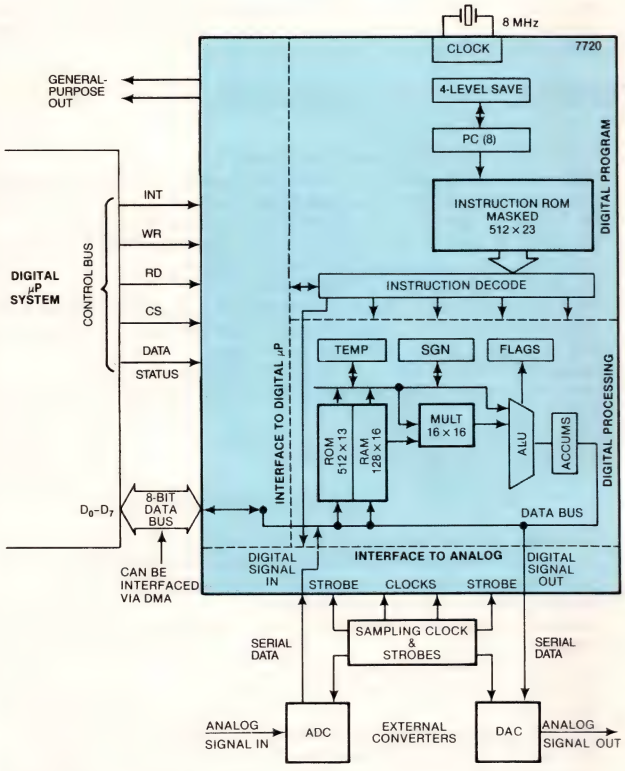
Natick, MA 01760
Phone (617) 655-8833

Status: This 28-pin device is the first single-chip DSP to achieve commodity-level volume and pricing. According to NEC, it is being shipped at 5M annual unit volume and is selling for $7 in volume. Its price for both NMOS and CMOS versions is headed toward $5 by end of '87. It has three second sources. NEC claims that 75% of modem designers in US use the 7720 (for 2400- and 4800-bps modems). Although NEC has the new, much more powerful and more general-purpose 77230, NEC says it is unlikely to abandon the 7720 because it's generating revenues of $50M annually and is still being designed into new products.

HARDWARE — CHARACTERISTICS — SOFTWARE



DATE OF INTRO	PART NO	SOURCES		TECHNOLOGY	POWER DRAIN, mA
		PRIME	SECOND		
1980	7720D	NEC	GOULD	3.1-μm NMOS	280
1982	77P20	NEC		3.1-μm NMOS	NA
1984	7720A	NEC		2.4-μm NMOS	170
1985	77C20D	OKI	SIL SYST	3.1-μm CMOS	20–40
1986	77C20A	NEC		2.4-μm CMOS	10–40

I—DATA-MANIPULATION INSTRUCTIONS
For ALU: add, logicals, decrement, shift, and complement (multiplication done in the separate multiplier every instruction cycle)
II—DATA-MOVEMENT INSTRUCTIONS
Source/destination addressing; load immediate; unique row/column RAM addressing scheme provides for efficient filter algorithms
III—PROGRAM-MANIPULATION INSTR
Conditional branches for zero, overflow, serial-data-buffer status and other flags
Four levels of subroutining
IV—PROGRAM-STATUS-MANIP INSTR
Each of the two accumulators has a duplicate set of flags relating to ALU status
Notes:
1. Multifunction instructions allowing six separate functions in one instruction cycle.
2. Benchmarks said to show a second-order biquad filter section requires nine instructions and takes 2.25 μsec; a 32-point complex FFT requires 213 instructions and takes 700 μsec.
3. Dual overflow and sign flags allow special hardware saturation register (SGN) to hold correct value for as many as three consecutive additions/subtractions for proper overflow correction in second-order filters. Two additional instructions for testing and loading required.

Specification summary: Single-chip digital signal processor that can execute 16-bit sum-of-products computations in 250-nsec instruction cycle. Split-memory architecture with instruction side fed from 512×23 masked ROM as addressed by program counter with 4-level subroutine/interrupt-save stack. Data side receives and delivers 8-bit digitally coded analog signals at 2-MHz shift rate and processes them in 16-bit parallel data paths and registers, storing intermediate results in 128×16 RAM and obtaining equation coefficients from 512×13 ROM. Two NMOS versions (see table): the original 3.0-μm-process part that runs at 250-nsec instruction cycles and consumes 180-mA typ and 280-mA max supply current and the newer 2.4-μm-process part (by die shrink) that runs at 240-nsec instruction cycle and consumes 120 mA typ and 170 mA max. There are similar speed differences between the 77C20 and 77C20A CMOS parts. Extended −40 to +85°C temperature range for the NMOS 7720A and for the CMOS 77C20A. Package options include 28-pin DIP (plastic and ceramic) and 44-pin PLCC.

HARDWARE — SUPPORT — SOFTWARE

Evakit-7720 hardware emulator (less than $3000) is a 3-board system with full-speed operation. First board contains special version of 7720 with 100 leads, permitting access to all internal buses and registers. Fast bipolar RAM provided for program store. Second board carries an 8085 μP that serves as host μP and system monitor. Third board provides programming for EPROM version of 7720 (77P20).

Assembler ($900) and simulator ($900). Simulator includes tracing, breakpoint, disassembly, and other software-debugging capabilities. Versions available for MS/PC-DOS, CP/M-86, CP/M development systems and Intel development system (ISIS-based). A VAX-based crossassembler written in Fortran is available for $2500.

320 DSP FAMILY

16-BIT NMOS AND CMOS DSP

AVAILABILITY: Now for 32010 (14, 20, and 25 MHz). Now for 320C10 (20 and 25 MHz with 32 MHz from GI). Now for 32020 (20 MHz). Samples for 32C20 (10 MHz)
COST: $42 (100 qty), dropping to $10 in high volume for ROMless 32010. Masked-ROM 320M10, CMOS versions and 25-MHz version has adder on price: $12 in 100 qty, dropping to $5 in high volumes for slower 32010-14. For 32020: $125 for 32020 (100 qty), dropping to $15 for high volume for NMOS. $500 for CMOS 320C25 samples, dropping to $20 in '87
SECOND SOURCE: General Instrument for 32010 and 320C10 (and some original design versions)

Description: Listed in this directory since 1982, this DSP family was the first to combine a general-purpose single-chip-μC architecture with a fast and powerful ALU and a 1-cycle multiplier. Similarity to 4- and 8-bit single-chip μCs made it easier to program than previous DSP devices, and it benchmarked well on DSP algorithms. It also has been found suitable for fast controller-type applications and is low enough in cost that it could be used on personal-computer accelerator boards. Speed improvements of original family models and architectural improvements of later models have boosted the performance.

Texas Instruments Inc
DSP Dept
Box 1443, M/S 6437
Houston, TX 77001
Phone (713) 879-2320

For Military Version:
Texas Instruments Inc
Military Products
Box 6448, MS 3028
Midland, TX 79711
Phone (915) 561-6599

Status: This continues to be the sales leader in the DSP market, according to a 1985 Gnostic Concepts DSP Report. However, the 320 architecture with its relatively narrow instruction, address, and data words and somewhat slow cycle time may begin to feel competition from the many new higher-performance DSP architectures now being introduced from other suppliers (see for example the AT&T and NEC floating-point 32-bit machines and the Motorola 24-bit fixed-point machine elsewhere in this directory). But TI may have some breathing time because the newer DSPs have very large chips and packages, and for time being can't hope to come any where close to the $10-in-volume prices promised by TI.

HARDWARE — CHARACTERISTICS — SOFTWARE

SEE EDN, NOVEMBER 28, 1985, PG 193, FOR BLOCK DIAGRAM AND NOTES.

Specification summary: First family member, **32010**, is single-chip 16-bit DSP with 32-bit data paths. Has modified split-memory architecture so 1.5k×(16) program ROM can interact with 144×(16) data RAM. 32-bit product of 16×16 multiply feeds 32-bit ALU, as does 0 to 15-bit barrel shifter. Can perform a 120-point FFT with 16 scratch-pad data locations left over. Chip area around 50k sq mils. Fabricated in 2.4-μm silicon-gate NMOS, draws 950 mW from 5V supply, and comes in 40-pin DIP. **320C10** is 32010 fabricated in 2.0-μm CMOS, draws 125 mW from 5V supply, and comes in 40-pin DIP or 44-pin PLCC. **32020** is enhanced 32010 that can address up to 64k program and 64k data memory. Internal RAM expanded to 544×(16) that can be split in two blocks shared between program and data or used as two separate data sources to feed both inputs of multiplier simultaneously. Has 6-bits-to-right shift for avoiding overflow on long DSP multiply/accumulate sequences. Can perform a multiply/accumulate/data move in single cycle. Repeat instruction allows savings of program space and make multicycle instructions into single-cycle instructions. Multiprocessing capabilities such as synchronization, global memory, and μP-like interface. Block moves streamline memory management. Wait states, on-chip timer, and serial ports. Fabricated from 2.4-μm silicon-gate NMOS with chip measuring 115k sq mills and drawing 1.2W from 5V supply. Packaged in 68-pin grid array. **320C25** is enhanced 32020 with 4k ROM on chip, 100-nsec cycle time, 8 auxiliary registers, carry bit on accumulator, 8-deep stack for interrupts, and double-buffered serial ports. Fabricated in 1.8 DLM CMOS with chip measuring 110 sq mils and drawing 450 mW from 5V supply. Packaged in 68-pin PLCC.

I—DATA-MANIPULATION INSTRUCTIONS
Add and subtract, with 0- to 15-bit simultaneous shift option, multiply and conditional subtract (to assist divide), logicals
On 32020: floating-point assist and "square-and-add" instructions
On 320C25: carry bit with multiprecision arithmetic support and unsigned multiply instructions. Also adaptive filtering instructions
II—DATA-MOVEMENT INSTRUCTIONS
Four basic addressing modes: Direct, Indirect from AR, Indirect from AR with autoincrement or autodecrement. Also Immediate operands (13 bits on original 32010, 16-bits on later models)
Store accumulator HIGH or LOW with 0- to 8-bit offset option
Data-shift memory (can be used for Z^{-1} shift in DSP and in correlation, etc)
Load T register (for multiply), accumulate and shift data memory (example of multiple operations for DSP)
IN, OUT to eight external ports
TABLE Write and Read (so can use external program memory for data or I/O)
On 32020: more addressing modes, full 16-bit immediates, block moves, and 1-cycle multiply/accumulate by Repeat instruction. On 320C25: bit-reversal addressing, 8-bit immediate add and subtract
III—PROGRAM-MANIPULATION INSTR
Conditional BRANCHs upon status bits or contents of accumulator
Branch on I/O pin
Call and RETURN (for subroutines)
Vectored interrupts (with special 10V inputs, can be used for emulation breakpoints)
On 32020: repeat instructions allow single instruction to be performed up to 256 times; Push and Pop instructions to allow extended nesting of subroutines and interrupts in data memory. On 320C25: Hold mode allows processor to continue operation with on-chip memory while external memories are read/modified
IV—PROGRAM-STATUS-MANIP INSTR
Enable and disable interrupt
Load and Store status: overflow, overflow mode, interrupt mode, plus data-address pointers are saved in data RAM. Additional flags and instructions on 32020 with still more on 320C25
Notes:
1. Most instructions are one 16-bit word long and execute in one 200-nsec cycle. Multiplication executes in one cycle but multiply-accumulate needs 2 cycles. However, due to pipelining, register set ups and data moves can be done concurrently. Branches are 2-word, 2-cycle instructions and have a 16-bit address span (expansion to 24 bits).
2. 32020 instructions superset of 32010. It does have dual data RAMs so in one mode can load in both operands to multiplier simultaneously.

HARDWARE — SUPPORT — SOFTWARE

From TI: EVM evaluation modules ($1000 for 32010, $3000 for 32020/C25). AIB analog interface board ($795) for 12-bit A/D and D/A, with adapter board for 32020/C25 ($150).
XDS-box emulators for full-speed in-circuit emulation up to 100-nsec cycle ($8500 for 32010, $13,500 for 32020/C25). Interfaces to terminal or host computer such as IBM PC.
From others: There are dozens of third-party vendors supporting family, many making easy-to-use products such as boards that plug into IBM PC. Contact TI for names.

From TI: Macro assembler/linkers ($500) and simulators ($1500) to run on VAX/VMS and IBM PC/MS-DOS. 3020/C25 software development system ($3000) is composed of PC card, assembler/linker and applications library. Provides real-time in- circuit emulation with environment to reassemble, relink, and reload code when debugging.
From others: A dozen or so companies have developed crossassemblers and simulators and DSP design aids for the 32010 and 32020. Most of these programs are for IBM PC. Contact TI for names.

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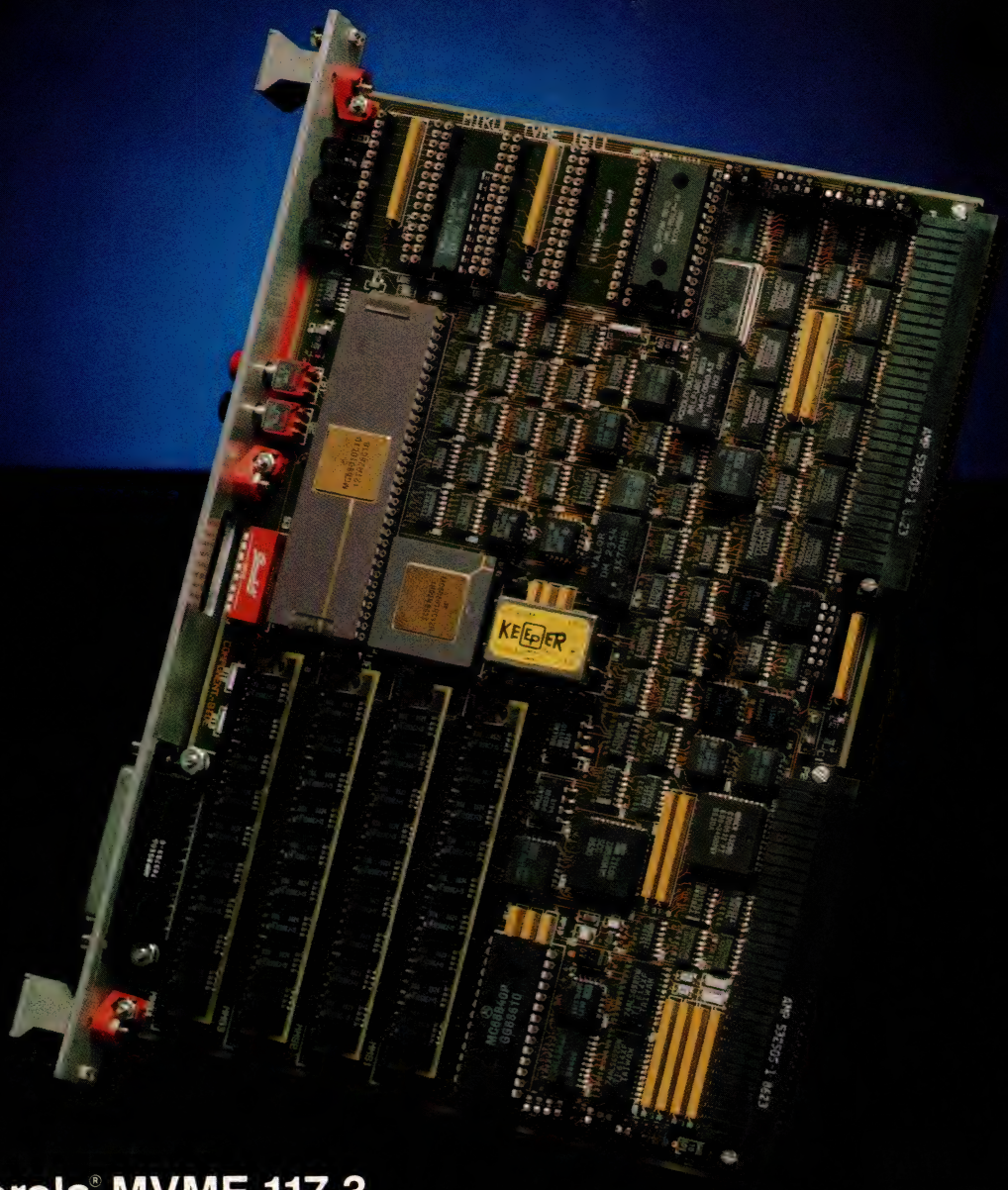

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CIRCLE NO 101

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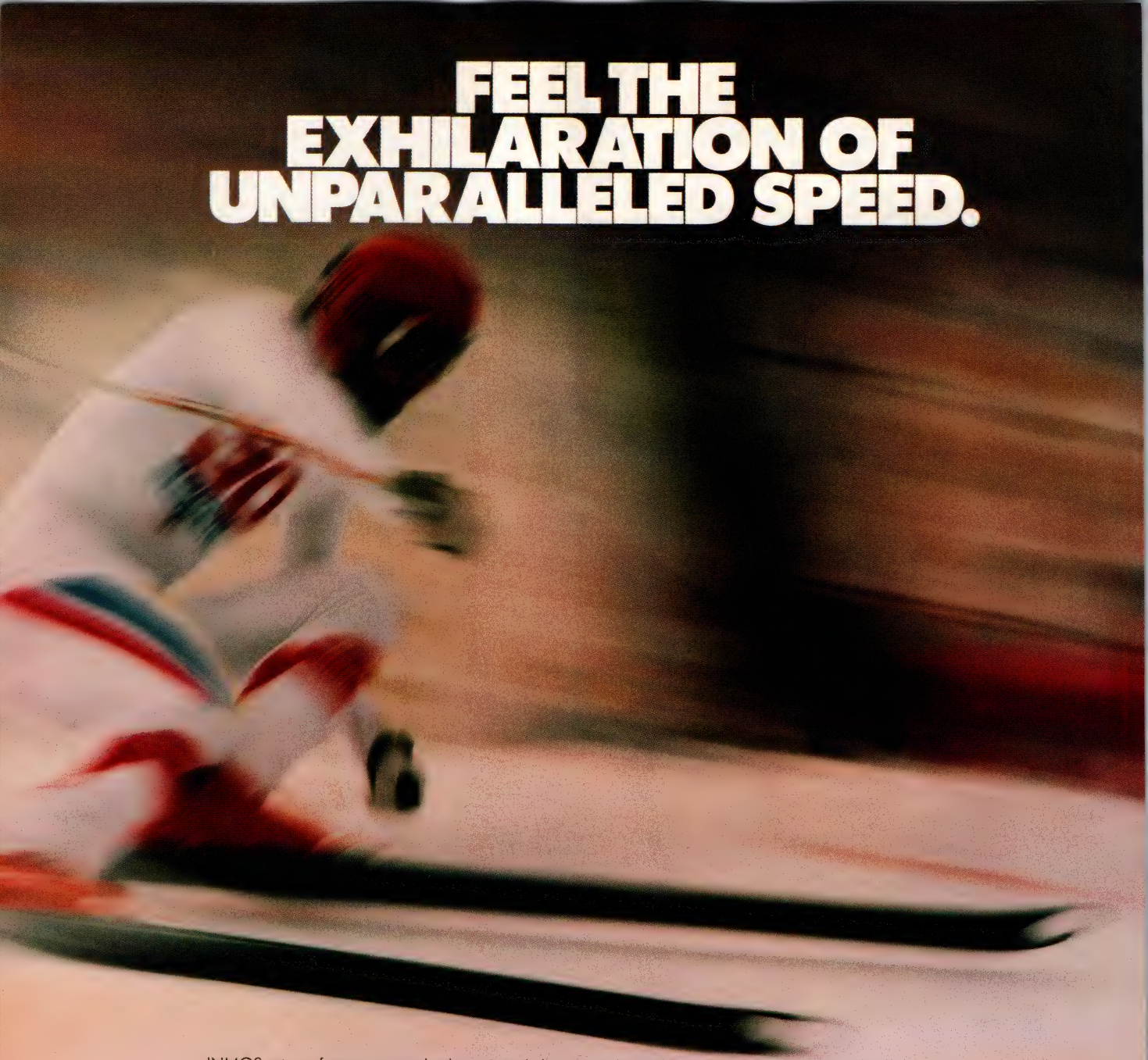

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Part Number	Function	Address Access Time (Max.)	$\overline{RAS}$ Access Time (Max.)	$\overline{RAS}$ Read/Write Cycle Time (Min.)
IMS2800-60*	Static	32ns	60ns	121ns
IMS2800-80	Column	43ns	80ns	146ns
IMS2800-10	Decode	53ns	100ns	176ns

Part Number	Function	Column Access Time (Max.)	$\overline{CAS}$ Access Time (Max.)	Page Mode Cycle Time (Min.)
IMS2801-60*	Enhanced Page Mode	32ns	11ns	35ns
IMS2801-80		43ns	13ns	46ns
IMS2801-10		53ns	16ns	56ns

Data on Nibble Mode and Extended Serial Mode versions available upon request. *Contact factory for delivery. inmos, and IMS are trademarks of the INMOS Group of Companies.

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Tokyo, Japan, Tel. 03-505-2840

CIRCLE NO 102

LM 32900

16-BIT CMOS DSP

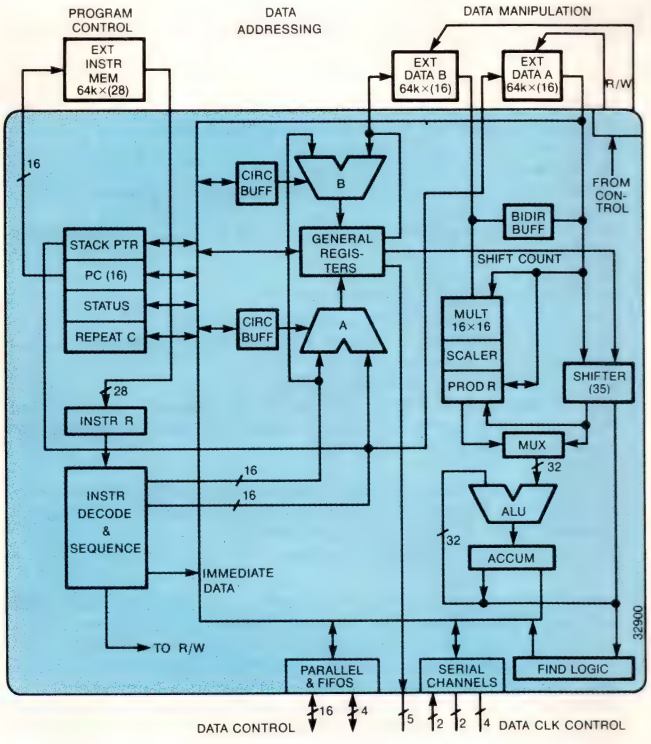
AVAILABILITY: Second half '86 for first silicon (32800 multiplier/ALU half of chip has been available since Jan '86)
COST: Not available but will probably be in the hundreds of dollars initially because die and package are so large
SECOND SOURCE: None announced

Description: 16-bit fixed-point (integer) DSP that accesses all external memories via a large 172-pin package. The external memory spaces are fairly large—the program memory space is 64k×28 bits, and the dual data spaces are 64k×16 each. Expected to have 100-nsec instruction cycle and operate over −55 to +125°C; MIL temperature range. DSP is implemented in static CMOS. Has software commandable power-down mode with wake up from interrupts such as FIFO input buffers full. These features are said to save energy in applications that need only burst-mode processing.

National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95051
Phone (408) 721-5000

Status: This part is from National's linear group, which has been marketing speech chips for many years. The supplier is confident that full 32900 will come out on schedule (samples in fourth quarter) and will meet 100-nsec performance specs (because the multiplier/ALU has been in sample production since the beginning of 86 under part designation LM 32800). But supplier admits the yields of 32800 have been "erratic" and expects the yields of the much larger 32900 (400 mils on side before planned shrink to 300 mils on side) will be low at first. Supplier says best acceptance so far has been with the military, which likes the full temperature range (and power down), and when used in image-processing applications, where the large (all off chip) memory space is desirable.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Adds, subtracts, logicals, absolute, clear and negate
Multiply add and multiply subtract
II—DATA-MOVEMENT INSTRUCTIONS
Addressing via indirection using 8 general-purpose registers as pointers. Instructions to increment and decrement these registers
I/O instructions that specify either FIFOs on parallel ports or shift registers on serial ports.
III—PROGRAM-MANIPULATION INSTR
Repeat counter for iterative instructions
DSP shifting of group of data in external memory via circular buffer mechanism
Conditional and unconditional branches, calls, and returns
IV—PROGRAM-STATUS-MANIPULATION INSTR
14 flags that include ALU-driven status indicator bits and interrupts from internal and external situations
V—POWER-SAVING INSTRUCTIONS
WAIT instruction causes clock to be disconnected from circuitry so chip goes into power-down mode, from which it can be awakened by interrupts (including FIFO full signal from input ports)

Specification summary: μP-like digital-signal-processing chip with all memory outboard. Typical DSP Harvard architecture with third-generation enhancements, such as having dual data memories to simultaneously feed both sides of 16×16=32 integer multiplier, a 32-bit ALU, and a 35-bit shifter. Hardware assists for normalization and block floating point. 20-MHz external clock divided down to 10 MHz on chip, giving 100-nsec cycles for all instructions, including multiply. Generous memory spaces include a 64k×28 program memory and two 64k×16 data memories, each of which has its own RAU (register ALU) for address generation. Efficient asynchronous serial I/O facilitated by two 16×16 FIFOs. 2-μm CMOS with double-layer metallization that is expected to qualify for full speed operation over −55 to +125°C military temperature range. 500-mW operating power drain can be programmed down to 50 mW at standby. 172-pin LCC or PGA package.

HARDWARE — SUPPORT — SOFTWARE

Development board that works with IBM PC, VAX-11/780, or National SYS32000. A National 32016 is used on board as controller for 32900.

Crossassembler for IBM PC (MS-DOS), VAX-11/780 (Unix DSD 4.2). Also being ported to National SYS32000 (GENIX). Simulator runs on IBM PC and is being extended to other hosts. All software tools written in C.

MB8764

16-BIT CMOS DSP

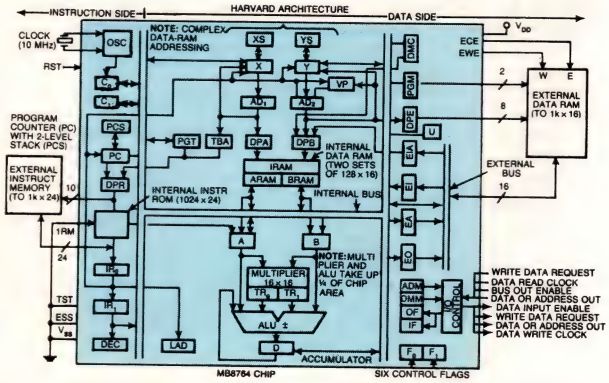
AVAILABILITY: Now for 8764 and 87064. More surface-mount packaging options in '87
COST: For 8764: $70, qty 1; $85, qty 1k; <$40, qty 50k+. For 87064: $35, qty 1k; $27, qty 10k; <$20, qty 50k+
SECOND SOURCE: None planned at this time
CORE: Fujitsu's semicustom group is using 8764 core and tailoring memory and I/O to suit needs of several large telecommunications companies, according to Fujitsu

Description: This has been the fastest single-chip DSP μP available and one of first to be in CMOS, though now will have competition from several new "third-generation" DSPs (see, for example, the 2100, 5010, and 56000 elsewhere in this directory). Compared with second-generation 32010, the 2½-generation 8764 has more raw speed and more parallelism in its architecture so it can "crunch" DSP algorithms twice as fast. The 8764 however starts off with a much larger die size (374×378 mil) and more complex package (88 pins in double-row grid array). Also it needs very fast external memories to operate at full 10-MHz clock speed over temperature. The 87064 version uses the same chip but doesn't bring out buses for accessing external memories; therefore it can be in a smaller 42-pin package and cost less.

Fujitsu Microelectronics Inc
3320 Scott Blvd
Santa Clara, CA 95051
Phone (408) 727-1700

Status: Along with the NEC 7720 and TI 320, this device has been one of the first single-chip DSPs to be used by OEMs, and as such, has helped in the practical definition of this new class of μPs. It hasn't yet reached over a million units/yr as has the other two DSPs—its being used at rate of several 10k/yr in US, according to Fujitsu. But because it is a real, in-production 100-nsec DSP, it may find a niche before the new third-generation DSPs become real and low enough in price to compete. The lower-cost 42-pin version (87064) without access to external memory may help the part maximize this in-between position before the prices of the new third-generation DSPs come down. Meanwhile, as might be expected, Fujitsu is working on its own new fourth-generation "super DSP." This is scheduled for release in '87 and will have a different architecture.

HARDWARE CHARACTERISTICS SOFTWARE



Notes:
1. For full speed, external memories must have 25- to 30-nsec access times.
2. No interrupt, but has DMA for efficient communication with host μP.

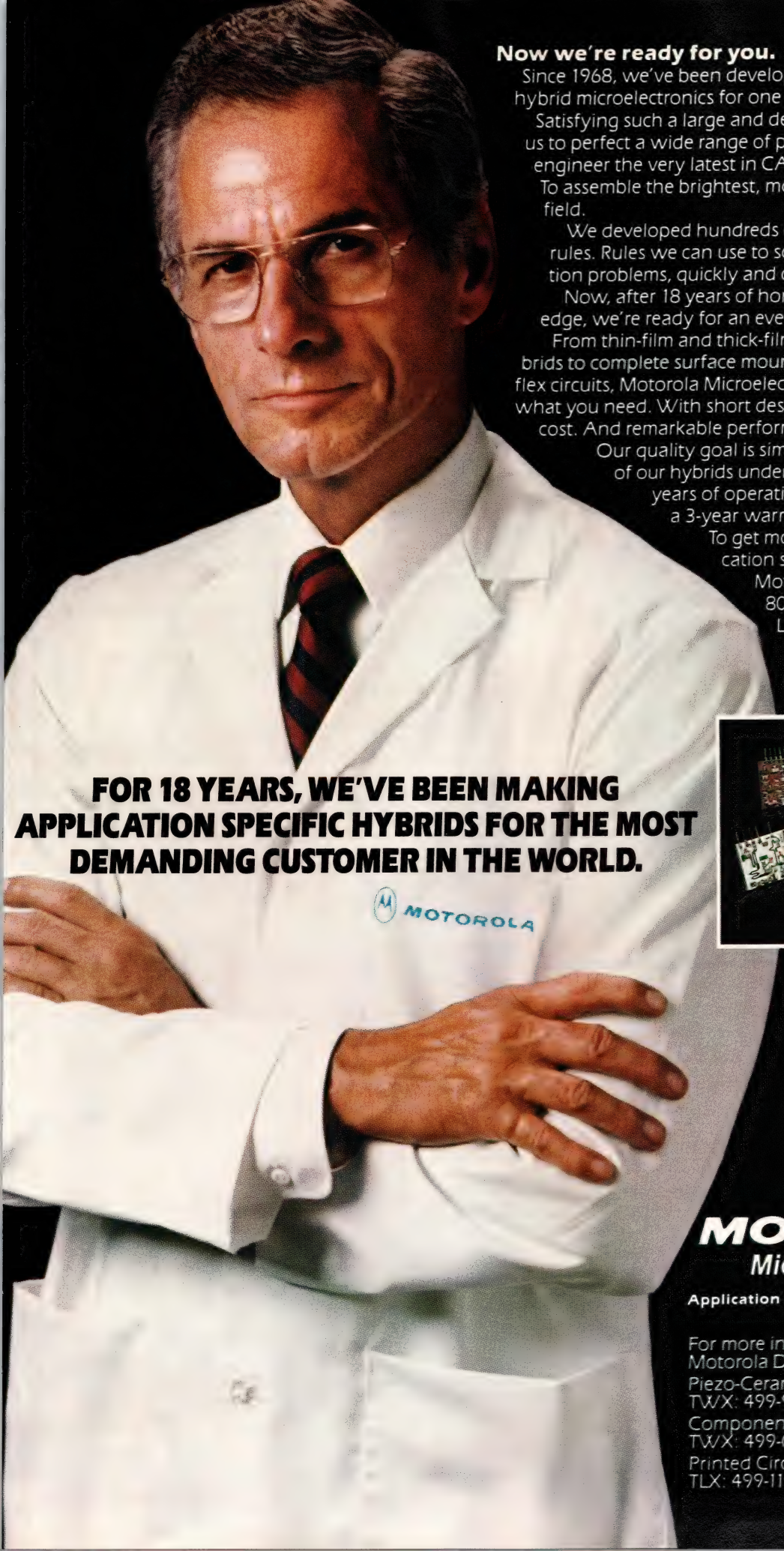
I—DATA-MANIPULATION INSTRUCTIONS
Multiply and divide as well as add and subtract, etc
Some logicals and some shifting ability
II—DATA-MOVEMENT INSTRUCTIONS
Each of two 128×16-bit on-chip RAMs has own independent address-calculation arithmetic
Virtual shift to implement Z^{-1} delay operator is helpful in doing DSP equations
Multiple I/O modes
III—PROGRAM-MANIPULATION INSTR
Conditional and unconditional jumps based on flags
ROM can be used for coefficient table (crossover between separate sides of Harvard architecture)
IV—PROGRAM-STATUS-MANIP INSTR
Has 12 flags for ALU, etc, that are used for conditional instructions, but flags are not grouped into status register for saving (perhaps not needed, as device has no interrupt)
Notes:
1. Some instruction combinations can be compounded for concurrent execution. For example, an arithmetic or logical instruction (category I) can be combined with a move instruction (category II).
2. Data operations handled as fixed-point 2's-complement.

Specification summary: Single-chip digital processor. Has 1k×24-bit program ROM and two 128×16-bit data RAMs on chip. Expandable to 4k×24 bits (via bank switching) and 1k×16 bits, respectively. Has 100-nsec instruction cycles including 16×16=26 multiply (plus accumulate) and 26/16=16 divide. Fabricated in 2.3- to 2.8-μm silicon-gate CMOS with two levels of metallization. One 5V supply, consuming 300 mW at full speed (30 mW/MHz). 88-pin grid array package for 8764 and 42-pin plastic DIP for 87064 with 44-pin PLCC for '87.

HARDWARE SUPPORT SOFTWARE

Evaluation board (FDSP kit 8764) supported on Fujitsu FM-16S, an 8086-based personal computer that runs CP/M-86. Evaluation board has external memories intended to be downloaded by host. Hardware manual (February '84).

Assembler and simulator for IBM PC ($285) and VAX/Unix and VAX/VMS ($500). Programming manual (March '84), instruction set manual (edition 1.1, March '84), and new approximately 50-page application manual.
Note: Original Software Development Tool Kit (MB87902) consisting of crossassembler (ASM64) to run on Fujitsu FM-16S personal computer (CP/M-86), the evaluation board mentioned under hardware support (FDSP kit 8764), and monitor program (MON64).



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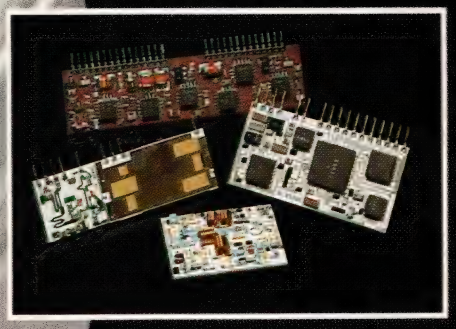

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CIRCLE NO 103

ADSP 2100

16-BIT CMOS DSP

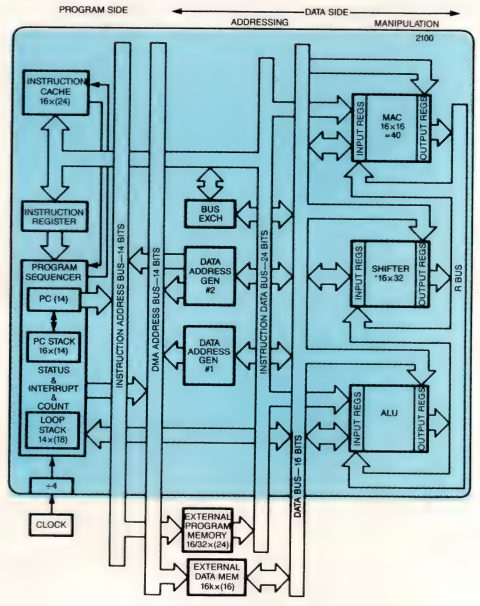
AVAILABILITY: Samples since first quarter '86, production fourth quarter '86.
COST: $375 for single units; $295, 100 qty
SECOND SOURCE: Under discussion

Description: A μP-like 16-bit DSP chip that is to be used with external memory. The supplier says it has patterned the architecture after popular configurations in bit-slice-DSP approaches. As result, DSP experts will probably find the subsystem sections—the program control, the data-address generation, the data crunching—have familiar features. Supplier says device is advantageous when larger memory spaces are required because chip is able to run full speed even when accessing data off chip. Ideally the critical software loops should be running out of on-chip cache so that the two data operands can be accessed simultaneously, one from data memory and the other from program memory.

Analog Devices Inc
Digital Signal Processing Div
1 Technology Way
Norwood, MA 02062
Phone (617) 329-4700

Status: This device is one of the first of the third-generation 16-bit fixed point DSPs to become available and to have good support. The 2100 will have a lot of competition. Similar devices are being introduced by Philips/Signetics (5010), National (32900), and Motorola (24-bit fixed-point 56000). This device's price should be attractive; it has a moderate die size (90k sq mils) as compared to the over 100k sq mils of some other DSP devices. But it doesn't have features like serial I/O that will found in some of its competitors.

HARDWARE CHARACTERISTICS SOFTWARE



Note:
1. Only main chip subsystem blocks and main buses are shown. Actual chip is much more complex than indicated.

I—DATA-MANIPULATION INSTRUCTIONS
Three main groups of instructions that control the operations of the multiply/accumulator, shifter, and ALU. Most of these can be made conditional

II—DATA-MOVEMENT INSTRUCTIONS
Data can be moved quite flexibly between the approximately two dozen register locations on chip and between these registers and external memories. Both direct and indirect addressing are available for many of these instructions

III—PROGRAM-MANIPULATION INSTR
JUMP, CALL and RETURN from subroutine, RETURN from interrupt, DO UNTIL, and TRAP. All can be made conditional

IV—PROGRAM-STATUS-MANIPULATION INSTR
A large number of status registers are maintained: 8-bit ALU status, 8-bit stack status, 5-bits for interrupt (plus 4 bits for interrupt mask). Some of these are used for determining decisions in program-manipulation instructions

V—PROGRAM MODE CONTROL INSTRUCTIONS
4-bit mode-control register allows software selection of desirable DSP options such as bit reversal in addressing and saturation-mode arithmetic

Notes:
1. As is common in highly parallel DSP architectures, instructions can combine functions from groups I, II, and III. However, because instruction word is only moderately long (24 bits), only certain combinations are valid.
2. Supplier describes assembly language as "high-level" because it is patterned after Fortran and C, using an algebraic-like notation. This is said to ease programming. It makes the functions being performed intuitively obvious.

Specification summary: Harvard architecture μP with program and data memory off chip. There is, however, a 16×24-bit program-memory cache on chip that is said to be adequate for holding short routines (such as DSP inner loops). A 14-bit PC to address 16k instruction words off chip (optionally 32k) and 14-bit data address generators allow addressing 16k×16 data words off chip. Access time for external memory: 50 nsec for program and 55 nsec for data. When a program loop is executing from cache, both operands can be read in simultaneously: the signal data from data space and the coefficient from program space. Loop counters and special stacks are provided for "zero-overhead" execution of typical DSP recursive operations. Data-crunching section includes the three elements typical of DSP devices: a 16×16=40 multiplier, a 32-bit barrel shifter (facilitates block floating point), and a 16-bit ALU. All instructions including compound data-manipulation/data-movements/program-manipulation executed in 125 nsec. I/O is memory-mapped, and control signals are available so a host μP can access the program memory via DMA. Fabricated in 1.5-μm CMOS with double-metal interconnect layers. Die size is 280×230 mils. Packaged in 100-pin ceramic PGA.

HARDWARE SUPPORT SOFTWARE

Stand-alone emulator ($6500) for real-time tests of software and hardware. Connects to host μP via RS-232C. Uses same interactive and symbolic user interface as software simulator. Evaluation board being readied.

Cross software tools for VAX (VMS and Unix) and IBM PC (MS-DOS). Includes system builder for defining target hardware details, assembler, linker, and software simulator. The simulator uses the same interactive and symbolic user interface as the hardware simulator (emulator). Cost of multiuser VAX is $2850; cost for single-user IBM PC is $450 for assembler, linker, and system builder; $975 for simulator.

PCB 5010/11 (SP-50 FAMILY)

16-BIT CMOS DSP

AVAILABILITY: Samples for 5011 with production first quarter '87. Production for 5010, second quarter '87
COST: $195 for 5011 samples; $45 in 1k qty for 5010
SECOND SOURCE: To be announced

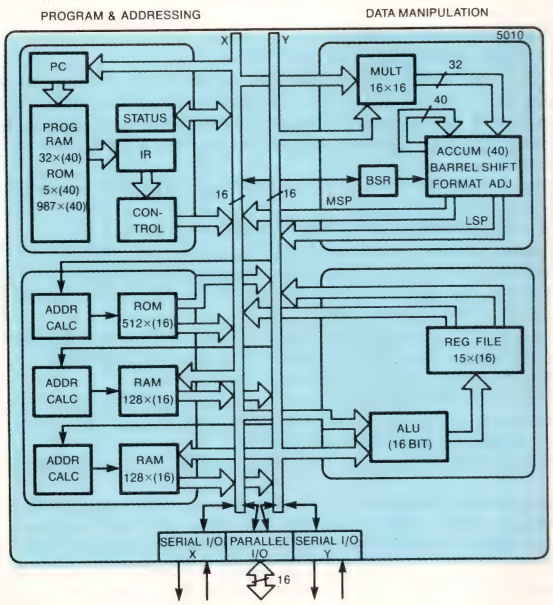
Philips
Elcoma Corp Center
Box 218
5600 MD Eindhoven, The Netherlands
31 40 724223

Signetics Corp
Box 3409
Sunnyvale, CA 94088
Phone (408) 991-2000

Description: Another example of pushing DSP-oriented architecture to its logical limit. The design aim appears to be to keep the die and package size moderate (in DSP terms) for reasonable device cost. At same time, designers wanted to achieve third-generation performance (beyond second-generation TI 32010), so a very wide control word (40 bits) and dual data paths are used.

Status: This part was announced at February '86 ISSCC conference, so it can be assumed that mostly working silicon has been available since the first quarter '86. Supplier says it has gone through three iterations on chip and expects to have fully functional, full-speed parts by the fourth quarter '86. Supplier expects to extend family upwards and downwards and to add analog interfaces.

HARDWARE CHARACTERISTICS SOFTWARE



Notes:
1. 5010 is one-chip μC with limited 1k×40 program ROM. Its data-side memory space can be expanded off chip.
2. 5011 is ROMless μP version of 5011 that has large 64k×40 off-chip program memory space.

I—DATA-MANIPULATION INSTRUCTIONS
45 multiply/accumulate and 31 ALU operations
II—DATA-MOVEMENT INSTRUCTIONS
Extensive movements between blocks of chip with selection of pathways
III—PROGRAM-MANIPULATION INSTR
4 branches with 50 different conditions
IV—PROGRAM-STATUS-MANIPULATION INSTR
All 16-bits of status word are active, giving wide range of conditions for decisions
Notes:
1. The many fields of wide instruction word provide an orthogonal matrix of software options that are said to make DSP operation flexible and programming simple.
2. User can choose either pipelined or nonpipelined mode via software control.

Specification summary: Harvard architecture with entirely separate program and data sides. High degree of parallelism. Control side has 40-bit-wide control word that allows up to 6 operations to be performed simultaneously. Data side has dual 128×16 RAMs and dual 16-bit buses so that both operands can be presented simultaneously to 16×16=40 multiplier and 16-bit ALU. Each data RAM and an additional 512×16 data ROM has its own address computation ALU. A 3-port 15×16 register file aids data movements and frees buses. The instruction cycle is 125 nsec (8 MIPS) for all instructions including multiply (although the one, two, or four optional levels of pipelining can mean a delay at beginning of a series of DSP instructions). Fabricated in 2-μm CMOS with die size approximately 370-mil sq. Packaged in 68-pin PLCC (5010) and 144-pin PGA (5011).

HARDWARE SUPPORT SOFTWARE

Stand-alone debug station (SDS) with real-time emulation capability ($3995) will be available in fourth quarter '86. Incorporating a special bonded-out version of 5011, SDS is claimed to have fully transparent performance (all device functions available). Also a prototyping board ($1995).

Crossassemblers that will run on VAX/VMS ($3995) or IBM PC ($995). Standard macro library covering single- and double-precision arithmetic and complex arithmetic; and bit manipulation, initialization and I/O. DSP functions such as FIR and IIR filters and FFTs is included in VAX package, but is extra for IBM PC ($995). Software simulators for VAX/VMS ($5200) and IBM PC ($1995).

DSP 56000 FAMILY

24-BIT CMOS DSP

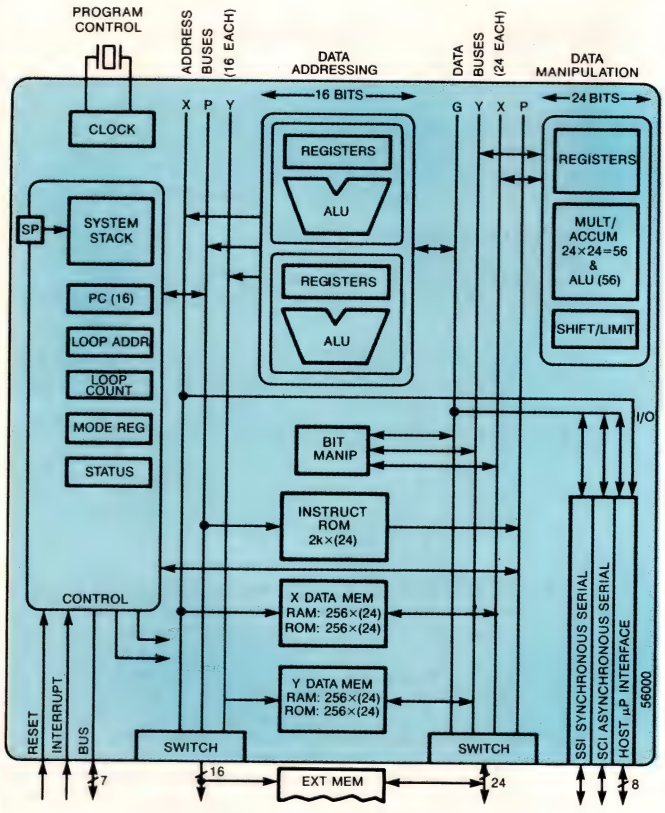
AVAILABILITY: RAM-based 56001 samples in first quarter '87; ROM-based 56000 will follow in '87
COST: $500 for RAM-based 56001 samples. There will be a nonrecurring mask charge for ROM-based 56000
SECOND SOURCE: None announced

Motorola Integrated Circuits Div
3501 Ed Bluestein Blvd
Austin, TX 78721
Phone (512) 928-6000

Description: A 24-bit fixed-point-arithmetic CMOS DSP (mostly one-chip) family. First members will be a ROM-based model (56000) that requires factory programming. A RAM-based model (56001) will be somewhat unusual among 1-chip devices: The program-memory space is in on-chip RAM. The architecture follows recent trends among DSPs in that it has the program-control, data-addressing, and data-manipulation functions in separate subsystem so that each can operate in parallel with the others. Note that this is first μP device in directory to have balanced 24-bit widths for both instruction and data words for parallel control and analog precision, respectively. An unusually large assortment of on-chip peripheral functions are included on chip, after the fashion of microcontroller μCs such as Motorola's 6805 and 6801 families.

Status: Motorola says it is on schedule and expects samples of the RAM-based 56001 version (program RAM on chip) first quarter '87. The ROM-based 56000 (program ROM on chip) will be available later in '87. Speed is projected at 97.5 nsec per instruction cycle, making it competitive with other DSPs. However, it's difficult to compare speeds, because most makers are continually promising die shrinks. (Motorola is talking of going under 1.5 μm) with attendent speed increases. The die shrinks are needed as much to bring the die sizes down for reasonable parts costs as they are needed for increased speed). Motorola claims that several major coporations have designed in the 56000/1 and will announce products in '87. Motorola says its design wins have been due to "56000's high throughput, programming ease, minimum need for surrounding glue parts, and development-system support."

HARDWARE CHARACTERISTICS SOFTWARE



Notes:
1. Diagram is for 56001 program-in-RAM version.
2. The 56000 program-in-ROM is identical except for:
a) Program memory=2k ROM.
b) X,Y data ROMs are customer-specified.
c) No bootstrap ROM.
3. There are 18 interrupt sources, which are serviced in 200 nsec).
4. No speed penalty for single external-memory accesses.

I—DATA-MANIPULATION INSTRUCTIONS
Special instructions for ALU include absolute value, compare magnitude, divide iteration, normalization iteration, round (to nearest even), Multiply/Accumulate with Round. All A&L instructions execute in one cycle, and parallel data moves are allowed with all but 5 of the 35 instructions
Bit manipulation (useful for I/O decisions)
II—DATA-MOVEMENT INSTRUCTIONS
Five MOVE instructions: LUA, load updated address pointer; MOVE, parallel data move; MOVEC, move control register; MOVEP, move peripheral data (memory to memory); MOVEM, move program memory (used to access internal program memory on 56001 for instructions or data)
Data moves are allowed in parallel with all but 5 of the 35 data-manipulation instructions
III—PROGRAM-MANIPULATION INSTR
Special DSP-algorithm instructions for control subsystem include Repeat-the-next-instruction-N-times and stop-the-clock-and-wait-for-interrupt (with clock to peripherals). Both of these cause device to go into low power dissipation mode
Program loops via DO and ENDO instructions (replace space-wasting straightline code). DO loops are interruptable and nestable
IV—PROGRAM-STATUS-MANIPULATION INSTR
16 status bits that can be used as basis for program-manipulation instruction decisions (JUMP, etc), and control of operating modes
V—POWER-SAVING INSTRUCTIONS
STOP and WAIT instructions, similar to those in supplier's 6805

Specification summary: Single-chip device with divided Harvard architecture carried to point that there are three separate subsystems that can operate independently and in parallel for increased throughput. Program control subsystem implements a 3-stage instruction pipeline, allowing instructions to be fetched, decoded, and executed concurrently. On-chip program memory is 512×(24). Available either as masked ROM (56000) or as user-downloadable RAM (56001). Expandable off chip to 64k instruction words. Data-side memory divided into two separate spaces for simultaneously feeding in the two operands needed by ALU. Each of these on-chip data spaces has 256×(24) RAM, 256×(24) ROM, and its own separate addressing arithmetic. The address arithmetic can operate in linear, modulo, or reverse carry modes (as needed in DSP) and contains 24 16-bit address registers. The data ALU contains a nonpipelined multiplier/accumulator with four 24-bit input registers and two 56-bit accumulators. It performs 24-bit fixed-point arithmetic but has wide 56-bit data paths. Rate of instruction performance is 10.25 MHz (97.5-nsec instruction cycle). This is 10.75 MIPS if taken literally or the equivalent of 70 MIPS if all the parallelism is taken into account. Three I/Os include an 8-bit parallel bus interface to a host μP with DMA; a serial communications port with baud-rate generator; and a CODEC port with clock generator.

HARDWARE SUPPORT SOFTWARE

From Motorola: Evaluation Module (EVM) consisting of an interface board and evaluation board (EVB) with diskette ($1000 to $2500). The host is an IBM PC in which the interface board occupies one slot. Because third-party DSP applications software exists for the PC and the EVM user interface is the same as the simulator user interface, the PC+EVM combination offers an algothithm-development environment as opposed to just a hardware/software development environment. The EVM is, logically, based on the 56001 and will be available with the part in the first quarter '87.
From third parties: To be announced.

From Motorola: User-friendly assembler and simulator which run on IBM PC under MS DOS ($295), on VAX under VMS, and on Sun-3 workstation under Unix 4.2. The 56000 assembler is an absolute assembler that supports source-code linking and macros. The 56000 simulator simulates on a clock-cycle basis as opposed to just an instruction-cycle basis. Each of the execution subsystems is simulated individually, as are each of the on-chip peripherals. A C compiler that will take advantage of the regularity of the instruction set is scheduled for release in '87.
Documentation available: *56000 User's Manual,* 1986, a ⅞-in. thick paperback covering hardware and software, and a 16-pg technical data folder.
From third parties: To be announced.

77230

32-BIT FLOATING-POINT AND 24-BIT FIXED-POINT CMOS DSP

AVAILABILITY: Now for samples of 77230 (with prerecorded ROM for customer evaluation); second quarter '87 for samples of 77220. ROM codes now being accepted
COST: For 10k qty, from $80 to $100 for 77230; $60 to $80 for 77220. Probably won't go much below $40 even in large volumes in next few years because of large die and package
SECOND SOURCE: Actively being pursued with Zilog one US possibility

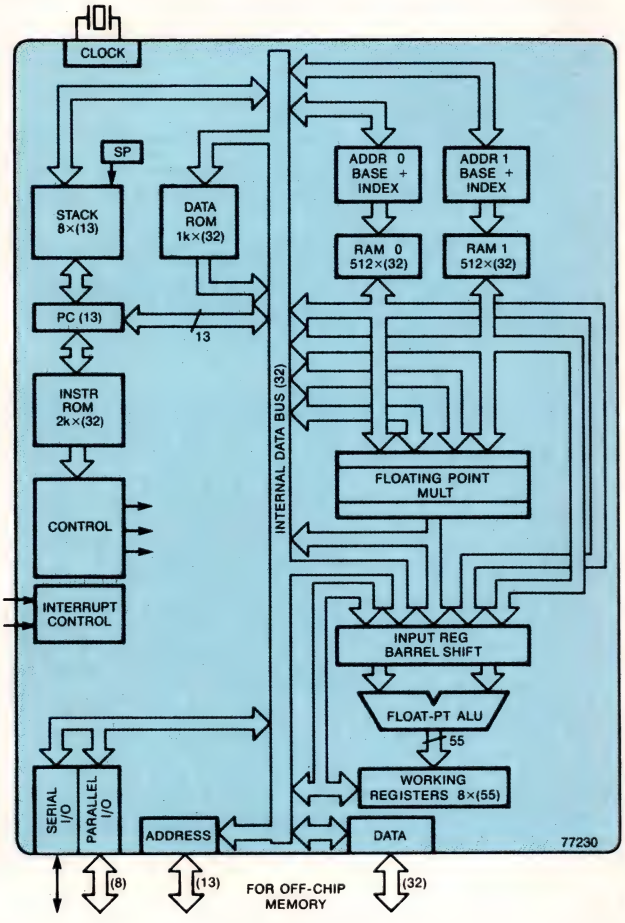
NEC Electronics Inc
(Corporate Headquarters)
401 Ellis St
Mountain View, CA 94039
Phone (415) 960-6000

NEC Electronics Inc
Natick Technology Center
1 Natick Executive Park
Natick, MA 01760
Phone (617) 655-8833

Description: 32-bit floating-point μP/μC intended for audio-bandwidth, digital-signal-processing, and similar number-crunching applications. Features a 24×24=47 multiplier and a 55-bit wide ALU. The 77230 has companion version, the 77220, that is 24-bit fixed point.

Status: Announced at the February '86 ISSCC conference, the device has been more or less in silicon as of that time (a requirement for ISSCC presentation). At time of writing, samples that were said to be fully functional, and full-speed ones had been received in US. It competes with AT&T's somewhat similar 32-bit floating-point DSP chip (see elsewhere in this directory). Although the chip is quite large (315×591=186k sq mils), NEC expects to price it as low as $60 to $80 in 10k volume in '87. NEC says it is finding interest for the floating-point 77230 from designers of graphics and imaging systems and workstations. The fixed-point 77220 interests telecommunications designers.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Floating-point and fixed-point add and subtract
Logicals
N-bit shift
Data rounding and normalization
Data conversions between floating and fixed point and to IEEE format
II—DATA-MOVEMENT INSTRUCTIONS
Source-register to destination-register transfers
External memory access
III—PROGRAM-MANIPULATION INSTR
Branch and conditional branch, with conditions based on state of ALU-driven status bits, index registers, and serial and parallel ports
Subroutine call and return
Loop counter control (decrement)
IV—PROGRAM-STATUS-MANIPULATION INSTR
Operations on PSW
Note:
1. As is common in DSPs, the wide (32-bit) instruction word has many different fields, each pertaining to a different class of operations. Thus instructions are combinations of the above classes of instructions, and during an instruction cycle, a number of operations may go on in parallel.

Specification summary: 32-bit floating-point DSP-oriented, Harvard split-memory architecture with both on-chip and off-chip program and data memories. Program memory is 2k×32 bits on chip and 4k×32 bits off chip. Data memory is composed of a 1k×32 RAM and 1k×32 ROM on chip and 8k×32 bits off chip. The 32-bit program instruction word is divided into multiple fields for simultaneous control of data manipulation, data movement, and program manipulation. The 32-bit data word is divided into a 24-bit mantissa and an 8-bit exponent, but the option for 24-bit fixed-point operation is also provided. Much of device area is taken up with powerful multiplier, ALU, and special ALUs for address generation. Both inputs of 24×24=47 multiplier can be fed simultaneously from dual data memories. The output can be fed to a 47-bit barrel shifter and then on to a 55-bit-wide ALU (8-bit exponent added) and eight 55-bit working registers. All instructions including multiply execute in one 150-nsec cycle. 32-bit parallel I/O and 5-MHz serial I/O. Fabricated in 1.5-μm CMOS, consuming 1.7W power. Packaged in 68-pin PGA. The 7720 is same architecture but with just 24-bit fixed point for lower cost.

HARDWARE — SUPPORT — SOFTWARE

Evakit 77230 emulator (price not determined but probably in the thousands of dollars).

Relocatable assembler, librarian, linker, etc, for MS-DOS and CP/M-86 systems. Also a powerful simulator that runs on VAX/VMS, priced at about $1000.

DSP32

32-BIT FLOATING-POINT NMOS AND CMOS DSP

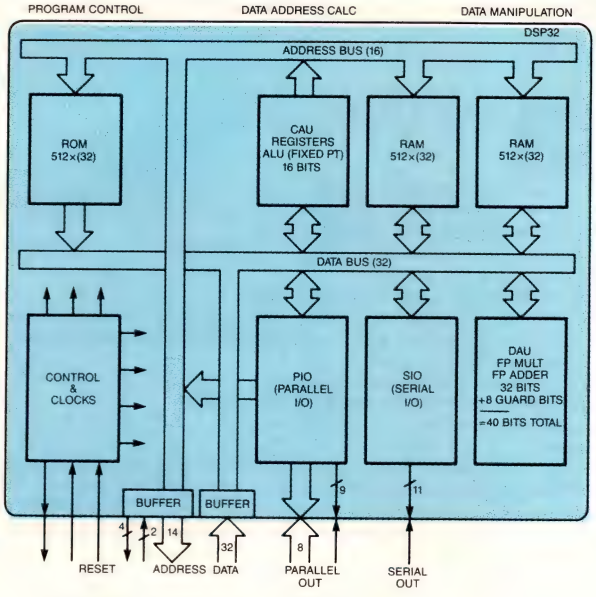
AVAILABILITY: Now for production. (Being used in high volume by AT&T internally.) CMOS version first quarter '88
COST: 100 qty prices in '87 for 100-pin package will be $200 for 250-nsec part and $270 for 160-nsec part. High-volume prices will be $153 and $190, respectively
SECOND SOURCE: Being actively pursued

AT&T
555 Union Blvd
Allentown, PA 18103
Phone (215) 439-7317

Description: 32-bit floating-point NMOS DSP μP/μC with transparent normalization after operations. Has both on-chip and off-chip memory. Has parallel (8-bit) ports and serial ports, the latter being CODEC compatible. (Floating point said to be especially desirable for graphic applications and large FFTs where there is danger of overflow or loss of accuracy during computations.)

Status: Originally disclosed at the February '85 ISSCC, this was the first 32-bit floating-point DSP to become real (about a year ahead of the NEC 77230, which is just now becoming available). This shouldn't be surprising because AT&T has long been the leader in both DSP theory and practice. The part is said to be in volume use inside AT&T (probably 100k units in '87, because it is being used in electronic switching systems). AT&T is giving 1-day design seminars on DSP32 to help convince OEM designers that it is serious about outside sales. It will also bring out a higher-speed version of the NMOS part in '87 and a finer-geometry CMOS version in the first quarter '88.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Can run full speed with external memory but memory access time must be 80 nsec (for 250-nsec speed).
2. Two arithmetic units:
a) The DAU (data arithmetic unit), which performs 32-bit floating-point DSP computations and is heavily pipelined.
b) The CAU (control arithmetic unit), which performs 16-bit fixed-point operations to generate the complex addressing typical of DSP (especially when doing FFTs), as well as doing integer arithmetic. It is not pipelined, so it can quickly respond to branch decisions.

I—DATA-MANIPULATION INSTRUCTIONS
Instructions for the DAU, which performs the main DSP multiply/accumulate computations in floating point. (Transparent normalization after operations to maintain floating-point accuracy)
Instructions for the CAU, which performs 16-bit fixed-point computations such as add, subtract, logicals, and shift
II—DATA-MOVEMENT INSTRUCTIONS
Instructions for the CAU, which does data-address computations
III—PROGRAM-MANIPULATION INSTR
Instructions for the CAU, which performs program-address computations
IV—PROGRAM-STATUS-MANIPULATION INSTR
Status conditions monitored include status of DAU and CAU and I/O
Notes:
1. Assembly-language syntax intended to resemble high-level language like C to ease task of converting DSP algorithms to code.
2. As with most DSPs, the wide instruction word has separate fields for the various categories of instructions so that more than one category can be performed during an instruction cycle.

Specification summary: 32-bit Harvard architecture with separate sections that can operate in parallel for increased throughput. On-chip program memory (2k bytes) arranged as 512×(32). On-chip data memory (4k bytes) arranged in two 512×(32) RAMs. Off-chip memory space is 56k×(32); off-chip memories must have fast access times to keep up with full-speed operation of chip (80 nsec for 250-nsec cycle). Has 32-bit multiplier that can simultaneously receive inputs from two data RAMs and deliver result for addition to 40-bit accumulator (32-bits plus 8 bits to guard against overflow) all in same cycle. This multiplier/accumulator combination (plus associated registers is called the DAU). In addition has 16-bit fixed-point ALU for usual integer operations plus computing addresses for both program and data side of Harvard architecture. This ALU plus associated registers is called the CAU. 250-nsec instruction cycles with 16-MHz clock. This gives 8 MIPS for multiply/accumulator operations (in DAU) and 4 MIPS for 16-bit integer operations (in CAU). Higher-speed version with 160-nsec cycle time will be available in '87. Serial and parallel I/O ports. Both have provisions for user-implemented DMA. Serial port is compatible with CODECs. Fabricated in 1.5-μm NMOS with single metal layer. Chip size 500×250 mils. Consumes 1.7W average, 2.6W worst case. Packaged in 40-pin DIP and 100-pin PGA (need 100-pin package for external memory). CMOS version will have improved speed power.

HARDWARE — SUPPORT — SOFTWARE

Single board development system ($3000) allows real-time testing. Note: Because AT&T has been designing DSP32 into applications in house for several years now, good development tools should exist, though type of tools AT&T might use in house might be more expensive than some smaller OEMs could afford.

Assembler with C-language-like syntax, linker, editor, and simulator. Latter is architectural simulator with appearance of high-level language. Software tools operate on Unix V ($1000) and MS-DOS ($500); VMS version planned.

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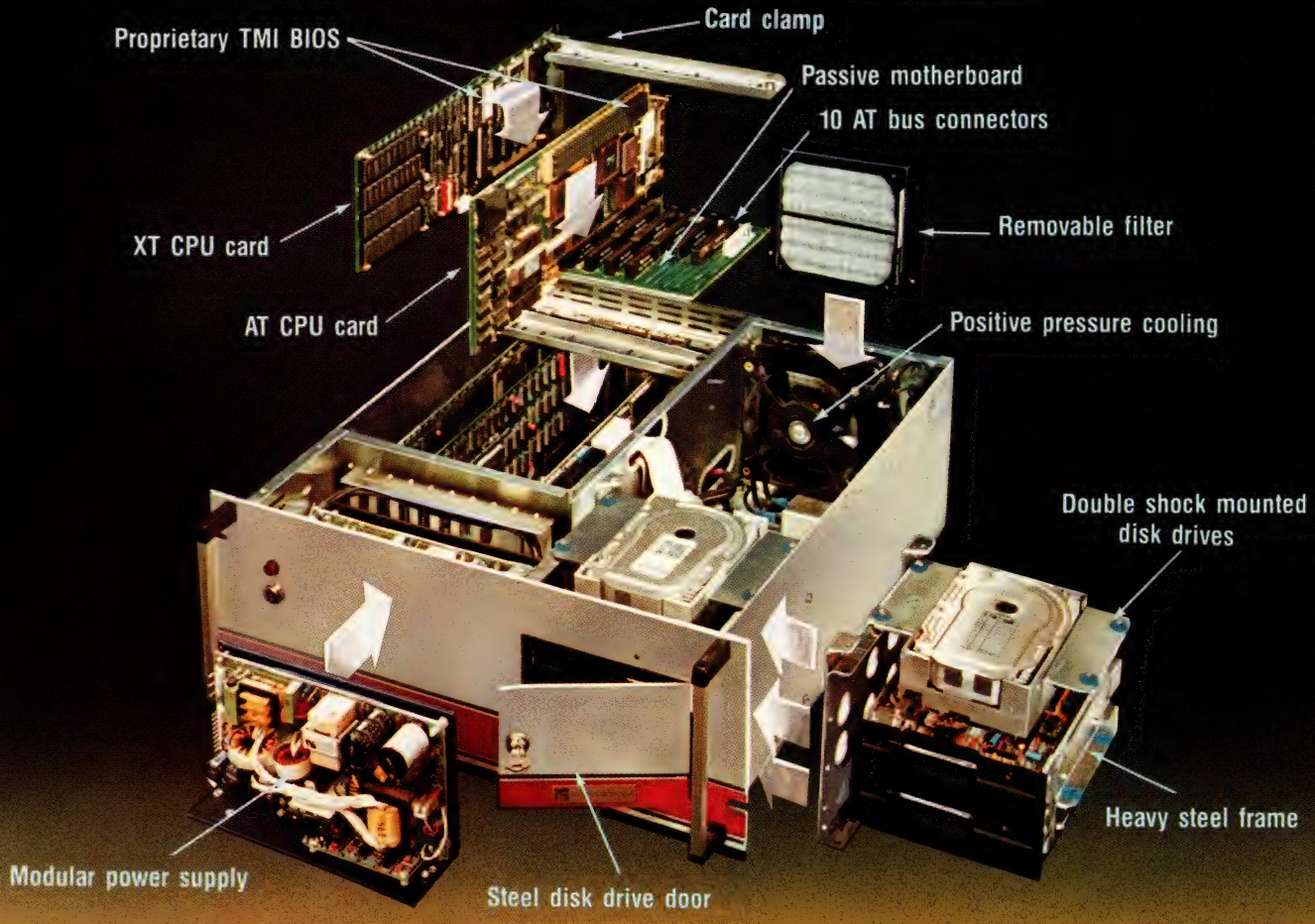

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CIRCLE NO 105

WORD-SLICE DSP

16-BIT CMOS DSP

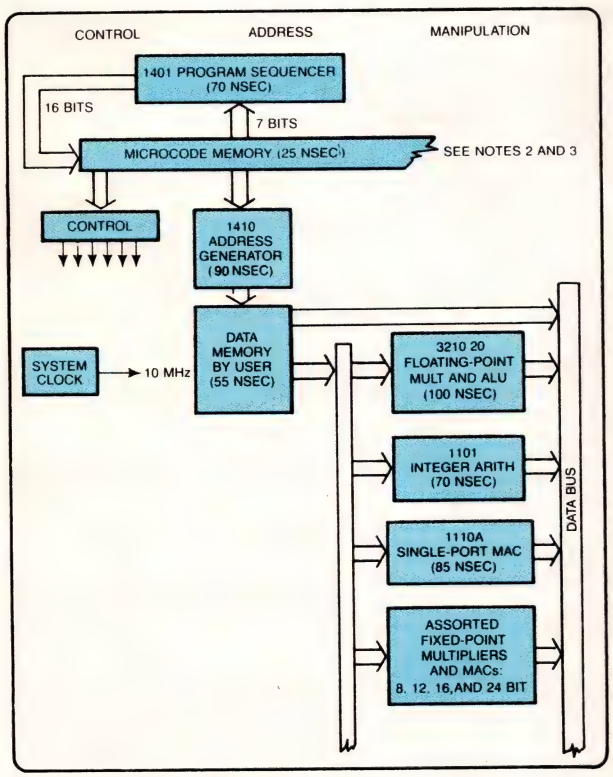
AVAILABILITY: Now for most parts; see table
COST: $37 to $300; see table
SECOND SOURCE: No direct source, except for industry-standard multipliers. Similar functions are available from AMD, Cypress Semiconductor (San Jose, CA), Integrated Device Technology (Santa Clara, CA), Wafer Scale Integration (Fremont, CA), Weitek (Sunnyvale, CA), and others.

Description: Follows trend established with 2900 bit-slice family of providing building blocks that system designers can use in microprogrammed systems. This family is intended for digital-signal-processing applications but its parts are also applicable to other types of numeric or number-crunching applications, such as accelerators. Supplier's goal was to provide microprogram sequencers and address generators that could be used with supplier's floating- and fixed-point multipliers to design complete systems.

Analog Devices Inc
Digital Signal Processing Div
1 Technology Way
Norwood, MA 02062
Phone (617) 461-3881

Status: Supplier says early response to its Word-Slice and floating-point chips has been very positive because of "high performance, low power, and functional integration," but admits that for systems with lesser performance requirements, competition is coming from programmable DSP single-chip or few-chip DSP processors like TI's 320 family and supplier's own 2100.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Architecture shown is only one of many possibilities.
2. Microcode memory can be up to 64k deep. It can be as wide as designer needs for simultaneous control of one or more data pipes (typically approximately 100 bits).
3. Microcode memory can be RAM for downloading of algorithms from a host.

I—DATA-MANIPULATION INSTRUCTIONS
For ADSP-1101 integer arithmetic unit:
Add and subtract, multiply, multiply and accumulate (MAC). Conditional multiply and accumulate
Dual accumulator control and internal feedback
Logical and shifts
Block floating point
For ADSP-3210/20 floating-point multiplier and ALU:
Multiply single-precision floating point, double-precision floating point, and 32-bit fixed point
Complete arithmetic and logical ALU operations
Complete format conversions operations
II—DATA-MOVEMENT INSTRUCTIONS
For ADSP-1410 address generator:
Pre-update and post-update modes conditional looping (zero overhead)
Add or subract increments or offsets to pointers
Register transfers
Logicals and shifts
Bit-reverse output (for FFT)
III & IV—PROGRAM-MANIPULATION AND -STATUS INSTR
For ADSP-1401 program sequencer:
Jump and branch-absolute, relative and indirect
Push, pop data, counters and pointers to subroutine stacks
Modify subroutine stack and register stack pointers
Interrupt masking and control
Write control store (for downloading)

Specification summary: Microprogrammable chips set for digital signal processing and similar numerical processing. Consists of various multipliers and multiplier accumulators (see table) and microcode program sequences and address generators (see table). It can be driven by a 10-MHz clock, and within the resulting 100-nsec cycle, can perform complete instructions (obtain data from memory and process it). Architecture slanted towards digital signal processing and permits increasing throughput by increasing parallelism. Sequencer helps a host computer download code into a RAM microprogram store. Fabricated in CMOS.

PART	DESCRIPTION	AVAILABILITY	COST (100 QTY)
3210	FLOATING-POINT MULTIPLIER	NOW	$300
3220	FLOATING-POINT ALU	NOW	$300
1401	PROGRAM SEQUENCER	NOW	$57
1410	ADDRESS GENERATOR	NOW	$37
1110A	16-BIT SINGLE-PORT MAC	NOW	$37
1101	16-BIT INTEGER ARITH	NOW	$175
1080A	8-BIT 2'S-COMPL MULT	NOW	$27
1081A	8-BIT UNSIGNED MULT	NOW	$27
1012A	12-BIT MULT	NOW	$42
1016A	16-BIT MULT	NOW	$45
1024A	24-BIT MULT	NOW	$93
1008A	8-BIT MAC	NOW	$41
1009A	12-BIT MAC	NOW	$53
1010A	16-BIT MAC	NOW	$56

HARDWARE — SUPPORT — SOFTWARE

Supplier recommends the same approach to development systems as used with bit-slice microcoded components (ie, the AMD 2900 family). Suitable ROM-simulation systems are available from Step Engineering (Sunnyvale, CA) and HiLevel Technology (Tustin, CA). Similar aids are offered by Tektronix and Hewlett-Packard.

Mnemonics with microcode fields are available from the supplier for use with a meta assembler. These programs can be used by a designer to create a design-dependent assembly-level language. Step Engineering and HiLevel Technology meta-assemblers support parts via definition files for Word Slice mnemonics.

7281 Data Flow DSP

16-BIT NMOS AND CMOS DSP

AVAILABILITY: Now for NMOS. CMOS fourth quarter '87
COST: For 7281, $100 in 100 qty; $65 in 1k qty. For 9305, $35 each and $25 in 1k qty
SECOND SOURCE: None announced

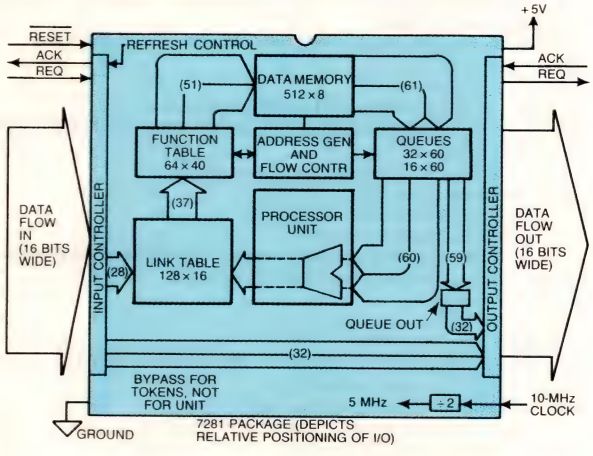
NEC Electronics Inc
(Corporate Headquarters)
401 Ellis St
Mountain View, CA 94039
Phone (415) 960-6000

NEC Electronics Inc
Natick Technology Center
1 Natick Executive Park
Natick, MA 01760
Phone (617) 655-8833

Description: First VLSI implementation of data-flow architecture, which is said to be ideal for programming data-flow graphs. Especially suited for computations with large amounts of concurrency. One example is image processing; another is array processing. Single units can achieve 5 MIPS and multiple units can be used in cascade or ring structures for increased computing throughput; for example, 14 units can be used together to achieve 70 MIPS, according to NEC.

Status: NEC's educational program during the spring and summer of '86 has convinced the company that there is a market for this device in USA despite its unorthodox, "data-flow" architecture. NEC said it had an average attendence of 100 OEM designers at each of the thirty 7281 technical application seminars it gave in the US. Over 100 of NEC's 7281 evaluation kits were purchased ($900 each), NEC said. Besides the intended image-processing applications for the 7281, NEC says that the designers were interested in multiple 7281's for low-cost array-processor accelerator boards for personal computers. To this point, most of the 10k/month production of 7281 has gone to about 180 customers in Japan, according to NEC.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Diagram emphasizes difference between the data-flow architecture and more familiar von Neumann architecture. Note that with the exception of system clock and reset, there's only a 16-bit-wide input and a 16-bit-wide output and associated handshaking controls.
2. Programming instructions are downloaded via the input into the FT and LT blocks immediately after reset (or before a given batch of data is to be processed).
3. In operation, 32-bit-wide "tokens" flow in and out as sequential tandem 16-bit words, of which 16 bits are data and the rest are fields that tell where the data is to be processed.

I—DATA-MANIPULATION INSTRUCTIONS
(32 instructions for processor unit)
Multiply, add, and subtract
Compound multiply, add, or subtract with shift count
Compare, compare exchange, compare normalize
Full set of logicals
Bit manipulation and check
Convert sign magnitude to 2's-complement and vice versa
Double-precision adjust
Cumulative addition
II & III—DATA-MOVEMENT & PROGRAM-MANIP INSTR
(16 instructions for address-generator/flow-control unit)
Cyclic read and cyclic write
Read modify write
Read with index
Count, divide, distribute, and cut tokens
Token synchronization
Output tokens (note: no input instructions)
Program control done by altering token ID's field
(Note: Count instruction in address-generator/flow-control unit is equivalent to loop count)
IV—PROGRAM-STATUS-MANIP INSTR
No flags as such, but decisions are reflected in fields of PU instructions
Notes:
1. Instructions intended for implementing data-flow diagram.
2. See hardware notes for indication of how unusual the software approach for this machine must be.

Specification summary: Implements data-flow architecture. 16-bit data words enter as 32-bit tokens that include control information. Internally, there is a 7-stage pipelined computing ring in which pairs of operands are queued for processing in processor unit. At 200 nsec per stage, 7-stage ring takes 1.4 μsec. Single 5V NMOS part housed in 40-pin DIP. The 9305 Magic interface chip is housed in a 132-pin PGA. Devices can be cascaded or put in ring structures for increased throughput.

HARDWARE — SUPPORT — SOFTWARE

7281 Execution System: hardware simulation system containing four 7281s, one 9305, one 7720, and 512k bytes of memory. Allows users to test and debug their programs in hardware.
Promotional kit: four 7281s, two 9305, plus crossassembler and simulator software to run on IBM PC ($900).
IBM PC-compatible evaluation board under development (fourth quarter '86).
The 9305 is a 132-pin CMOS peripheral support chip developed to simplify 7281 designs. It will connect up to eight 7281s to a host μP and to local (image) memory. Replaces about 80 MSI/SSI parts.
Note that the 7281 has debug and breakpoint modes, which help the user see what is going on inside the chip. These modes are invoked by their own special instructions.

Crossassembler of the "functional" type allows users to translate data-flow graphs into 7281 object code. Software simulator that provides complete information on the internal and external operations of the 7281. These tools run under CP/M-86, MP/M-86, MS-DOS, VAX VMS, or Unix/Ultrix.
Application libraries containing programs for binary and gray-scale image processing and numerical calculations. Will include basic image-processing functions such as rotation, zoom, pattern recognition, and edge detection. It will also contain LP and HP filters (both FIR and IIR types) and FFTs. Application notes and user manuals.
NEC has applications engineers familiar with 7281 in both its East and West Coast offices.

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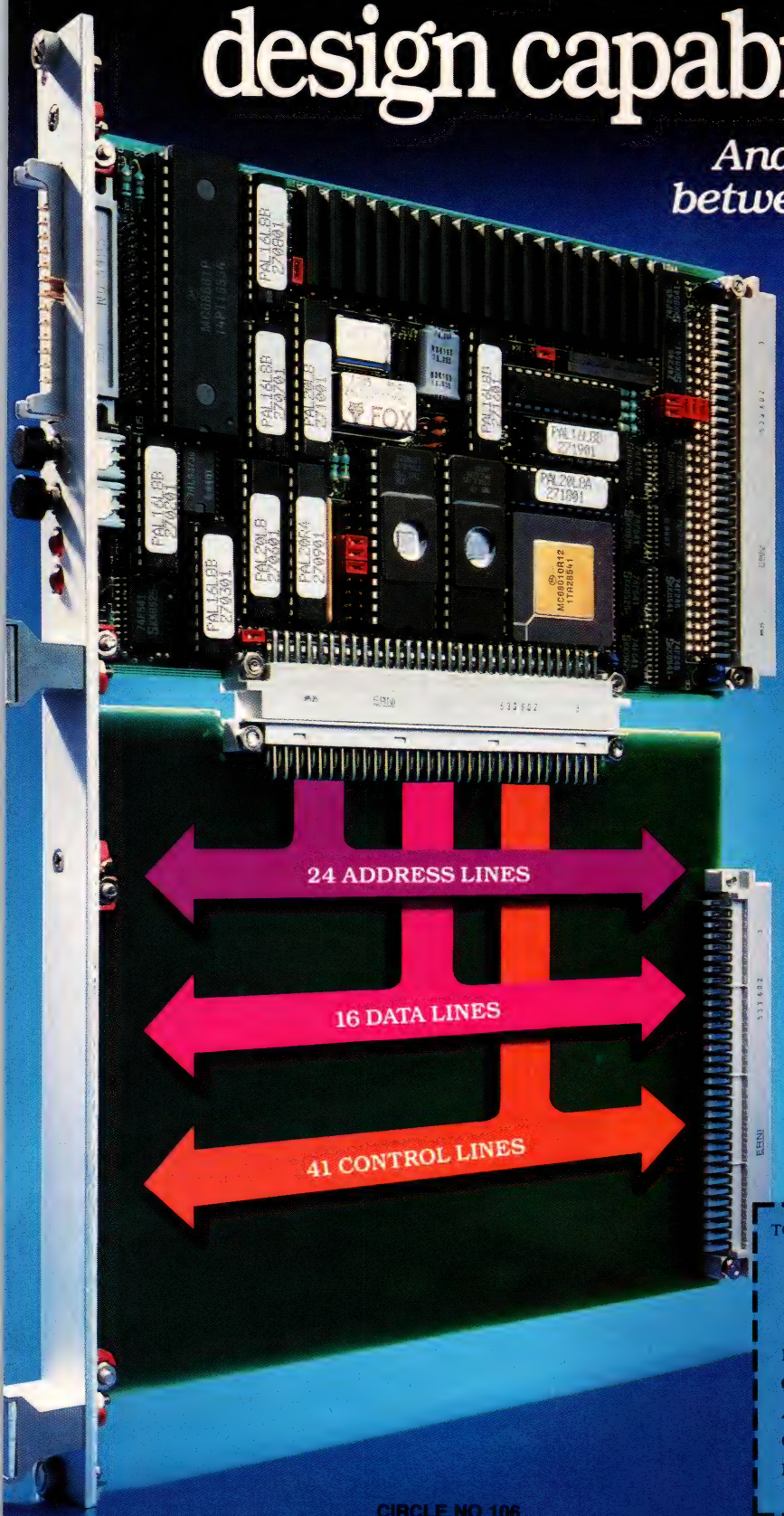

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EDN112786

CIRCLE NO 106

A100 DSP

16-BIT CMOS DSP

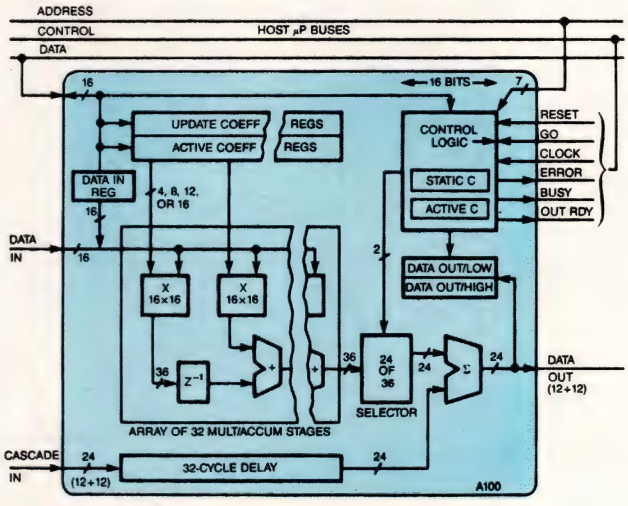
AVAILABILITY: Sample versions of 20-MHz part said to be available since summer '86. Full product availability, fourth quarter '86
COST: $406 in 100 qty. Volume pricing projected to be <$100 in 18 months
SECOND SOURCE: Not yet announced

Inmos Corp
Box 16000
Colorado Springs, CO 80935
Phone (303) 630-4000

Description: Coprocessor optimized to implement digital filtering, correlation and convolution algorithms. Uses multiple 16×16 multipliers to implement 32 taps of transversal filter and achieve the equivalent of 3 nsec per tap (ie, low video bandwidth) with 4-bit coefficients. Coefficients of 8, 12, and full 16 bits can also be selected with corresponding slowdowns of speed. Two banks of coefficient registers allow adaptive modification on the fly. A 36-bit result is accumulated, of which 24-bits may be selected for output or passed down to a cascade of similar devices.

Status: Along with somewhat similar products from TRW and Zoran, this is a "vector" processor optimized for DSP. The dedicated, mostly hardwired, architecture with its "brute-force" paralleling of multipliers allows video sampling rates in contrast to the audio sampling rates of programmable general-purpose DSP chips (such as TI 320 or NEC 77230). Supplier expects full video sample rate parts (30 MHz) by early '87. It's an example of one type of definitely non-von Neumann architecture that may be necessary for faster processing of certain classes of algorithms. Progress in VLSI will make this sort of heavy-on-hardware approach even more feasible.

HARDWARE CHARACTERISTICS SOFTWARE



Notes:
1. In contrast to usual FIR filter diagram the pipeline delays (Z^{-1}) are incorporated after the coefficient multipliers.
2. The similarity of diagram to graphic description of algorithm is not accidental. This hardware-biased approach gives more speed but less versatility.

I—DATA-MANIPULATION INSTRUCTIONS
Hardwired 32-stage compound signed multiply/accumulate with 24 of 36-bit output range select
II & III—DATA-MOVEMENT & PROGRAM-MANIP INSTRUCTIONS
In data mode can use data input pins/write to data input register
Update either coefficient register bank (active update).
IV—PROGRAM-STATUS-MANIPULATION INSTR
Initiate bank swap
Continuous bank swap mode
Notes:
1. Coprocessor requires external control from μP or sequencer. "Programing" is via loading appropriate bit patterns into memory-mapped control registers.
2. Adaptive filtering can be achieved by changing the coefficient values.

Specification summary: Cascadable single-chip modified transversal filter integrating 32 parallel multiply/accumulator stages. Supports two's-complement signed 16×16 multiplication with full precision 36-bit accumulation. Coefficients selectable as 4, 8, 12, or 16 bits for throughput rates from 10M to 2.5M samples per second (at 20-MHz clock). Two coefficient banks allow adaptive and complex filtering. 24 bits of the 36-bit accumulation can be selected for output. This output can be cascaded down a pipeline of A100 devices. Fabricated in 1.5-μm CMOS, consuming <1.5W. Packaged in 84-pin ceramic PGA. Military and full video sample rate (30-MHz) parts are projected.

HARDWARE SUPPORT SOFTWARE

IBM PC-compatible evaluation board (IMS-B009) to be available in fourth quarter '86. It will contain four cascadable A100s, a T414 32-bit Transputer μP with 1M-byte fast DRAM, a T212 16-bit Transputer μP with 64k bytes of fast static RAM, and a C002 link adapter to interface to PC bus.

Software (in Occam language) for supplier's Transputer μP systems. Includes model of A100 for logical simulation and coefficient-generation tools for automatic, interactive development of desired filter characteristics or Fourier transforms. The application notes for A100 appear to be helpful for DSP generally, perhaps because of the direct and obvious match between the A100 and DSP algorithms.

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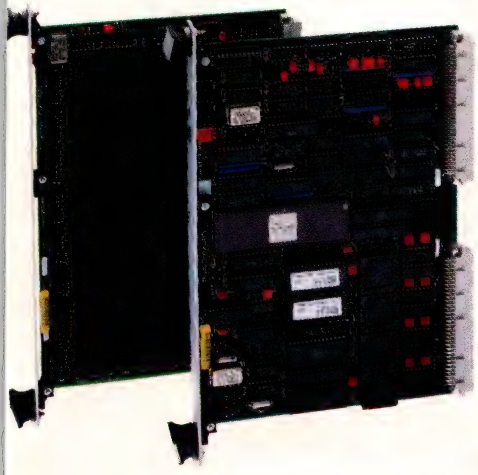

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CEO, SBE, Inc.

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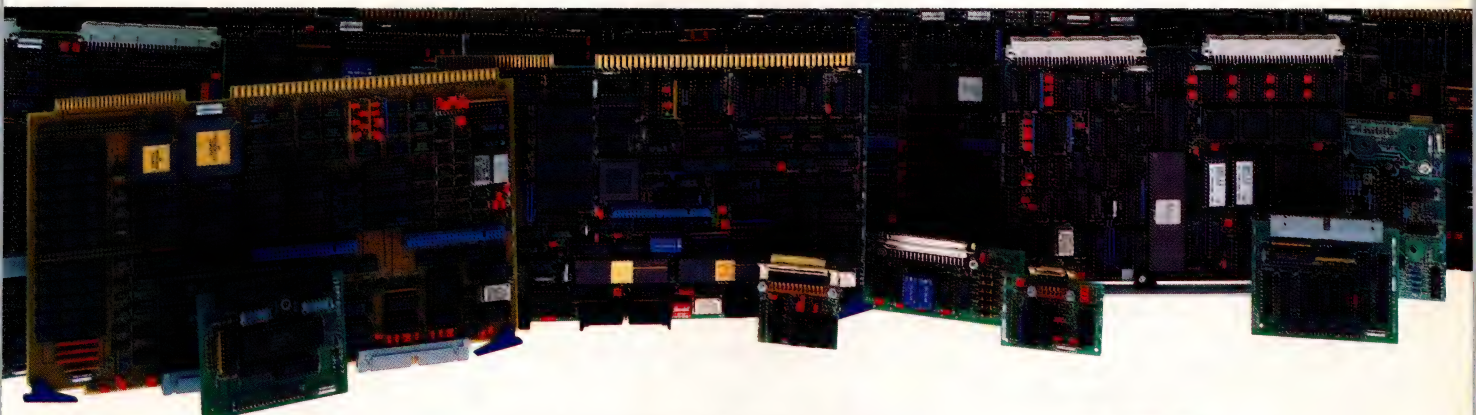

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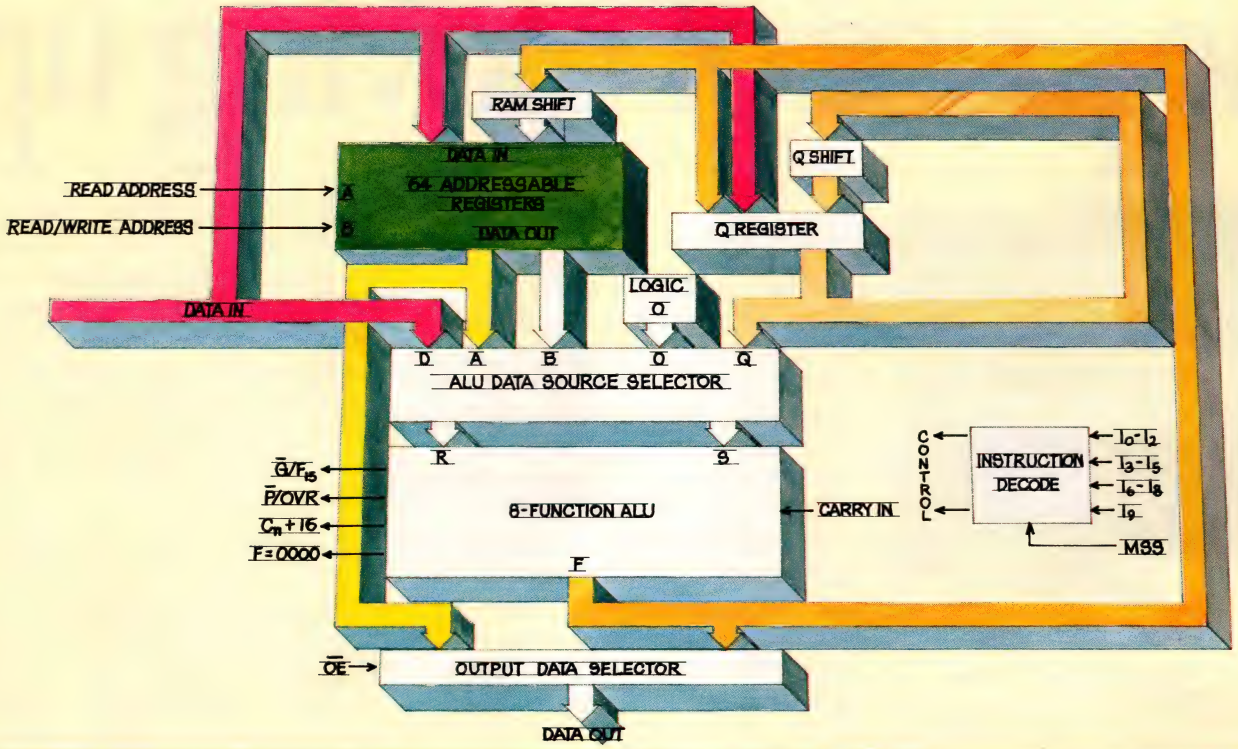
16-bit 2901
64 registers, 20 MIPS



Use the IDT49C402A 16-bit slice to architect a fast, 20 MIPS data path.

High-performance features like ABI to Y and flags of 37ns make 20 MIPs a reality.

ABI to Y = 37ns ☐ Faster system performance than any quad 2901 (30% faster than four of the fastest 2901s and a 2902A) ☐ 64 registers ☐ eight new destination paths ☐ 2901 instruction set ☐ cascadable ☐ higher fanout than 2901 ☐ denser packaging solutions.

More RAM means fewer cycles. The IDT49C402A has a 64-word x 16-bit two-port register RAM. Four times more registers than any other quad 2901.

The ultimate in parallel architecture. Eight new destination functions control an additional data bus to improve overall speed. You now have the flexibility of inputting data directly to the on-board RAM or Q register while performing ALU operations and outputting data at data out and flags.

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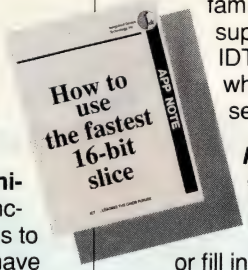

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IDT39C01E	World's fastest 4-bit Slice	2901
IDT39C03A/B	4-bit Slice	2903
IDT39C203/A	4-bit Slice	29203
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IDT39C10B/C	12-bit	2910
IDT39C09A/B	4-bit	2909
IDT39C11A/B	4-bit	2911
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CIRCLE NO 108

External hardware augments low-cost display controller

A single-chip μP driving a display-controller chip set yields a CRT terminal with a minimal parts count. The display-controller chip set itself brings several sophisticated features to your system, and you can add even more features with a handful of inexpensive logic chips.

Juergen Stelbrink, *Advanced Micro Devices Inc*

Miniaturization and falling prices of ICs have rendered the so-called "dumb" terminal a relic; it's easy and inexpensive to design intelligence into a display. The low-cost terminal design described in this article provides a variety of features through the use of a standard 8-bit single-chip μP from the 8051 family (the 8751) and a CRT-controller chip set (the Am8052 and Am8152A). A small amount of additional circuitry provides horizontal smooth scrolling and italic characters.

The display-controller chip set is optimized for alphanumeric displays. The set has on-chip functions for windowing, vertical smooth scrolling, and proportional spacing, as well as such attributes as blinking, underlined, double-width, reverse-video, and highlighted characters. (Caution: Do not confuse the 8052 display controller with the enhanced member of the 8051 single-chip μP family that, unfortunately, has the same part number.)

The 8751 single-chip μP, without any extra circuitry, handles terminal overhead that, in the past, an entire system would have handled. The μP interfaces with the keyboard, communicates with the host computer via its on-chip asynchronous port, interprets the display commands, and generates a display list for the 8052. To allow the μP's on-chip baud-rate circuitry to generate standard baud rates, such as 300, 1200, 9600, and 19,200 baud, the μP's clock frequency is 11.059 MHz (11.059 MHz÷12÷16÷3=19,200 Hz).

Because the keyboard sends a scan code instead of an ASCII character, the terminal's μP must use a look-up table to convert the scan code to ASCII format. One advantage of the look-up-table approach is that simply by changing the look-up table, the keyboard becomes programmable. A programmable keyboard is important if your design calls for user-definable function keys or foreign-key arrangements.

Display information in RAM

A 16k-byte static RAM stores all display information. The 8751 addresses this memory as 16k bytes. Because the 8052 has a word-wide data interface, it addresses this memory as 8k words (**Fig 1**). A bidirectional latch allows the 8751 to access the upper byte of memory and the 16-bit registers of the 8052.

The 8751 single-chip μP, without any extra circuitry, handles terminal overhead that, in the past, an entire system would have handled.

To execute a 16-bit register write, the 8751 first writes the upper byte to a latch. In a second cycle, the 8751 writes the lower byte directly into the 8052 while the latch supplies the upper byte. The 8751 reads a 16-bit register in the same fashion. In the first cycle, the 8751 reads the 8052's register, loading the low byte directly into the 8751, while a latch temporarily holds the upper byte. The 8751 can then read this latched byte in its second cycle.

Bus arbitration in software

Unlike many standard μPs, the 8751 does not provide any hardware for bus-arbitration operations, such as a bus-request and -acknowledge handshake. Consequently, software must perform the bus arbitration, because both the 8751 and the 8052 need to have access to the display memory.

The 8052 must load its 132-character internal line buffers with rows of characters from the display memory. It initiates this action by asserting its bus-request line and thereby interrupting the 8751. The 8751's interrupt service routine then sets the chip's address/data bus (ports 0 and 2) to a high-impedance state and grants the bus to the 8052 by asserting P1.2. While the 8052 performs its display-memory access operations, the 8751 monitors the on-chip serial interface and the bus request of the 8052. As soon as the 8052 releases the bus, the 8751 regains control over the display memory.

Though your product could use windows in a variety of more imaginative ways, consider by way of example the case in which the terminal displays two windows concurrently. The first window appears simply as a message line on the bottom row of the display. Once activated, the message line will stay in place independently of any scrolling in the remainder of the screen.

Application programs can pop the second window up in the middle of the screen to show temporarily required information. Pointer modification performs selection and deselection of windows. You need not move any display data.

The display chip performs two types of scrolling.

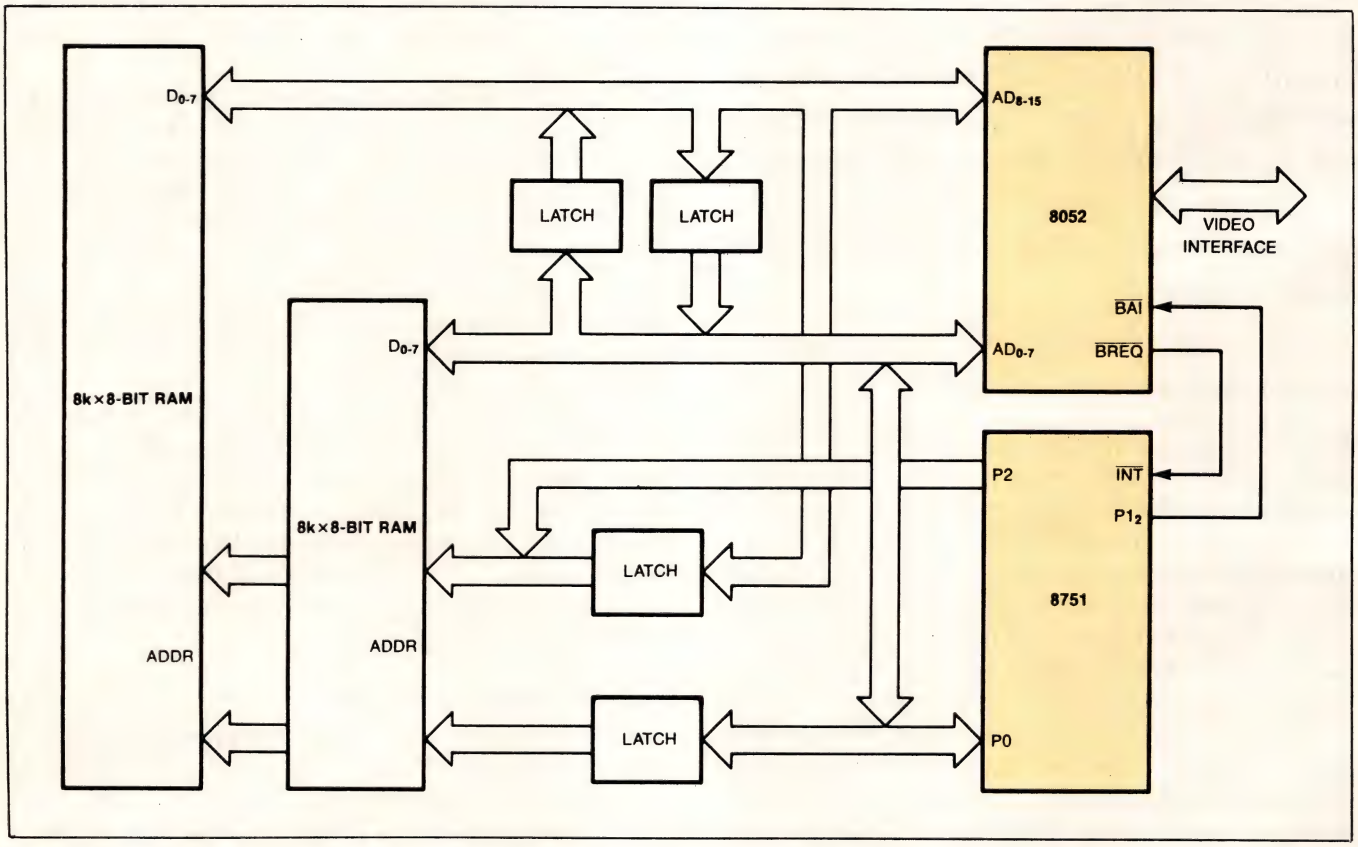


Fig 1—The 8052 display-controller chip reads 16-bit words *from the video RAM. The 8-bit, single-chip 8751 μP requires extra latches to address the same memory.*

First, the 8052 allows jump-scrolling, where character rows are replaced on a row-by-row basis. The result is a jagged movement of the text. Smooth scrolling overcomes this annoying effect. By replacing character rows gradually, scan line by scan line (that is, pixel line by pixel line), the system scrolls in a slow, smooth, eye-pleasing motion. You can adjust the scroll rate within a wide range, from very slow rates, where the scan line replacement is noticeable, to very fast rates, which create the same effect as jump scrolling.

Variable screen formats

Many applications require a feature that allows the terminal user to dynamically change the number of characters displayed on the screen. In word-processing applications, a screen format of 80 characters horizontally is sufficient because most documents use about 65 columns of characters. This width leaves some space for format-control information. In programming applications, however, programmers often need more than 80 columns. A typical listing file, for example, uses 132 columns.

The design described here offers two screen formats. In the normal mode, it displays 24 rows (plus one status row), with 80 characters per row. Character cells of 7×9 pixels, spaced at 9×14-pixel intervals, yield a resolution of 720×350 pixels. The IBM PC Monochrome Adapter has these same parameters.

In the compressed mode, the system displays 30 rows (plus one status row), with 120 characters per row. In this mode, cells of 5×7 pixels spaced at 6×11-pixel intervals define the characters. This spacing yields approximately the same pixel resolution (720×341) as the normal mode (720×350).

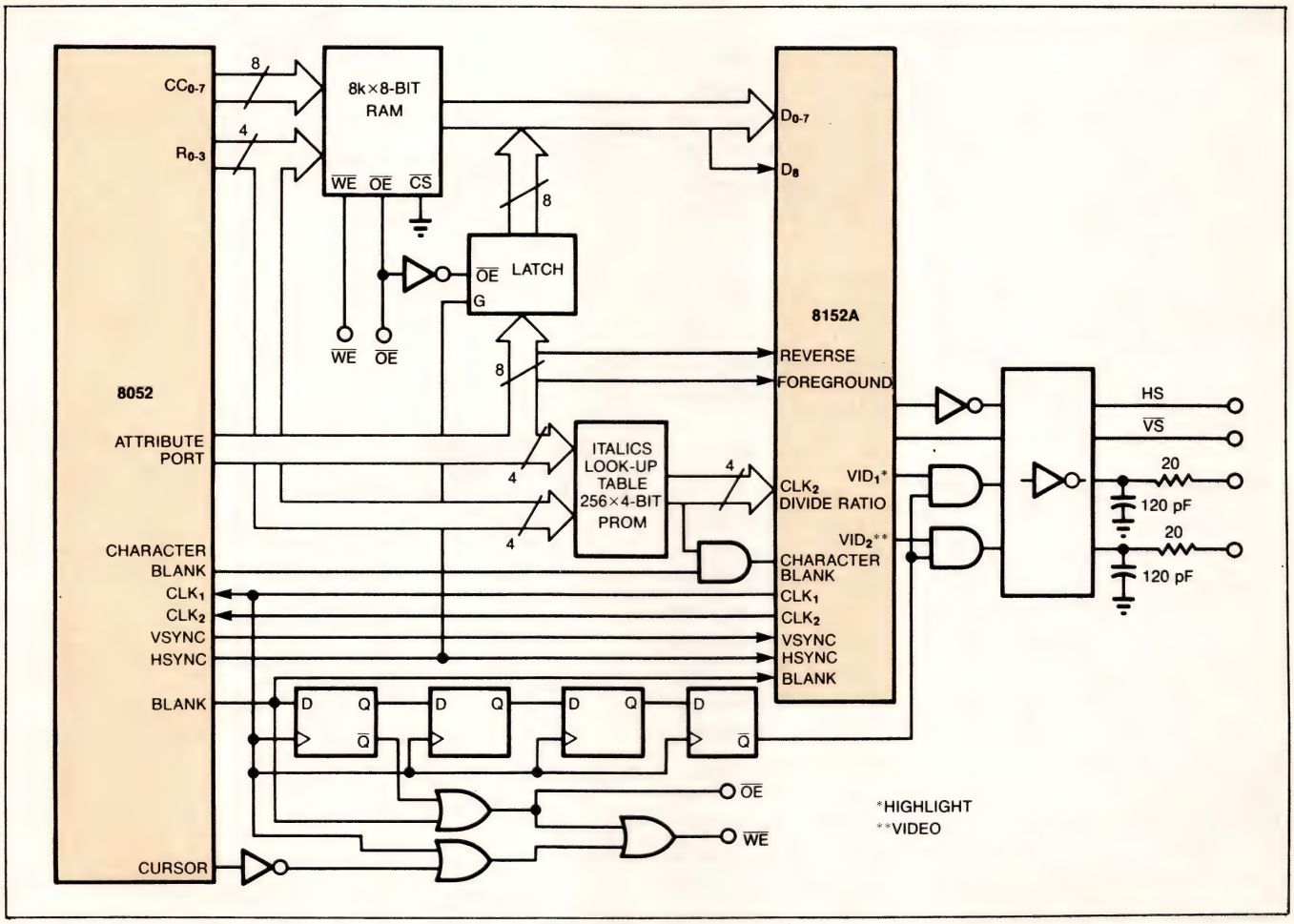


Fig 2—Normally, the 8152 connects directly to the 8052 *display controller. In this design, however, extra circuitry provides horizontal smooth scrolling, a programmable character font, and an italic-character generator.*

Many applications require a feature that allows the terminal user to dynamically change the number of characters displayed on the screen.

The character-font generator is a key element of any alphanumeric CRT display. It holds the bit-by-bit character layouts that the terminal uses to map ASCII characters onto a pixel pattern on the screen. Typically, a character font is a matrix of 8×8 or 8×16 pixels. Because they store either the 128 standard ASCII characters or 256 characters (the standard set plus an alternate font or the enhanced ASCII set with block graphic characters), the character-font generators vary in size from 1k byte (128 characters, each 8×8 pixels) to 8k bytes (512 characters, each 8×16 pixels).

In traditional terminal designs, the character-font generator has been a ROM, giving the terminal user access to one or two fixed character fonts. Today, users are demanding more flexibility, such as the ability to support special characters, foreign languages, or symbols.

RAM font permits special characters

Many designs now use a RAM-based generator to ease modification of the character font. The character-font RAM is usually a dual-port memory, with one port allocated to the display controller and the other port dedicated to the local μP. The RAM holds two complete 256-character fonts: one for the normal mode and one for the compressed mode.

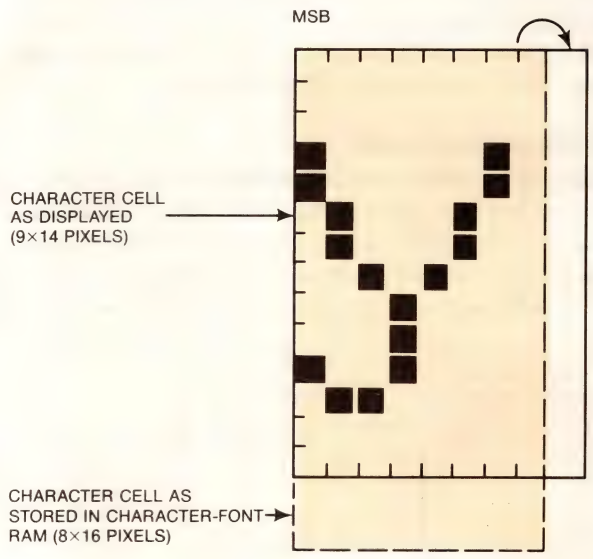
A dual-port memory generally requires an address multiplexer, data-bus transceivers, and a bus arbiter. The 8052 offers a simpler approach. The CRT controller itself loads the new character patterns into the character-font RAM, eliminating the need for a dual-port memory.

Attributes set character patterns

The key to this trick is the 8052's attribute port. Normally, the attribute port supplies character-by-character attribute specifications to the 8152 coincidentally with the 8052's supplying the row and column addresses to the character-font memory. In this design, however, the attribute for the first character of every line is actually a character pattern that is written into the character-font RAM. Note the $\overline{WE}$ and $\overline{OE}$ decoding circuitry in **Fig 2.**

This approach requires external logic to keep these character patterns, which are meaningful to the character RAM but not to the 8152, from being displayed. A digital delay line built of D flip-flops blanks the first character of each character row. An 8-bit latch serves as the data path from the attribute port of the CRT controller to the data bus of the character-font RAM.

Because the hardware externally blanks the first character of all rows, the 8052's output buffers can now contain any character code and attribute without affecting the display. Each of these spare character positions holds one byte—enough bits to alter one character slice



NOTE: N="Y"×16=790$_H$

ESCAPE SEQUENCE:
ESC [y 3, 130, 130, 68, 68, 40, 16, 16, 144, 96;

CHARACTER-FONT RAM ADDRESS	DATA BINARY	HEX	DEC
N+0	0 0 0 0 0 0 0 0$_B$	00$_H$	0$_D$
N+1	0 0 0 0 0 0 0 0$_B$	00$_H$	0$_D$
N+2	0 0 0 0 0 0 0 0$_B$	00$_H$	0$_D$
N+3	1 0 0 0 0 0 1 0$_B$	82$_H$	130$_D$
N+4	1 0 0 0 0 0 1 0$_B$	82$_H$	130$_D$
N+5	0 1 0 0 0 1 0 0$_B$	44$_H$	68$_D$
N+6	0 1 0 0 0 1 0 0$_B$	44$_H$	68$_D$
N+7	0 0 1 0 1 0 0 0$_B$	28$_H$	40$_D$
N+8	0 0 0 1 0 0 0 0$_B$	10$_H$	16$_D$
N+9	0 0 0 1 0 0 0 0$_B$	10$_H$	16$_D$
N+10	1 0 0 1 0 0 0 0$_B$	90$_H$	144$_D$
N+11	0 1 1 0 0 0 0 0$_B$	60$_H$	96$_D$
N+12	0 0 0 0 0 0 0 0$_B$	00$_H$	0$_D$
N+13	0 0 0 0 0 0 0 0$_B$	00$_H$	0$_D$
N+14	0 0 0 0 0 0 0 0$_B$	00$_H$	0$_D$
N+15	0 0 0 0 0 0 0 0$_B$	00$_H$	0$_D$

Fig 3—Programming a character cell involves *the host computer's sending to the terminal an escape sequence with the new bit pattern encoded into ASCII numbers. These numbers must be separated by commas.*

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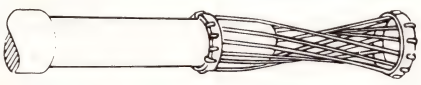

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of one character per character row (a character slice is a horizontal row of pixels within a character cell). With 24 character rows on the screen, you can modify 24 bytes per frame. With 12 visible slices per character, the 8052 can load up to two full character matrices into the character-font RAM per frame.

More than enough speed

A 60-Hz frame rate yields an update speed of about 120 cps. Although a 120-cps speed might not seem very fast, this rate is about six times faster than the rate at which the 8751's asynchronous communication port can receive new character fonts that are downloaded from the host. For example, at 9600 baud, the host transfers about 1000 bytes per second.

Defining a typical character cell requires approximately 50 bytes of command, control, position, and bit-pattern data, which results in a host update rate of about 20 cps. The first few character positions of the message string that the host sends to the terminal provide all the information required to initiate loading. The μP decodes the message string and supplies the 8052 with appropriate character codes and attributes to make the 8052 perform the loading process.

Subsequently, the character code from the 8052's row- and column-address port selects, in the manner described earlier, one particular character-font matrix in the character RAM. The position of the cursor attribute, which can be on any scan line of a given character, selects the scan line to be altered. The row-attribute word holds the new slice data, and finally an active cursor attribute enables loading.

If the cursor-attribute bit of the first character is set, simple combinatorial logic consisting of three OR gates enables the attribute-port latch, which stores the slice data and generates a write pulse to the character-font RAM to load in the new character slice. If the cursor attribute bit is not set, the logic masks off the write pulse. As a consequence, the character-font RAM is not updated.

Command loads font cell

The ANSI X3.64 standard, which defines control sequences of ASCII characters that the host computer must send to a terminal for special functions, such as "delete line," also allows for user-specific control functions. One of these user-specific control functions initiates font loading. The format for the command and data is fixed. Like all extended control sequences, this command starts with the Control Sequence Introducer

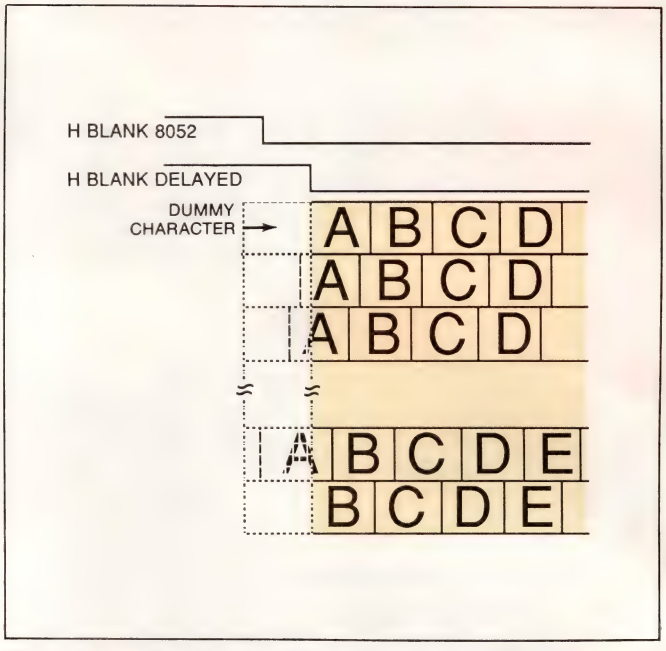

***Fig 4—You can scroll a given line of text** horizontally with the aid of a blanked, dummy character. You reduce the width of the dummy character one pixel column at a time until the left-most displayed character has almost disappeared. Then you restore the dummy character and delete the left-most character entirely.*

(CSI). According to the standard, the CSI can be the escape sequence "ESC [" or a single, 8-bit character code ($9B_{HEX}$).

Following the escape sequence, the first parameter in the control sequence is the ASCII code of the character-font cell that will be reloaded. The second parameter specifies at which character-cell slice the reloading should begin. The slices are numbered downward beginning with zero **(Fig 3).** The slices above the first loaded slice are automatically blanked.

Subsequent parameters each represent a slice of the new character cell. These parameters are decimally encoded byte values of the desired 8-bit slices. The most significant bit represents the left-most pixel of a character-cell slice. For example, consider the character slice 1001000, where "1" represents a white pixel (foreground color) and "0" represents a black pixel (background color). The corresponding decimal value is 144. The ASCII character sequence of "1," "4," and "4" (31_{HEX}, 34_{HEX}, 34_{HEX}) redefines the character slice. Following the standard, you must separate the code sequences of character slices by commas. **Fig 3** shows the pixel pattern and escape sequence for defining a character cell.

The 8052 directly supports vertical smooth scrolling

A RAM-based generator eases modification of the character font so that the terminal can display custom characters.

of split screens. The 8052 can scroll the background while windows stay stable, or it can scroll a window while the background stays stable. Horizontal smooth scrolling, or panning, takes advantage of the proportional-spacing feature of the 8152A but requires external hardware as well.

In this design, positioning a variable-width dummy character at the beginning of a row of characters allows the system to pan the entire character row. By varying the width of this dummy character, all subsequent characters in an entire row will move horizontally. In order to blank this dummy character, you must increase the size of the left margin, or "back porch," of the display. Delaying the falling edge of the signal from the 8052's Blank output (HBLANK) furnishes this delay. The 8052 cannot generate this timing delay; you must implement it in external hardware (shown in **Fig 2**) because the 8052 will always start strobing out character codes with the falling edge of HBLANK.

In this design, external circuitry delays HBLANK by three system clock (CLK1) cycles, which is equal to 12 pixels. The normal width of the dummy character, in the nonscrolling state, is also 12 pixels. To initiate scrolling, you gradually reduce the width of this dummy character to four pixels. In this final state, the added hardware now blanks the left-most eight columns of pixels of the first character, leaving only one pixel column visible. In the next step, this last pixel column will also scroll out. However, this state is identical to a nonscrolling state with the first visible character deleted. So you complete the horizontal scrolling of the character by restoring the full width of the dummy character (12 pixels) and by removing the first character from the character string **(Fig 4).** You can reverse this process to achieve panning to the right.

The vertical interrupt of the 8052 can control the horizontal-scroll rate (the same interrupt also controls the vertical-scroll rate). The 8052 interrupts the 8751 once per frame. The interrupt activates software that controls the panning process, and the software can move the pan forward one step after it counts a programmable number of interrupts.

The standard approach to producing italic characters is the same as that for producing any other nonstandard characters; the italic characters constitute a special font. If you wish to have both normal and italic characters available, however, this approach doubles the size of the character-font RAM. A less costly approach once again makes use of the chip set's proportional-spacing feature. Simply inserting a trapezoidally shaped blank, whose top is wider than its bottom, into the character stream tilts all subsequent characters **(Fig 5).** Inserting a blank that's the reverse of the trapezoidal shape cancels the italic mode.

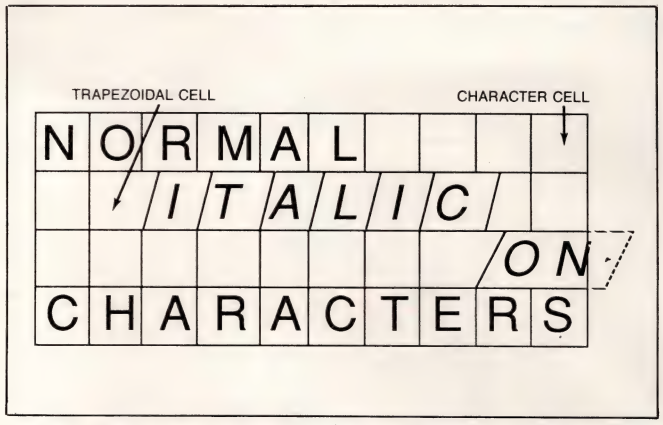

***Fig 5—Instead of doubling the size of the character font** to provide italic characters, you connect a PROM to the 8152A video interface to drive the chip's proportional-spacing divider, which produces a trapezoidal dummy character. The dummy character has the effect of tilting all subsequent characters into italic-style characters.*

External hardware helps to generate these trapezoidally shaped characters. The hardware is a 256×4-bit PROM that accepts outputs from the 8052's row-address and attribute ports as addresses. The output data from the PROM goes to the CLK_2DR input port of the 8152A. The CLK_2DR input programs a divider whose output feeds back to the 8052's CLK_2 input. The 8052's CLK_2 input times the fetches from the chip's character buffer; varying the CLK_2 rate has the effect of stretching or compressing one scan line of a given character. For normal characters, the PROM is transparent.

(Ed Note: Detailed schematics of a demo board for this terminal and the complete listing of the 8751 source code in assembly language are available. Please contact your local AMD office for further information.)

EDN

Author's biography

Juergen Stelbrink is a field application engineer for Advanced Micro Devices (Sunnyvale, CA). Juergen has worked in the US and is currently providing technical support in Bavaria, Austria, and Switzerland. He has an MS degree from RWTH Aachen in West Germany. In his spare time he enjoys photography, traveling, windsurfing, and skiing.

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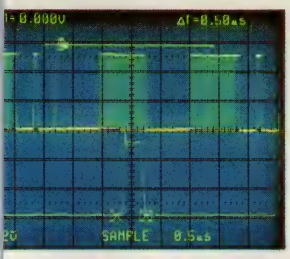

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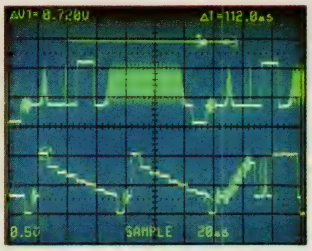

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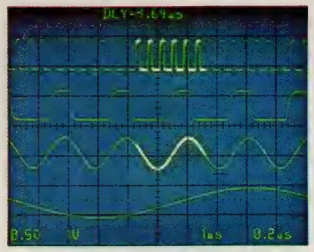

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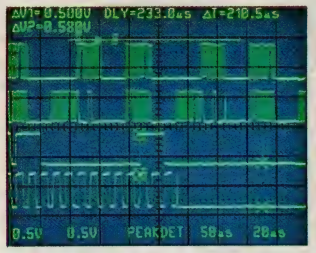

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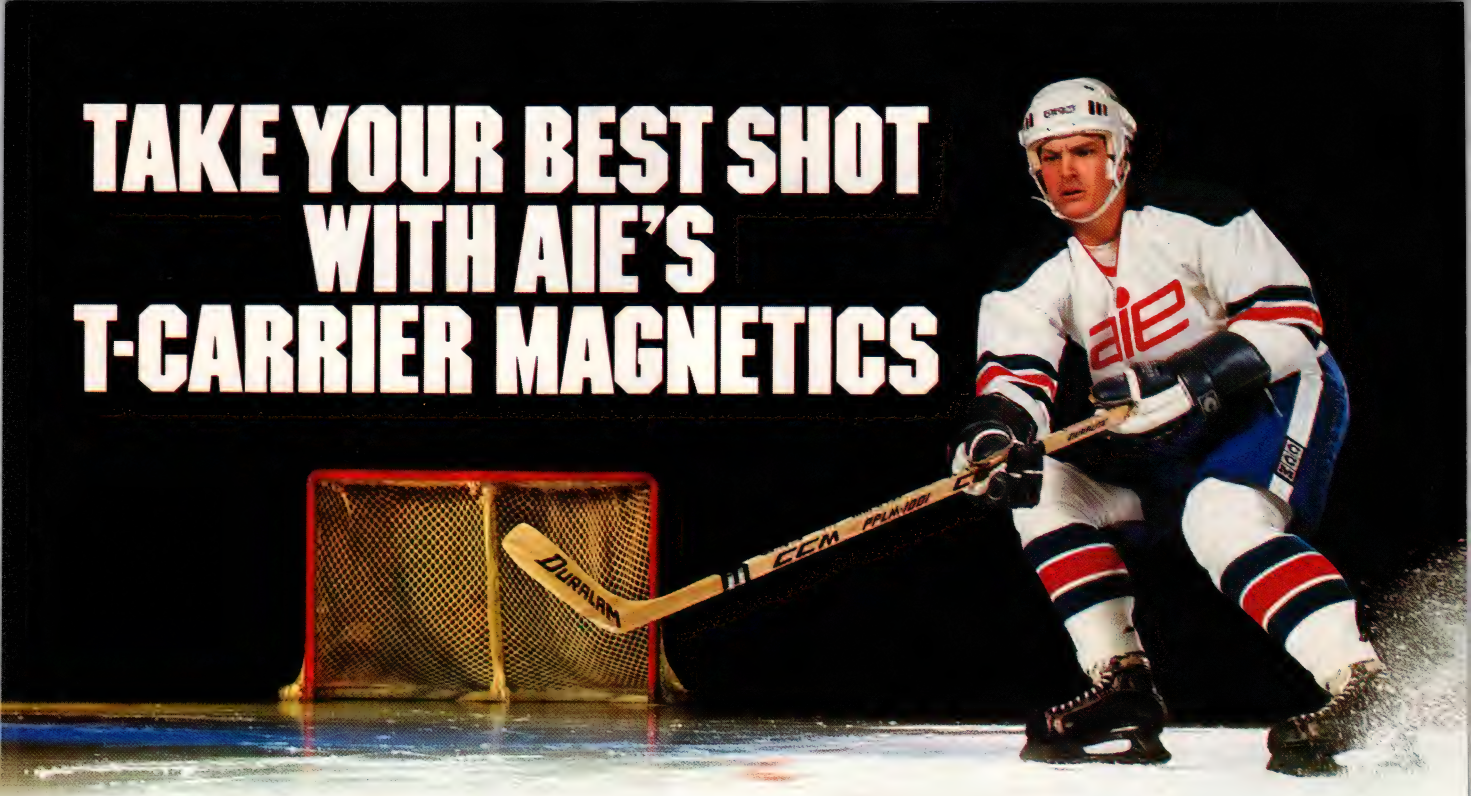

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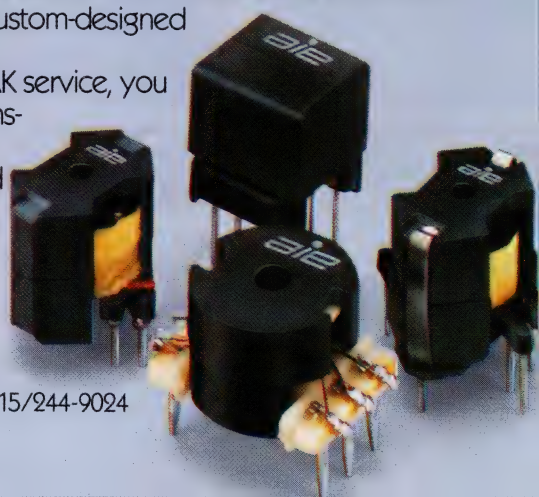

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CIRCLE NO 71

Consider how TTL outputs work during power-downs

When you use TTL circuits in systems that have backup batteries, you must go beyond a perfunctory "black-box" treatment of the devices. For systems that might suffer partial power losses, you must consider the behavior of the TTL ICs' output structure.

Mark A Taylor, *Hewlett-Packard Co*

Although most designers overlook the output structures of TTL circuits, the structure is of critical importance in applications where portions of a circuit remain powered up during a main-power loss—for example, in battery-backed-up memories or CMOS logic (for which you mustn't let the inputs float), or in designs that receive power from more than one source. TTL vendors' data sheets don't usually specify the gates' output impedance during power-down conditions, so it's important that you understand the output characteristics of the various TTL families. In order to gain such an understanding, you might have to spend a lot of time on the phone with a specific IC manufacturer's applications engineers, but the examples in the following pages will give you some insight into the general behavior of TTL output circuitry.

As a starting point, it's helpful to consider the basic TTL gate in **Fig 1.** Q_2 pulls the output high through R_3, and Q_3 pulls the output low. Q_1 is the phase-splitting transistor that alternately drives Q_2 or Q_3. An input signal can pull the base of Q_1 low to drive the output high. Pulling Q_1's base low turns Q_1 off. R_1 then pulls the base of Q_2 toward V_{CC}, thereby turning on Q_2.

Current flows from V_{CC} through the current-limiting resistor R_3 to the collector, and consequently the emitter, of Q_2. The current flows out of Q_2's emitter and through D_1 to the output; the output voltage thus goes high. To drive the output low, you must apply a voltage greater than approximately 1.4V to the base of Q_1. Q_1

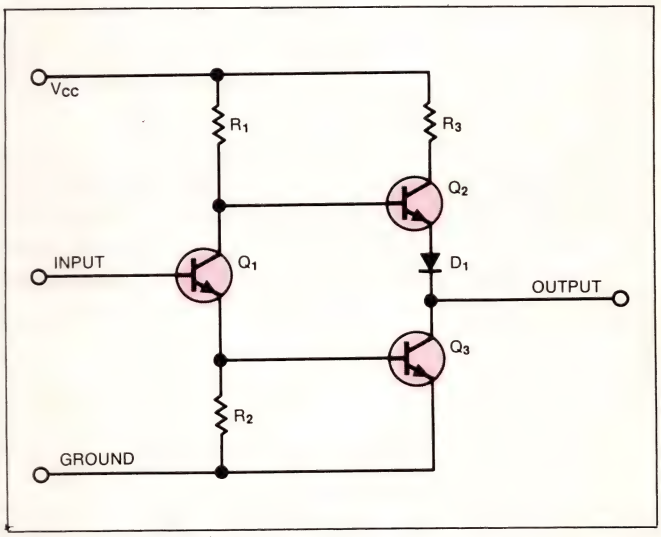

Fig 1—In this basic TTL gate, *no current path exists from the output to the positive supply, unless the output transistors break down. This condition doesn't prevail in later-generation TTL ICs.*

To drive the output low, you must apply a voltage greater than about 1.4V to the base of Q_1.

then draws current through R_1, thereby lowering Q_2's base voltage and turning Q_2 off.

The current drawn through R_1 goes to the base of Q_3 and to R_2. The base current turns Q_3 on to pull the output low. Diode D_1 keeps Q_2 turned off while Q_3 is turned on by inserting an extra diode drop between the output and the base of Q_2.

It's a common assumption among designers that when you remove V_{CC} from an IC, the output becomes an open circuit. This assumption is valid for the oldest TTL families (TTL, LTTL, HTTL). *The TTL Data Book*, Volume 2 **(Ref 1)**, shows that the ICs' output paths connect to the collector of the pull-down transistor and to the emitter of the pull-up transistor as shown in **Fig 1.** Therefore, no current path to V_{CC} exists upon power removal—unless the output transistors break down.

If you look through TTL-IC vendors' documentation, though, you can see that the story has changed as new families of parts have evolved. These newer TTL families can present a low-impedance path from the output to V_{CC} when the output level is higher than the voltage on the V_{CC} pin (that is, during power-down).

Although Schottky TTL parts don't appear to exhibit this low-impedance property, some LSTTL, Fast, advanced LSTTL, and advanced Schottky TTL devices do **(Fig 2).** Many of the small (single-gate) logic parts have a current path through a diode (D_2) to the pull-up

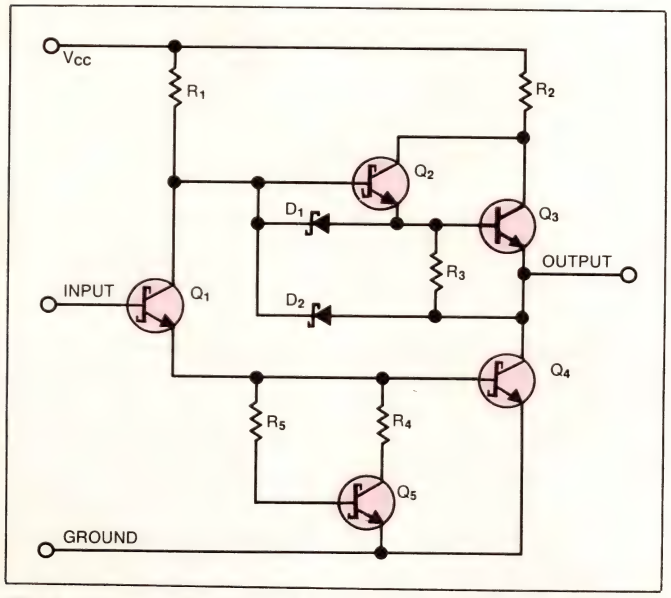

***Fig 2—A current path exists between the output and V_{CC}** in this typical TTL gate. D_2 and R_1 provide one such path; R_3, Q_2 (operating as a transistor in the inverted mode), and R_2 provide another.*

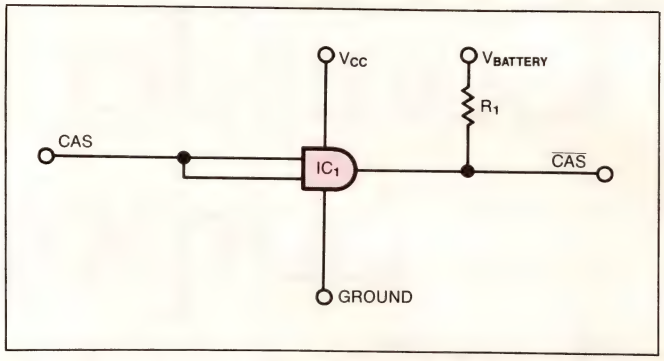

***Fig 3—Battery backup can create problems in memory systems** if you use a TTL gate whose output impedance is low when the IC's power supply goes down. If you use such a gate, the pull-up resistor to $V_{BATTERY}$ must be low enough to keep CAS unasserted when V_{CC} fails.*

resistor (R_1) for the phase-splitting transistor Q_1. The pull-up resistor thus provides a path from the output to V_{CC}. Further, once current is flowing in the phase splitter's pull-up resistor, the first transistor (Q_2) of the Q_2-Q_3 Darlington pair that pulls the output high can turn on backwards (that is, in the inverted mode).

This inverted-mode turn-on action typically provides a current path from the output through resistor R_3 to the backward-conducting Q_2, then on to the current-limiting (for low-to-high transitions) resistor R_2, and finally to V_{CC}. The behavior of D_2 and Q_2 can result in an equivalent load of 105Ω at 2V between the output and ground.

Low Z_{OUT} can pose problems

Fig 3 shows a sample circuit in which a low-impedance output might create a problem. Assume IC_1 is a CAS driver for a dynamic-RAM array that uses RAS-only cycles for its refresh operation. $V_{BATTERY}$'s role is to supply the dynamic RAMs and to keep CAS unasserted during the period when the battery-backup is in use. If the output of IC_1 exhibits a 100Ω output impedance when V_{CC} is low, then R_1 has to have a value lower than 100Ω in order to pull $\overline{CAS}$ up reliably. A pull-up resistor with such a low value is clearly unacceptable.

The test circuit shown in **Fig 4** provides a means to verify the behavior of the output structure in typical TTL ICs. A 10Ω resistor connected between the IC's V_{CC} and ground pins mimics the output impedance of a power supply that's turned off. The test involves applying a voltage between the output under test and ground.

For this case history, three vendors' TTL-family ICs were used: vendor A's 74S32 and 74F32, vendor B's

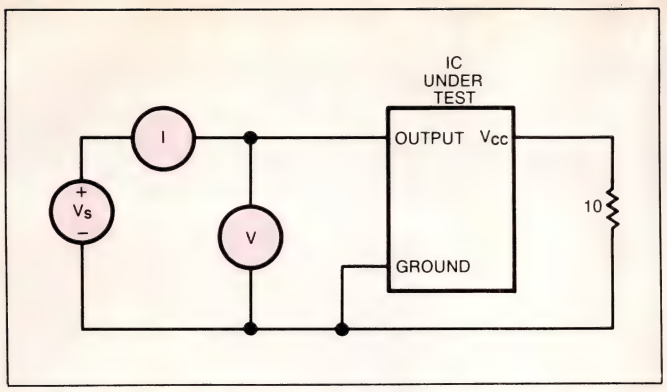

Fig 4—You can test a TTL device for power-down output impedance *by using this circuit. The 10Ω resistor simulates the output impedance of the turned-off power supply.*

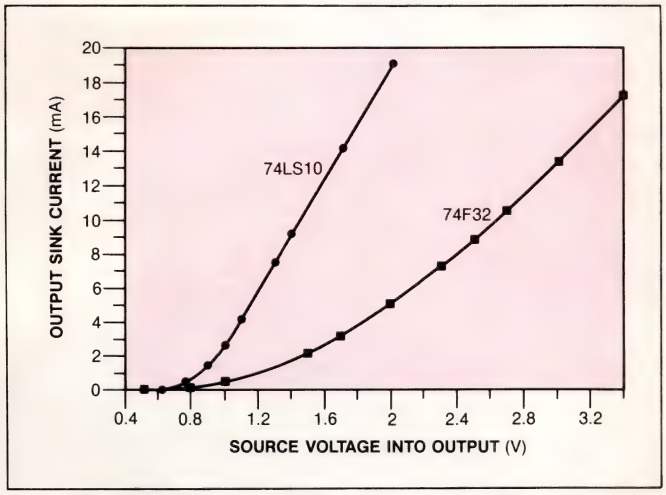

Fig 5—An unpowered TTL gate can draw significant current at its output, *as these curves for two typical TTL devices illustrate. The 74LS10 draws current as high as 20 mA when external circuitry applies voltages as low as 2V at the gate's output.*

74LS32 and 74LS10, and vendor C's 74LS10. Only vendor A's 74F32 and vendor C's 74LS10 exhibited low output impedance when V_{CC} was powered down. **Fig 5**'s graph shows the 74F32 and 74LS10's current vs applied voltage. If you were to examine the data books from vendors A and C, you'd be able to predict that current would flow.

The test results for vendor B's ICs were surprising. Neither of these LSTTL parts drew significant current until the output voltage exceeded 6V. There isn't any documentation in Vendor B's data book regarding the ICs' output structure, so it's difficult to tell how the manufacturer blocked the current.

Ascertain Z_{OUT} before purchasing

This test proves that different TTL families as well as different vendors' parts exhibit different output characteristics upon the removal of power from V_{CC}. One of the vendors in the test corroborated that different parts exhibit different output characteristics upon the removal of power from V_{CC}, and that these disparities apply to various parts within a TTL family. In particular, the vendor mentioned that bus-driver parts typically tend toward high impedance when V_{CC} loses power.

You won't find specifications for the required characteristics in data books, and so you should check with a vendor's applications engineers before you design a part into an application in which the IC's output must be predictable when V_{CC}'s power source goes down. If, a TTL manufacturer's technical support notwithstanding, the part you've chosen doesn't exhibit high output impedance when powered down, try another TTL family or another vendor. Once you find the correct part, specify the required output characteristic in the purchase contract.

If you have difficulty obtaining a commitment from a vendor, other options may sometimes be feasible. For example, when the rise time (which is affected by capacitive loading) isn't critical, you can use a gate having an open-collector output. Providing backup power to the offending TTL device can help if the extra power doesn't present a problem, but you must consider the part's inputs (which might come from other, unpowered circuits). Finally, the new HCTs (high-performance CMOS transistors) offer a solution, if your circuit is compatible with their operating parameters. **EDN**

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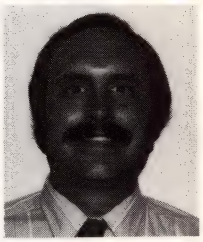
Author's biography



Mark A Taylor is a hardware-development engineer at Hewlett-Packard's Data Systems Div (Cupertino, CA). A 5-year employee at HP, he previously worked at Netcom Products Inc. Mark holds a Bachelor of Science degree in electrical engineering and computer science from the University of California at Berkeley and is a member of Tau Beta Pi and the IEEE. His spare-time pursuits include camping, bicycling, sailing, and off-road motorcycling.

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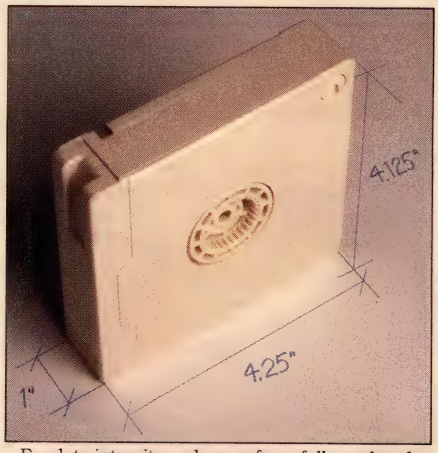

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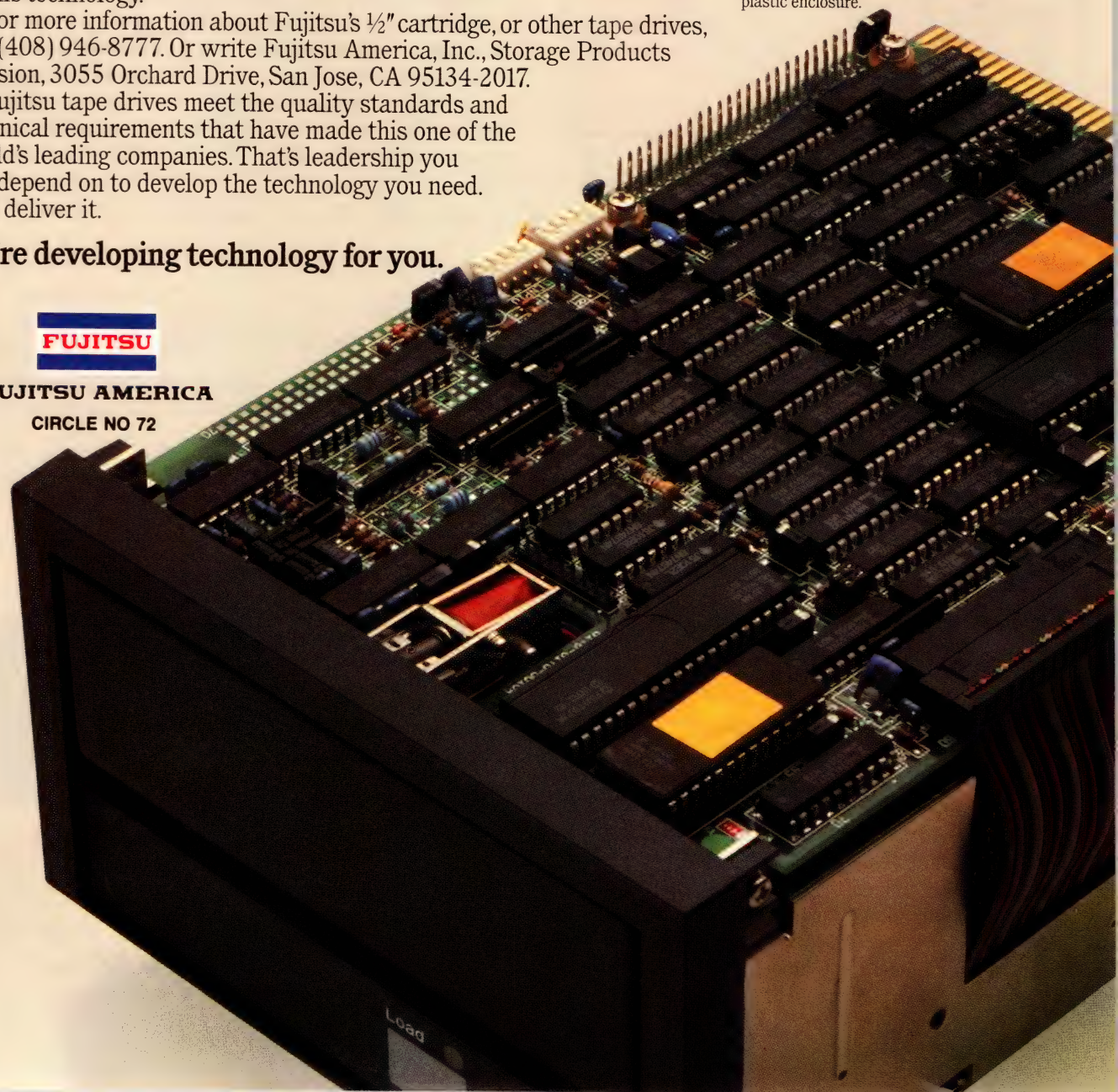

Power planes increase wire-wrapped circuit speeds

By adding power and ground planes to a wire-wrapped board, you can decrease signal rise and fall times. This technique also minimizes system noise, ringing, and propagation delays. By using a 4-layer board, you can build a prototype of a circuit that contains Schottky TTL devices.

P Anthony Visco, *Mupac Corp*

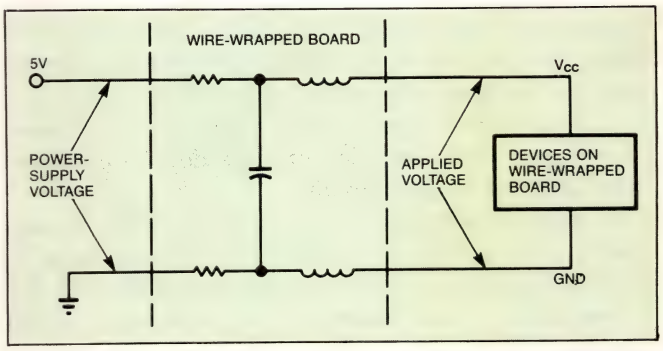

Fig 1—The resistance, capacitance, and inductance *of a wire-wrapped board decrease the potential difference that a power source can supply to the devices on the board.*

Using a multilayer wire-wrapped board improves the limiting characteristics of a 2-sided board and provides you with a more efficient power-distribution grid upon which to model a Schottky TTL circuit. On a standard 2-sided wire-wrapped board, the wires that connect a power supply to the devices' power and ground pins introduce a parasitic impedance. This impedance pushes the circuit's operating frequencies below the 30- to 50-MHz requirement of most Schottky TTL designs. The conducting layers in a multilayer wire-wrapped board, on the other hand, supply power and ground directly to the ICs, thereby reducing the impedance caused by the board.

Further, the conducting power-supply layers in multilayer wire-wrapped boards decrease the rise and fall times of signals, and they minimize system noise, ringing, and propagation delays.

To design a high-speed circuit, you must first calculate the rise and fall times and signal-to-noise ratios of your devices. You must also consider external factors such as the access time to peripherals and the time required to perform other operations. These external factors often limit a system's clock rate. Further, note the rise times: In asynchronous designs (or synchronous designs that include internal asynchronous sections), rise times—not clock rate—control the overall system speed.

Because no electronic device has zero impedance, every pulse has a finite rise time. The impedance in a wire-wrapped board's power-distribution system causes a transient voltage drop between the power supply and the devices on the board. **Fig 1** shows a wire-wrapped board's power-distribution system. In this circuit, V_{CC} is less than 5V and GND is greater than zero. Therefore, the potential difference (V_{CC}−GND) applied to the devices on the board, at high

Conducting layers on a wire-wrapped board decrease signal rise and fall times, system noise, ringing, and propagation delays.

frequencies, is smaller than the power supply's potential difference. Moreover, the magnitude of this voltage drop and its relative effect on the circuit depend on the amplitude of the current.

If your input current is in the microamp range and your gates provide high impedances, the high-frequency voltage drop will be an insignificant fraction of the step voltage. However, when a device must supply an output current of many milliamps—and when there are many devices that may turn on simultaneously—you can't ignore the effect of the voltage drop. For example, when you try to apply a square wave to your circuit, you get a spread-out pulse instead.

In a 2-sided board, high impedance at high frequencies causes a significant voltage drop. Because the board attenuates the high-frequency components of the voltage, the applied voltage and the signal-to-noise ratio decrease while the rise time increases. The resistance of the copper fingers (the conducting paths of the power and ground) on a 2-sided board prevents devices that are far from the power source from reacting as quickly as devices that are close to the source of power. The delay in the switching of some devices can cause false behavior in your circuit.

To take advantage of your Schottky TTL devices' speed, your prototype (or production) board must be able to distribute power to many devices in a few nanoseconds. When analyzing the power-distribution system of your wire-wrapped board, you must account for ac transient effects in both the applied voltage and the current. Your wire-wrapped board must deliver as ideal a response as possible, so that your ICs, not your board, limit the speed of your circuit.

To minimize the effect the wire-wrapped board has on your circuit, you must minimize the impedance caused by the board. Impedance is a complex quantity that you can break into resistive, capacitive, and inductive parts. You can describe the resistive, capacitive, and inductive parts of the complex impedance as

$$Z_R = R,\ Z_C = \frac{1}{j\omega C},\ Z_L = j\omega L, \qquad (1)$$

where R, C, and L are resistance, capacitance, and inductance, respectively; Z_R, Z_C, and Z_L are the respective resistive, capacitive, and inductive parts of the impedance; and ω is the operating frequency.

As **Fig 1** shows, the wire-wrapped board adds resistance and inductance in series with the rest of the devices in a circuit; the capacitance caused by the wire-wrapped board is in parallel with the rest of the circuit. By adding the series and parallel parts of the impedance, you can express the total impedance due to the wire-wrapped board, Z, as

$$Z = \frac{1}{j\omega C + \dfrac{1}{R + j\omega L}}. \qquad (2)$$

Eq 2 shows that, to minimize impedance, and thereby exploit the fast rise time of your Schottky TTL chips, you should keep your board's resistance and inductance as small as possible, and its capacitance as large as possible.

The 4-layer wire-wrapped board in **Fig 2** solves the wire-wrapped-board impedance problem; this structure has a smaller resistance and inductance and a larger capacitance than does a 2-sided board. The design has four interleaved V_{CC} and GND planes, each layer having 2-oz/ft^2 copper layers. The 2-oz/ft^2 spec of the copper layers is the industry standard. On each of the four layers, the copper is in a lattice structure.

The copper lattice doesn't touch any of the wire-wrapped-pin holes in **Fig 2;** a fiberglass dielectric surrounds each of these holes. Because the copper lattice runs between every hole and its surrounding holes, this design maximizes both the conductivity of each plane and the number of current paths on each layer. To avoid internal ground loops and ensure that the two common planes conduct as one, plated-through holes connect the two sets of power planes to each other. The plated-through holes are distributed throughout the board. These holes also bring power and ground to both sides of the board.

By using the plated-through holes to tie the planes together, you obtain a virtually infinite number of

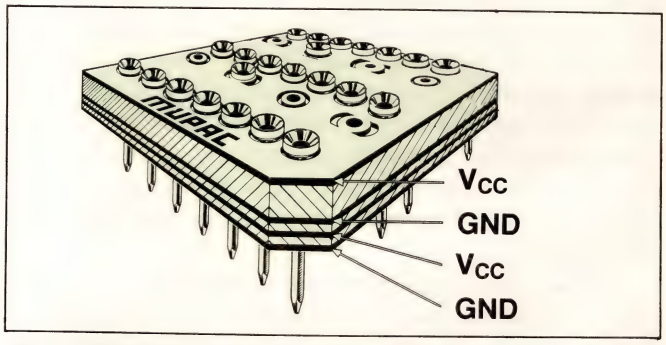

Fig 2—Plated-through holes interconnect *the V_{CC} pairs and the GND pairs on this 4-layer wire-wrapped board; a dielectric separates the wire-wrapped-pin holes from the power planes.*

current paths, thereby minimizing the voltage drop across the board. Instead of flowing through a wire or a copper finger to the devices on a board, the current on the multilayer board spreads out in all the power planes. Because the current can spread throughout the board, it can find the best multiple-path distribution for each turn-on condition.

This 3-D power-distribution design provides an extra benefit: It supplements the power supply's output capacitor with a local capacitance that supplies current to the devices on the board. The proximity of the power and ground planes, as shown in **Fig 2,** creates this built-in capacitor.

You can use this built-in capacitor as a decoupling capacitor; it supplies additional current to the Schottky TTL devices during turn-on and turn-off operations; this extra current decreases noise in the circuit. Because this capacitor discharges in less than a nanosecond, it doesn't affect signals to the circuit.

To increase the capacitance further, you can add decoupling capacitors to your circuit. Because V_{CC} and GND interconnections are available everywhere on the wire-wrapped board, the board has plenty of space for extra decoupling capacitors.

The greater the number of chips on a board, the larger the board's area must be, and the larger the area, the higher the capacitance between V_{CC} and GND. A larger board, therefore, can supply current to a greater number of devices. Furthermore, as **Eq 2** shows, increasing the capacitance decreases the impedance.

To minimize the resistance and maximize the capacitance, you must cover as much of the V_{CC} and GND planes with copper as possible. You must, however, keep copper away from the holes for the wire-wrapped pins. The annular clearance around the wire-wrapped pins in **Fig 2** is about 7.5 mil.

Besides improving the resistive and capacitive components of the impedance, a multilayer wire-wrapped board also reduces the inductive component by eliminating the need for wire-wrapping the V_{CC} and GND pins. Instead of wrapping a wire, you can connect the V_{CC} and GND pins of your IC directly to pins that connect directly to the V_{CC} and GND planes of your wire-wrapped board. This decrease in inductance is possible only for a multilayer board that has its V_{CC} and GND planes on external surfaces.

To connect a V_{CC} pin to the power plane, you place a solder-plated copper washer over the pin, as **Fig 3** shows. You heat the solder so that it runs onto the V_{CC} plane. The soldered washer shorts any V_{CC} or GND pin required by the IC to the V_{CC} or GND plane. The solder-plated copper washers reduce inductance because they eliminate the wrapped wire around the V_{CC} or GND pin.

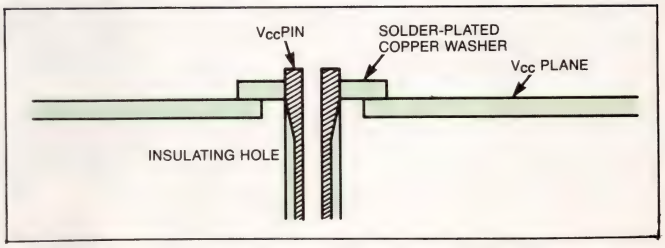

Fig 3—By using a solder-plated copper washer *to connect a V_{CC} pin to the V_{CC} plane, you can decrease your system's inductance.*

Taking measurements is, of course, the only way to evaluate the improvement a multilayer design provides in resistance, inductance, and capacitance. For a typical 2-sided board, the resistance between the two farthest points is 0.008Ω, the capacitance is 0.003 μF, and the inductance is 1.1 μH. For a 4-layer wire-wrapped board of the same dimensions, the resistance is 0.004Ω, the capacitance is 0.021 μF, and the inductance is 1.0 μH.

You can get even better specs by using solder washers. For a 4-layer board with solder washers, the resistance and inductance between any field pin and any plane is infinite; the capacitance is 6 pF. You can use this type of board for circuits that operate at frequencies as high as 100 MHz.

As on wire-wrapped boards, conducting layers minimize impedance on pc boards. Once you've verified a multilayer wire-wrapped breadboard of your design, you'll either use a multilayer pc board for your final product, or you'll fabricate a multilayer pc board. **EDN**

Author's biography

P Anthony Visco, marketing services manager for Mupac Corp (Brockton, MA), directs all the company's marketing communications activities. Tony, who has been with the company for three years, attended the New England School of Art and Design in Boston, MA. In his leisure time, he enjoys sport fishing, photography, painting, and music.

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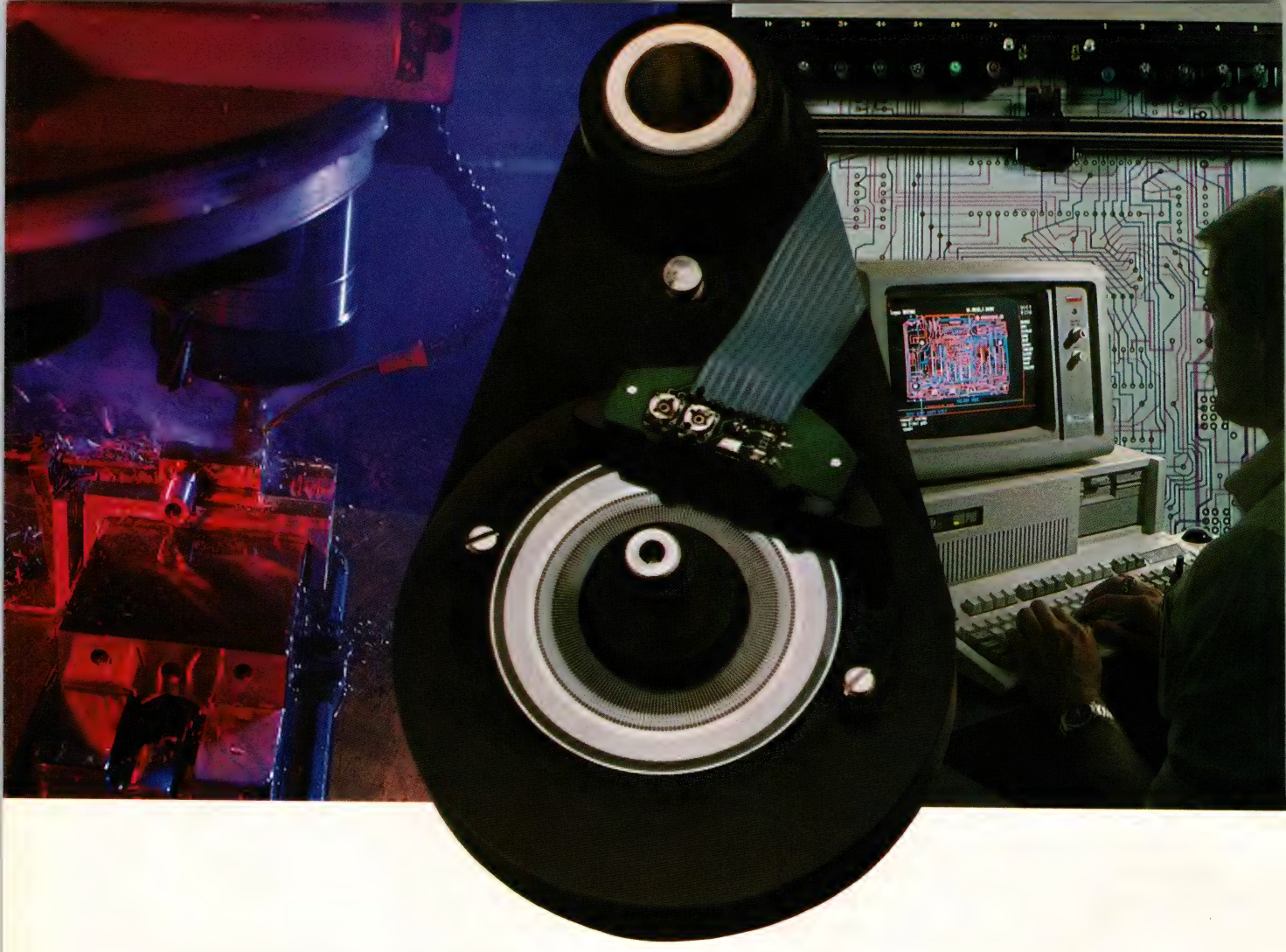

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Check lists help you avoid trouble with MOS and memory ICs

Before surrendering your CMOS and memory designs to production, you can make sure that they will work by asking yourself the right questions. By paying attention to potential problem areas, you can bypass the troubles associated with CMOS-, MOS-, RAM-, and ROM-device design.

Nathan O Sokal, *Design Automation Inc*

In the design realm, what you don't know might ultimately hurt the viability of your design. If you don't follow certain precautions, and if you don't safeguard potentially hazardous elements of your design, your CMOS, MOS, and memory designs might require costly corrective measures later on—after the manufacturing process has begun. The following two check lists offer guidance for avoiding potential complications. One check list is concerned with CMOS circuits; the other is concerned with MOS, RAM, and ROM devices. Part 1 of this series (**Ref 1**) presented a check list for designs that use TTL devices. Although much of that advice can apply also to CMOS, MOS, RAM, and ROM devices, MOS and memory circuits do pose special problems for the uninformed or unwary designer.

CMOS devices

1. Have you taken adequate precautions to avoid static-electricity damage? High static charges can occur and destroy CMOS input circuits while you're handling an IC or inserting a pc board into its socket.

2. Have you protected signal inputs and outputs against overvoltage spikes? If such spikes are greater than the supply voltage or less than ground, parasitic pnp or npn transistors can become forward-biased and can cause the device to latch up. A 3-state device's output in the high-impedance state is more sensitive than an output in the high or low state. The danger level depends on the specific CMOS technology used by a specific vendor.

3. Have you kept the output load within the device's capability? Heavy loads, such as those imposed by large capacitors or direct connection to common-emitter pnp or npn transistors, can damage CMOS ICs.

4. Is the supply voltage close to the maximum for which the device is rated? If so, keep in mind that the internal circuit arrangements of some MSI/LSI chips can boost internal voltages to values above the critical levels.

5. Are you using analog switches? If so, be sure to incorporate protective circuitry to limit the current

Heavy loads imposed by direct connection to grounded-emitter pnp or npn transistors can damage CMOS ICs.

flowing through them. Excessive current through analog switches results in latching and destructive breakdown.

6. Have you ensured that high signals cannot be applied to any input until the power supplies reach their full voltage levels? If V_{DD} has not yet reached its full value, applying a high signal could forward-bias the diode internally connected between the input terminal and V_{DD}, and thereby damage the input circuitry.

7. Are the rise and fall times of any input signals greater than 15 μsec? If so, the device may dissipate more power than its rated maximum. Be especially vigilant if you're using high-current drivers with high supply voltages.

8. Have you terminated all inputs? A floating input turns a CMOS device on and may cause faulty operation and damage.

9. Have you used CMOS gates as linear amplifiers or as building blocks for monostable circuits? Doing so may destroy buffer gates; moreover, the circuit may not operate with supplies of less than 4V. Even if you get the circuit to work, substituting similar parts from another vendor probably won't be feasible.

10. Have you used single-stage (unbuffered), multiple-input CMOS devices? Some logic conditions can cause both the static and the dynamic performance of these devices to deteriorate to the point that the system becomes pattern-sensitive. Be sure to design and run diagnostic tests that will reveal any such problems.

11. Is the operating frequency greater than 500 kHz? If so, be aware that the power consumption of a CMOS gate becomes greater than that of a low-power Schottky device at some frequency between 500 kHz and 2 MHz, depending on the CMOS supply voltage. At high frequencies, low-power Schottky devices are generally a better choice than CMOS devices.

12. Are you using CMOS one-shots? If so, note that you can't reset most vendors' one-shots; that is, applying a reset signal terminates the current timing cycle, but the device can't immediately start a new timing cycle. The recovery time varies according to the device type and the vendor.

13. Have you met the hold-time requirements of CMOS flip-flops, registers, and latches? Inputs to CMOS devices *must* remain stable for a specified period after the active edge of the clock pulse. CMOS systems are particularly prone to clock-skew problems, even at low clock frequencies.

14. Do any of the input signals have slow rise and fall times? Such signals can cause multiple triggering of some CMOS devices and may even lead to damage.

15. Have you used any wired-OR nodes? If so, the associated devices must have single-ended (open-drain) output circuits. Suitable devices are National Semiconductor's MM74C907 (p-channel only) and MM74C906 (n-channel only). You can't directly interconnect the outputs of devices with complementary-pair output circuits because such devices actively drive their output terminals to each logic state (one or zero). A direct connection between two or more such outputs can, in effect, short-circuit and damage the devices.

16. Have you verified that interfaces between CMOS devices and devices of other logic families satisfy all requirements? Interfacing requires a careful choosing of a vendor; few of the CMOS families have loading and threshold specifications that are detailed enough to ensure correct interfacing to bipolar devices.

17. Are you using CMOS flip-flops with transmission-gate inputs? These devices are particularly prone to malfunction if their inputs are driven above or below the supply voltages, which can occur when interfacing to other logic families or to distant boards.

18. Have you used the "typical" value specifications as the basis for your calculations? Because of the large part-to-part process variations, you can't assume that the parts you receive will be typical. Guaranteed values of propagation delay and supply current are often much larger than typical values.

19. Have you considered noise-energy levels? With a 5V supply, the noise margin of CMOS devices (approximately 0.4 nJ) is an order of magnitude smaller than that of TTL devices (approximately 4 nJ).

20. Have you carefully evaluated power-supply wir-

ing and bypassing considerations? To do so, refer to the first part of this article (EDN, November 13, 1986, pg 253) and ask yourself questions 46 through 49, substituting V_{DD} for V_{CC}.

21. Does the part listing properly identify the vendor of your CMOS devices? Parts with similar designations but manufactured by different vendors are often incompatible—for example, RCA's CD4028A and Motorola's MC14028 1-of-10 decoders.

22. Have you used devices of different technologies? The input and output voltages of HCT CMOS devices are identical to those of LSTTL devices. For this reason you can interconnect HCT and LSTTL devices with complete compatibility and very few problems.

MOS, RAM, and ROM devices

1. Are you operating memory chips at or near their maximum supply voltage or close to their maximum speed? In a large memory system—particularly one that uses dynamic memory—noise, loading, and skew problems reduce the apparent working area and the system speed.

2. Have you mixed different technologies in the same memory system? If so, you should take great care to ensure that no pin of a memory component is ever pulled below the substrate voltage (using diode clamps, if necessary). Such action usually activates parasitic substrate transistors and destroys data. For example, do not OR-tie the output of an n-channel RAM chip to that of a p-channel ROM: The ROM might pull the outputs below ground level and activate the parasitic transistor in the RAM, destroying data there.

3. Have you replaced wired logic gates with ROMs or PROMs? ROM or PROM chips aren't guaranteed to give a single output transition in response to a single input transition; the outputs are undefined until a time equivalent to the memory's access time has elapsed. During this interval, the memory's output lines may exhibit noise or extra transitions. Some memories (for example, those from Harris Semiconductor) avoid this problem by latching the inputs internally.

4. Have you used common bus lines? If so, do not allow more than one of the devices connected to the bus to be enabled at one time. Enabling more than one device simultaneously is unlikely to result in any physical damage but could produce severe noise problems.

5. Have you applied asynchronous input signals to a ROM? If you have, hold the asynchronous inputs stable for a period equal to or greater than the access time before you clock the output register. If the system doesn't meet this requirement, the contents of the output register may be completely unpredictable.

6. Do shift-register drivers have sufficient damping capability? All dynamic 2-phase shift registers exhibit some clock-to-clock coupling capacitance; drivers that have insufficient damping (that is, that have too high an impedance in the high state) may allow positive or negative spikes to leak from one clock line to the clock line of the opposite phase. Spikes that exceed the substrate voltage activate parasitic substrate transistors and destroy data.

7. Have you taken into consideration the input-to-output coupling characteristic of static RAMs? During a write cycle, the input data appears on the output lines, although the vendor's data sheets may not explicitly state this fact.

8. Have you provided adequate cooling? The power dissipation of memory chips is usually significantly greater than for most other MSI or LSI components. The power dissipation per unit area of circuit board can approach a level that's an order of magnitude greater than that of TTL.

9. Have you thoroughly evaluated the interfacing characteristics of the memory and its drivers? The voltage tolerance and noise immunity of MOS and CMOS memories are often very different from those of available drivers. Attempts by vendors to design MOS input circuits that match the available TTL or high-level driver voltages often result in large dc- or capacitive-loading effects.

10. Does your purchase specification for RAM include realistic and complete memory-pattern tests? It's very difficult to test memory components completely to ensure freedom from cell linkages and decoder errors; simple test sequences in which the number of tests is proportional to the number of bits (n-type tests) are totally ineffective unless specifically directed at known weaknesses of the component. Initially, you should

You can damage input circuitry by applying signals before V_{DD} has reached its full value.

subject parts to a full range of n^2 tests.

11. Have you carefully and regularly checked the programming specifications of the PROM devices you're using? Vendors often change the recommended programming method in order to improve programming yields. And typically, programming machines periodically require recalibration. Programming yields of less than 85% indicate that you should give immediate attention to the programming technique, to the calibration of the programming machine, or to both.

12. Have you used floating-gate MOS PROMs? These devices exhibit bit loss during exposure to x-rays and nuclear radiation. You may also have problems with inadequate erasure if your ultraviolet light source for erasure is improperly calibrated. You should monitor the actual voltage from each output at each address, during initial erasure and after each subsequent programming and erasure required by your testing program.

13. Have you used MNOS (metal nitride oxide semiconductor) electrically alterable PROMs? MNOS devices lose data from cells that have been accessed a large number of times (usually more than 10^9 times). This number is not as large as it seems; given an access time of 1 μsec, the device could lose data in less than one hour if the system performs continuous read operations from one memory location.

14. Have you used nichrome-fused bipolar PROMs? If so, make sure to test them thoroughly. It's not impossible for fuses to grow back after being blown during programming, and for unblown fuses to decay. No conclusive data is available, but the general opinion is that these defects are the result of programming-current slew rates that are larger or smaller than those recommended by the manufacturer. To avoid fuse failure, some users demand special freeze-out tests and high-voltage stressing tests, which are effective in revealing defective devices but greatly lengthen production lead times.

15. Have you used dynamic MOS shift registers to save power at low speeds? If the shift-clock speed is suddenly reduced for any reason, the shift register will lose data. The lower frequency limit given in the specification applies only to *ambient* temperatures, not to the higher junction temperatures produced by self-heating at high clock frequencies.

16. Have you included error-detection and -correction facilities? You can do so either by incorporating them into your system design or by selecting RAM ICs that have them built in. Error-detection and -correction facilities can improve the effective system reliability by two orders of magnitude, and the associated error indicators simplify both preventive and corrective maintenance.

17. Have you checked the access-time measurement criteria? Some vendors define access time as the time required for the output to reach the full V_{OL} and V_{OH} levels; other vendors define it as the time for both high and low outputs to reach 1.5V. Also, some vendors specify dc characteristics with two loads, but measure access time with only one load.

18. Do you completely understand the access-time specification? Some RAM specifications show a maximum access time; others show a minimum access time. Both describe worst-case conditions, but the maximum time is a characteristic of the component, and the minimum is the observed result of a test.

19. Do the vendor's access-time specifications indicate realistic memory operation? Vendors occasionally measure access time from the address-presentation edge alone, or from the chip-enable edge alone, regardless of the order in which you must apply these signals to the chip for proper operation.

20. Does your bipolar memory have pnp transistor inputs similar to those of low-power Schottky logic? If the system pulls such inputs far enough below ground level to saturate the pnp transistors, you'll encounter very long access times. Many ROM and PROM devices (including devices from Texas Instruments, Intel, and AMD) do have inputs of this type, and you should make sure that their inputs cannot swing below ground.

21. Does your ROM/PROM memory design allow for wide variations in access time over different parts of the arrray? Vendors specify only worst-case access times, but during ping-pong n^2 tests you can observe a range as great as 4:1 in the access times at various memory locations.

22. Have you considered operating-temperature

Power consumption of CMOS devices exceeds that of comparable LSTTL devices somewhere between 0.5 and 2 MHz.

ranges? Because memory components are so complex, they seem to be more sensitive to extremes of temperature than are other devices. Only a few vendors specify an operating-temperature range of 0 to 70°C, and some guarantee their memories over that range only if there is a transverse air flow that exceeds 400 linear feet/minute (for example, the Fairchild 93415).

23. Does your dynamic MOS RAM permit both burst- and distributed-refresh operations? Although designers commonly assume that all dynamic RAMs can be refreshed equally well in both modes, some RAMs that have unclamped bit lines don't respond to burst-refresh operations at high temperatures. At 70°C, these RAMs may not meet the 2-msec specification.

24. Have you evaluated the power-supply slew characteristic for the RAMs you're using? You might observe two separate problems in connection with the slew rate. First, at turn-on, slowly rising power-supply voltages may not initialize the RAM correctly, in which case you'll need to institute a separate initializing procedure. Second, the small, sharp changes that occur during normal operation of a memory system may cause data loss in some vendors' dynamic-memory products.

25. Have you taken precautions against transmission-line problems? Locate driver elements as close as possible to their associated memory components, so as to minimize transmission-line problems in the pc traces between them.

26. Have you used a multilayer board for an MOS memory? Multilayer boards greatly reduce noise problems and improve component density, but the capacitance between wiring and ground can be large. For example, a common-bus output line 20 cm long can have a capacitance of 150 pF. This capacitance, in conjunction with the limited drive current (2 to 4 mA) of most MOS memories, will increase rise and fall times to 200 nsec.

27. Have you taken adequate precautions against noise on the power-supply buses? Dynamic MOS memories exhibit small standby currents (approximately 4 mA) and large transient currents (approximately 120 mA) of short duration. For each supply bus, place a solid-tantalum bypass capacitor of 10 to 300 μF at the point where the supply enters the circuit board. Provide sets of ceramic bypass capacitors (10 to 100 nF) distributed over the board. On the V_{DD} (12V) and V_{CC} (5V) buses, use one capacitor for each group of four 14-pin DIPs (or equivalent). On the V_{BB} (−5V) bus, use a bypass capacitor for every 14-pin DIP (or equivalent). For additional guidance on the selection of bypass capacitors, refer to question 47 in the first article of this series (EDN, November 13, 1986, pg 260).

28. Have you evaluated your distribution techniques for ground and V_{DD} buses? Question 45 of part 1 (EDN, November 13, 1986, pg 258) contains information on pc-board layering and advice on the use of bus-bar components. Rogers Corp's Q/PAC Div (Tempe, AZ) sells a flat-plate decoupling capacitor that fits underneath a DIP RAM, sharing the voltage-supply and ground holes drilled for the IC.

29. Have you used field-programmable ROMs? If so, check the programming procedures carefully. Devices from the same family don't necessarily use the same procedures. For example, if you have equipment designed in the 1970s and it's in need of replacement parts, the programming operation for the 1602 and 1702 forces ones to zeros, but the programming operation for the 1602A and 1702A forces zeros to ones.
For modern field-programmable ROMs, there are wide variations in the programming procedures recommended by the various vendors of devices that are nominally identical in pinout and function. Don't assume that the programming method for a given device will work correctly with a similar device from a different vendor.

30. Have you carefully evaluated the production and compatibility claims of possible vendors? Memory components are more complex than standard MSI devices, and it's far more difficult to find a second source for them. Some dynamic memory components are known to have undergone at least eight revisions by the prime vendor.

31. Have you correctly interpreted the read/modify/write timing requirements for the dynamic RAM you've selected? Some types latch ones in the input data, other types latch zeros, and yet other types have no latch at all. Examining the read/modify/write sequence is the best way to discover these differences among nominally interchangeable RAMs.

32. Do the memory devices you've selected require a

separate substrate bias supply? Many dynamic RAMs require a substrate bias supply (V_{BB}) to ensure correct operation. High currents may be drawn unless this bias supply is raised before the main supply and dropped after the main supply. If the bias supply is reversed, even transiently, the parasitic substrate transistor will draw extremely high currents. Also, because the internal capacitances of the RAM are terminated to the substrate, very good transient bypassing is required.

EDN

Acknowledgment

The author gratefully acknowledges the help of his associates Drs Támas Hetényi, János Selmeczi, and Lázlo Drimusz for their review of and help with these check lists. All three are staff members at the Technical University of Budapest, Hungary, and have worked at Design Automation while on leave from that university. Dr Donald E Nelsen of Digital Equipment Corp contributed information on CMOS latch-up.

Author's biography

Nathan O Sokal is president of Design Automation Inc (Lexington, MA), a company that does electronic design and design reviews on a consulting basis. Nat received his BSEE and MSEE from MIT, is a senior member of the IEEE, and acts as a technical advisor to the American Radio Relay League. He enjoys ethnic-food restaurants.

Article Interest Quotient (Circle One)
High 482 Medium 483 Low 484

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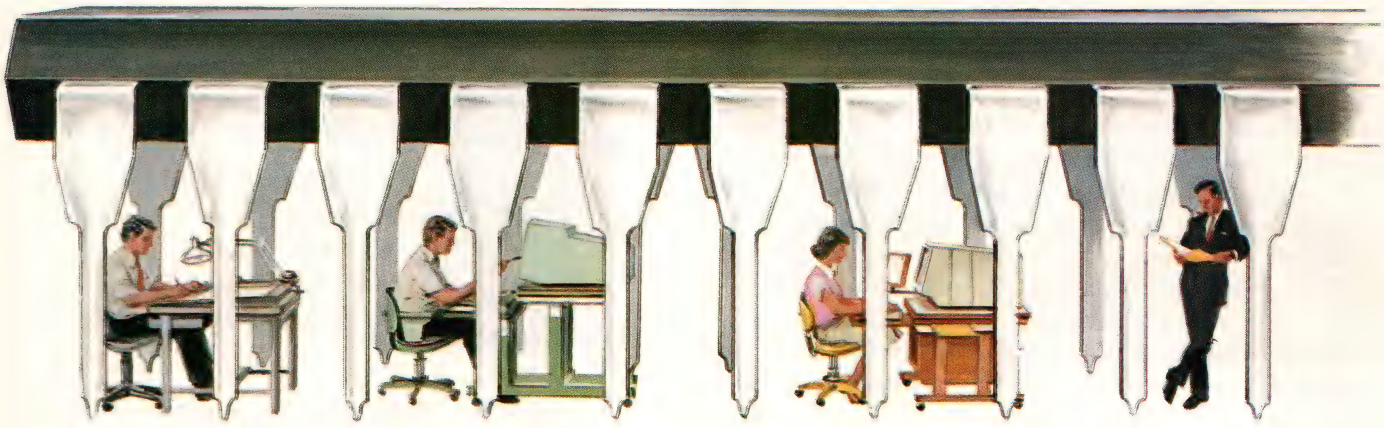

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CMOS circuit generates short pulses

H Ward Silver
RBR Engineering, Vashon, WA

Comprising two low-power, CMOS chips, the pulse generator shown in **Fig 1** produces a precise pulse width in the 50- to 500-nsec range. IC_1 is a dual monostable multivibrator (one-shot) in which each positive trigger pulse initiates simultaneous positive output pulses at pins 6 and 10. In response, the XOR gate, IC_2, produces a positive pulse whose duration is equal to the difference between the two input-pulse durations.

Section 1 of the one-shot generates an approximate 1-μsec reference pulse (shorter pulses are more subject to manufacturing variations caused by parasitic layout capacitance). Variable capacitor C_2 lets you adjust this pulse width. Section 2 of the one-shot generates a variable-length pulse; you adjust its width by using potentiometer R_3. Resistors R_4 and R_5 set the output pulse's maximum and minimum width, respectively. Because the XOR gate's rise and fall times are about 20 nsec for reasonable values of load capacitance, you should calibrate the circuit (using C_2) for a minimum output-pulse width of 50 nsec.

All the resistors should have similar temperature coefficients. Further, if the capacitors' temperature coefficients are of equal and opposite magnitude, the output-pulse width will be relatively insensitive to variations in temperature. Note that there's a delay of approximately 1 μsec between an input trigger and the resulting output pulse. **EDN**

To Vote For This Design, Circle No 747

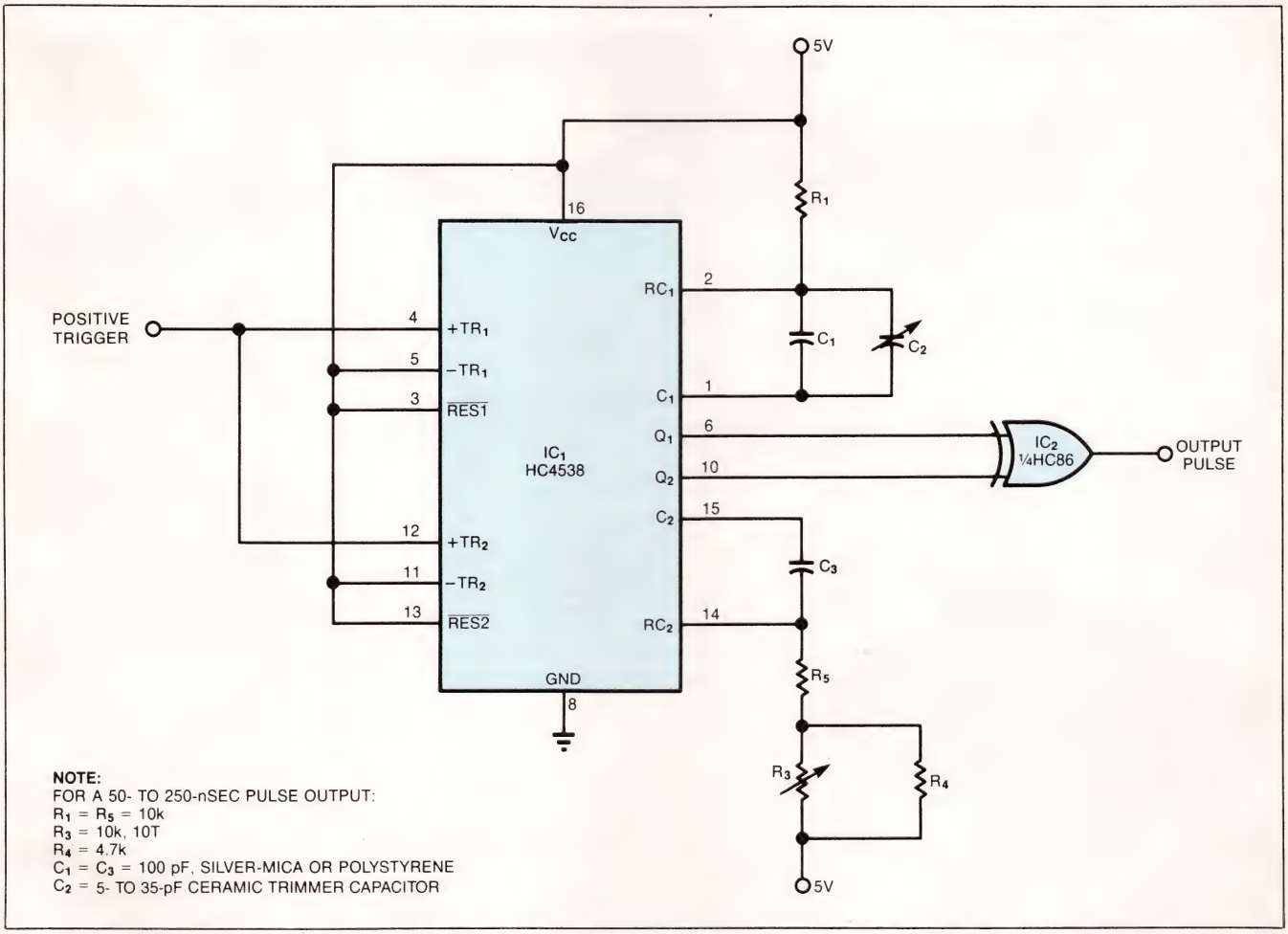

Fig 1—This circuit provides narrower pulses *than CMOS can normally deliver. The XOR gate, IC_2, combines pulses of unequal length from the dual one-shot, IC_1, to produce a short, positive output pulse.*

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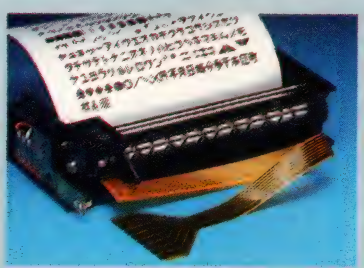

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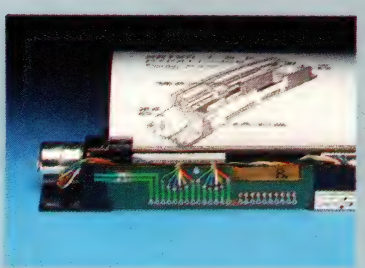

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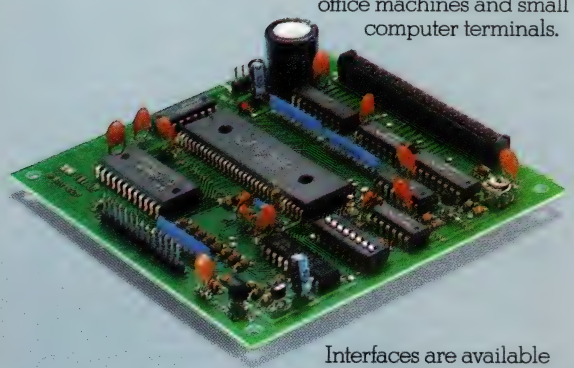

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SEIKO INSTRUMENTS

CIRCLE NO. 76

Arbiter lets two μPs use common RAM

Jim Wojcik
Allen-Bradley Co, Highland Heights, OH

The arbiter circuit shown in **Fig 1** allows two microprocessors to access a common RAM (not shown) through address buffers and data transceivers. When either μP alone seeks access to the RAM, the circuit introduces a maximum delay of only 6 nsec.

If either μP requests access to the common RAM (by asserting its RAM-enable signal) while the other μP has access, the circuit will put the requesting μP on hold by asserting the appropriate wait signal. This signal deactivates when the first μP finishes (its RAM enable goes high) and allows the second μP to complete its memory cycle.

The data input of each flip-flop is wired high, so Q outputs are high and $\overline{Q}$ outputs are low when a RAM access is not in progress. Then, when either μP requests access, the corresponding flip-flop's outputs change state in response to a low on that flip-flop's CLR input. As a result, the four output signals grant access to the requester and force the other μP to wait.

To prevent the circuit from forcing both processors to wait in response to near-simultaneous requests for access, you connect OR gate IC_{2A} to give one processor priority. To give priority to μP_1, for example, you connect the OR gate's output to IC_{3A}'s PR input as shown. To give priority to μP_2, you'd make the connection shown by the dotted line. In either case, you connect the PR input of the low-priority μP to 5V. **EDN**

To Vote For This Design, Circle No 750

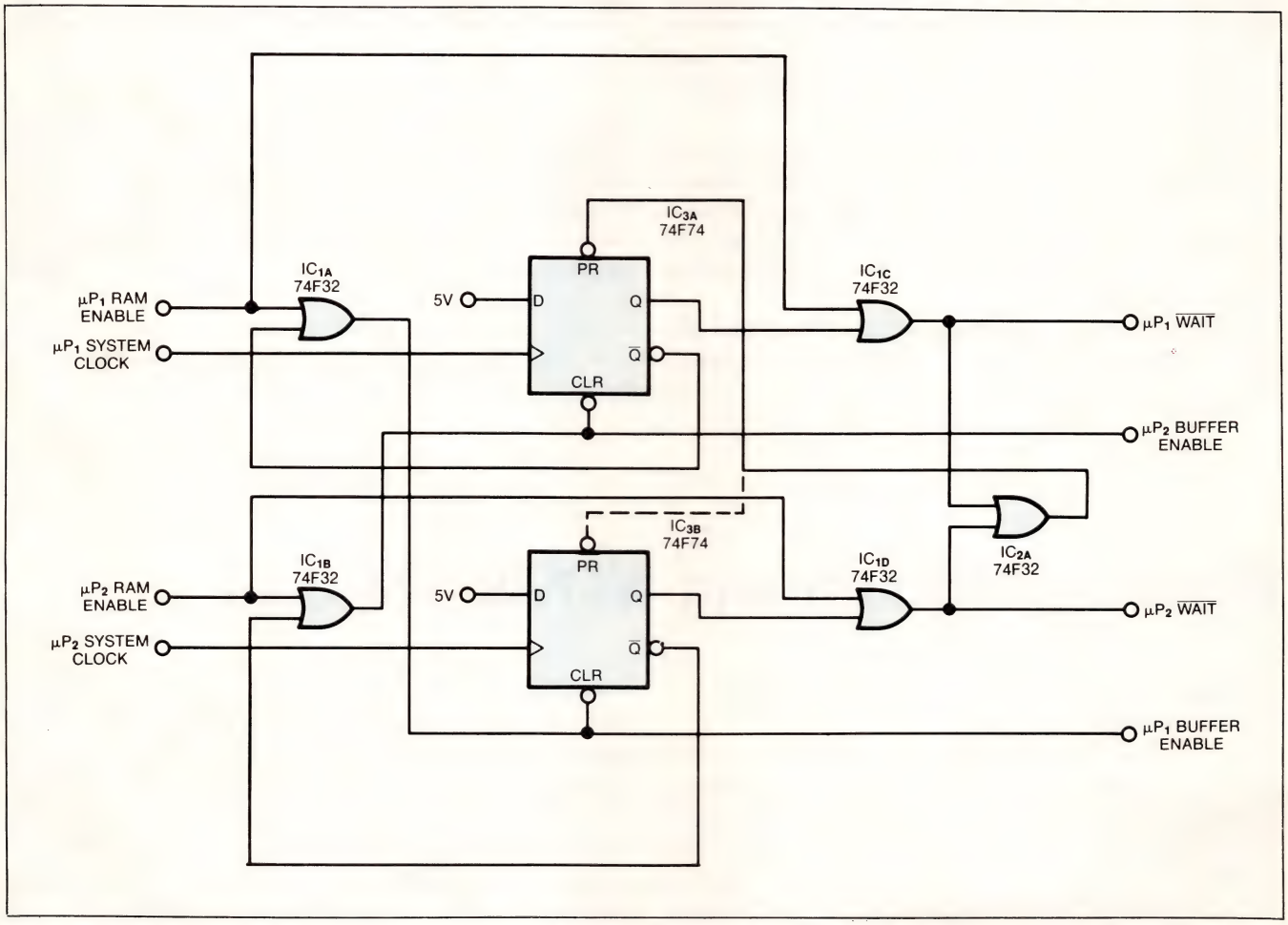

Fig 1—This circuit arbitrates between two microprocessors *requesting access to a common RAM. In the event of simultaneous requests, IC_{2A} grants priority according to a connection made by the designer.*

Op amp provides a current and voltage source

Scott Wayne
Analog Devices Inc, Norwood, MA

You can obtain a controlled source of voltage ($-V_R$) and current ($V_R/2R$) by using a single op amp and four transistors (**Fig 1**). The current and voltage outputs track the reference voltage. Moreover, they show little variation with temperature because the circuit compensates for changes in the transistors' beta and base-emitter voltage. For best results, you should use a single-chip array for the transistors and another one for the R-value resistors.

Transistors Q_1 and Q_4 form a current mirror that generates I_O by replicating Q_1's collector current. To calculate V_O, note that the currents through R_1 and R_2 are equal, so the voltage across R_2 is $V_R/2$. Similarly, the voltages across R_3 and R_4 are equal, because currents through these resistors are the same. Further, the voltage across R_4 is $V_R/2$ minus one base-emitter voltage (V_{BE}), so Q_1's base-collector voltage is also $V_R/2-V_{BE}$. Therefore, Q_1's collector-emitter voltage is $V_R/2$, and $V_O=-V_R$.

Without compensation, each transistor's V_{BE} would change about -2.2 mV/°C, making V_O vary with temperature. Q_2 and Q_3 prevent this variation by creating a temperature-dependent current in R_3 that moves the base voltage of Q_1 and Q_4 in a direction opposite to the change in V_{BE}.

You should choose the value of R_3 and R_4 so that the collector current of Q_2 and Q_3 will equal the collector current of Q_1 and Q_4. The matched currents and the circuit's symmetry ensure that all betas and collector currents will remain equal as temperature varies, provided that the transistors are well matched. Capacitor C_1 reduces output noise by limiting the circuit's bandwidth. **EDN**

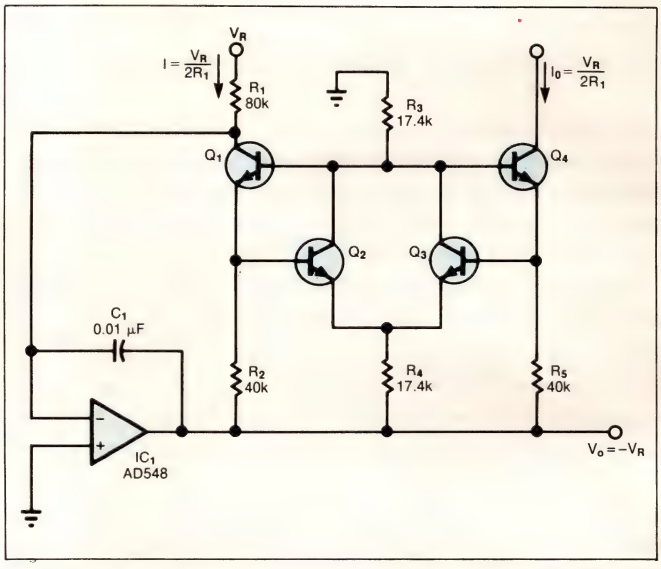

***Fig 1—This single-op-amp circuit generates** temperature-stable current- and voltage-source outputs that track the reference voltage (V_R).*

To Vote For This Design, Circle No 748

Protect EEPROM and NOVRAM data

Duc Ngo
Intel Corp, Folsom, CA

You should protect nonvolatile read/write memories, because an unwanted write cycle during power-up or power-down can corrupt the memories' contents. EEPROMs have several write-inhibit modes (**Fig 1a**), which can be the basis for memory-protection circuits that hold a signal low or high when V_{CC} is below a preset level.

The voltage-detection device shown in **Fig 1b** (IC_1) holds the EEPROM's $\overline{OE}$ input low whenever V_{CC} drops below the alarm level (3.0 to 4.75V) set by R_3. IC_1's open-collector output (pin 4) goes high again only when V_{CC} rises above the preset alarm level. To provide normal system operation, you must wire-OR this output with the system's $\overline{RD}$ command. The open-collector buffer adds only a few nanoseconds of delay. You can use a similar circuit (**Fig 1c**) to hold the EEPROM's $\overline{CE}$ or $\overline{WE}$ input high when V_{CC} is below a preset level.

Fig 2 shows another method of implementing power-fail protection for EEPROMs or other NOVRAMs. IC_1, a dedicated power-fail-protection IC, combines the functions of the circuits shown in **Figs 1b** and **1c.** IC_1 is preset to sense V_{CC} levels below 4.5 to 4.6V, and it provides active-high and active-low outputs (pins 6 and 5) that change state when V_{CC} rises above the threshold. The chip's internal delay circuit lets you delay this output response as required. **EDN**

To Vote For This Design, Circle No 749

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	IMPLEMENTATION
1	X	X	HELD HIGH
X	0	X	HELD LOW
X	X	1	HELD HIGH

(a)

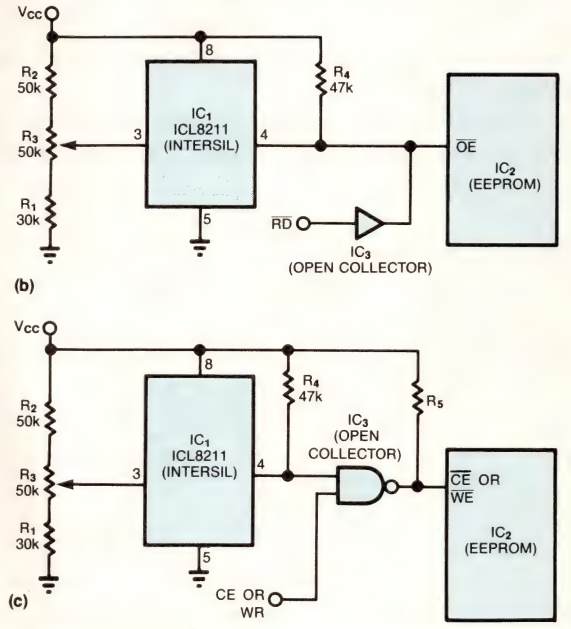

Fig 1—An EEPROM's write-inhibit inputs (a) *are the basis for memory-protection circuits that hold a signal low* ***(b)*** *or high* ***(c)*** *while V_{CC} is below a preset level.*

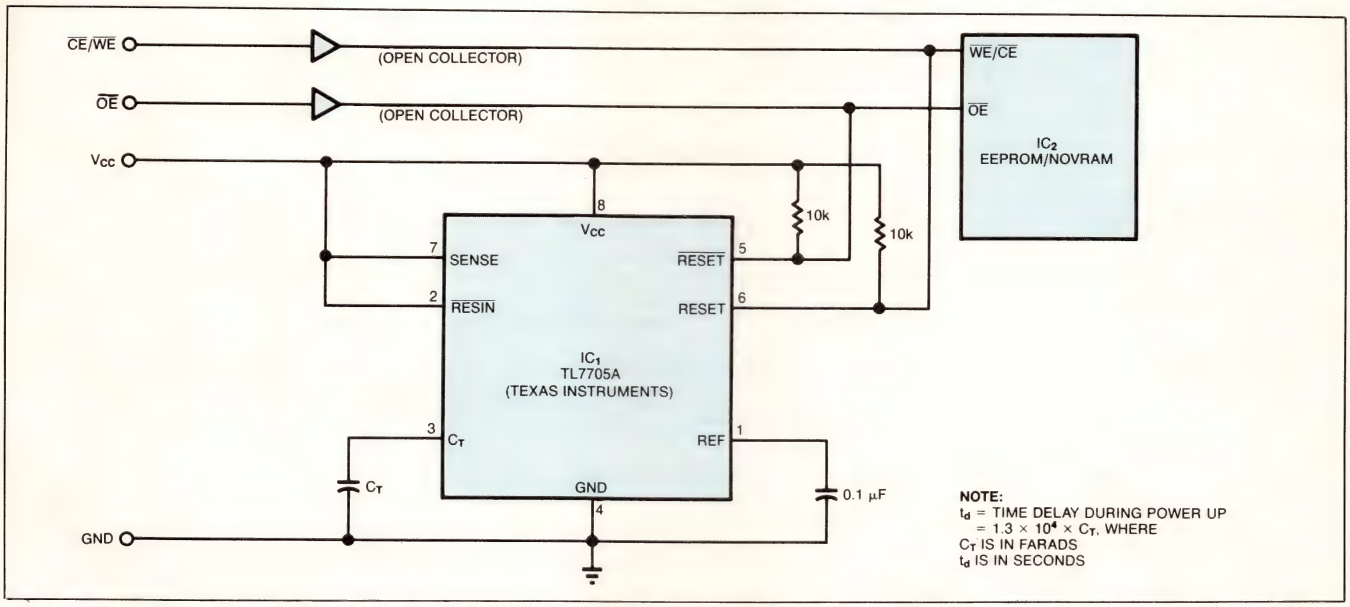

Fig 2—IC_1 offers active-high and active-low outputs *that inhibit an EEPROM or other NOVRAM when V_{CC} is below about 4.5V. In addition, IC_1 can delay activation of the memory after power-up.*

Delay circuit handles digital waveforms

Irwin Cohen
Hewlett-Packard Co, Rockaway, NJ

The circuit shown in **Fig 1** delays every transition of digital input **A** by approximately $0.9R_1C_1$. The circuit will delay any digital input by this amount, provided that the waveform's high and low intervals are greater than the selected delay time plus the RC network's discharge time.

Complementary waveforms **F** and **G** (**Fig 2**) gate

waveforms **A** and **B** to the input of IC_{2C}. The resulting output, **C**, which is composed of segments of **A** and **B**, initiates a positive charging of C_1 (waveform **D**) for each transition of input **A**.

The Schmitt inverter, IC_{1B}, changes state when C_1's voltage crosses the inverter's upper switching threshold. This action ripples around the loop, discharging C_1 through D_1 and creating the narrow pulses (**E**) that clock flip-flop IC_3. **EDN**

To Vote For This Design, Circle No 746

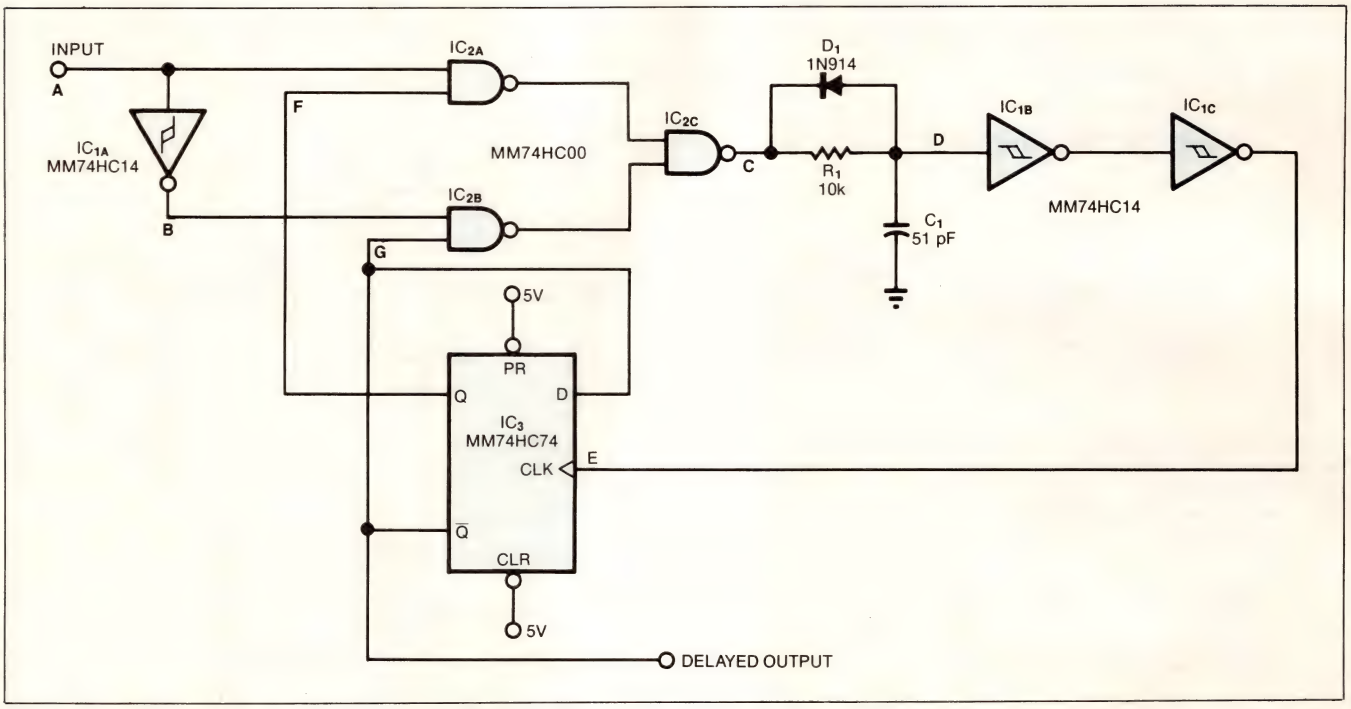

Fig 1—This digital-delay circuit *uses a single RC delay network that charges in the same direction for positive and negative transitions of its input.*

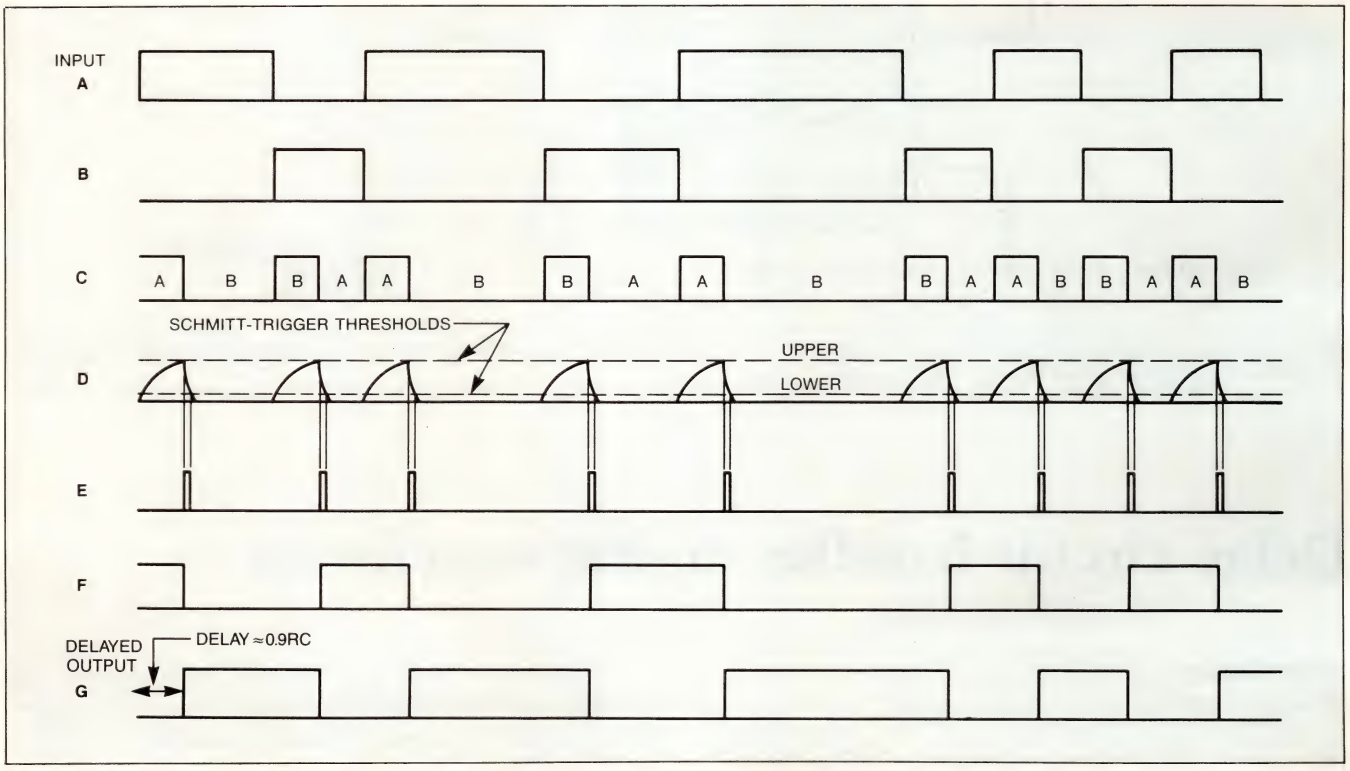

Fig 2—Selected waveforms from Fig 1 *show how the circuit generates a time delay of* $0.9R_1C_1$.

99¢

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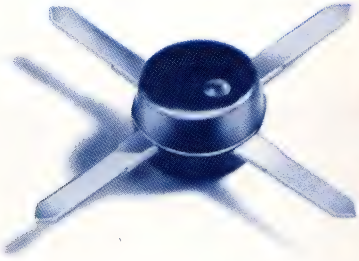

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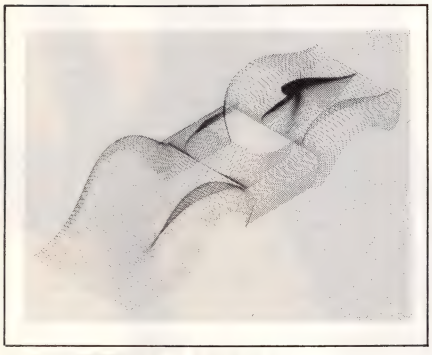

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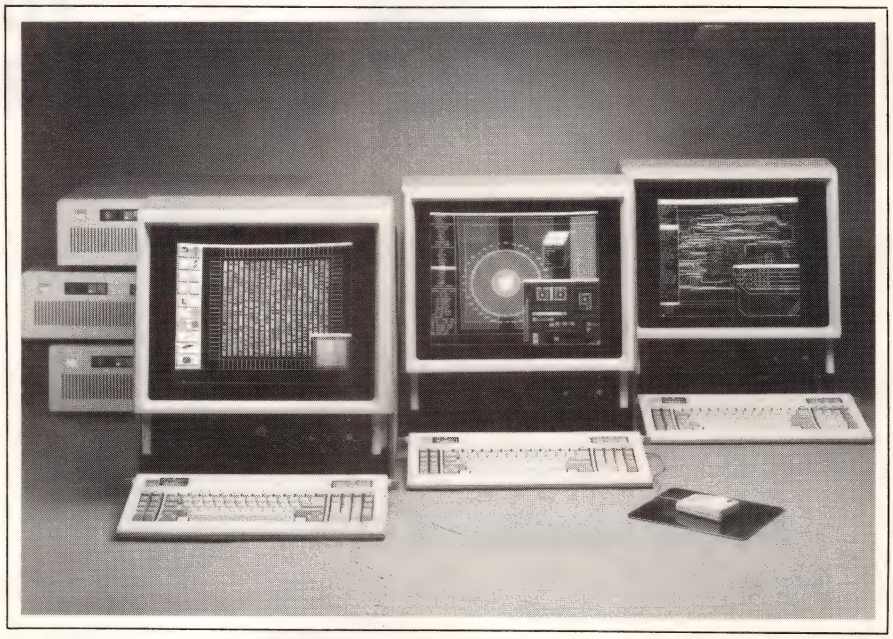

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- *Interfaces to pc-board layout package*

The Hiwire schematic-drawing package extracts symbols from a library of 700 components and connects the components with wires and buses. You can create new symbols by combining labels, lines, and arcs. The package includes net-list and bill-of-materials utilities. Using the package, you can produce hard copy on either a plotter or a dot-matrix printer. The software runs on IBM PCs and includes a 30-day money-back guarantee. $895.

Wintek Corp, 1801 South St, Lafayette, IN 47904. Phone (800) 742-6809; in IN, (317) 742-8428.

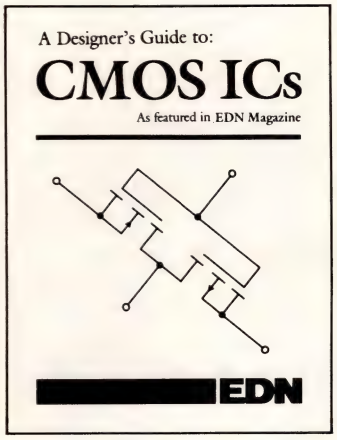
Circle No 355

ANALOG SIMULATION

- *Models system-level analog designs*
- *Has simulated an 8000-transistor circuit in 15 minutes*

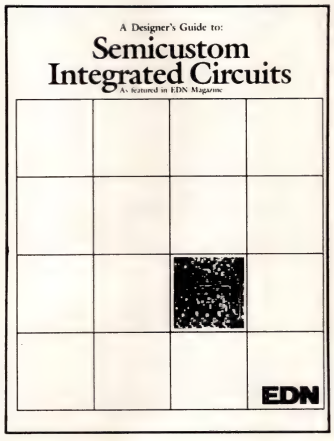
The Saber analog-simulation package can model board- or system-level designs. Because you can use

EDN REPRINTS



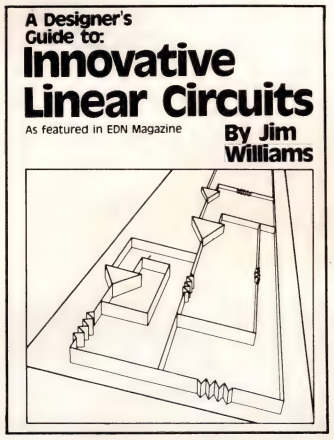
A Designer's Guide to CMOS ICs

CMOS is fast becoming the chosen technology for developing integrated circuits. That's because CMOS ICs are able to implement ultra-complex system-level functions on a chip! Now you can meet the special challenges posed by this new breed of ICs with *A Designer's Guide to CMOS ICs.* You'll learn the advanced design and fabrication techniques required. Plus the latest linear and digital CMOS ICs available.



A Designer's Guide to Semicustom Integrated Circuits

Learn how to design a semicustom IC with *A Designer's Guide to Semicustom Integrated Circuits.* Based on EDN's own design experience, this nine-chapter booklet outlines the complete procedure used to design, fabricate, and test EDN 1, a chip with a 1200 equivalent-gate complexity. You'll not only learn the steps to take when creating ICs, but also the design/cost analyses and vendor-interface methods that lead to successful semicustom chips.



A Designer's Guide to Innovative Linear Circuits

As exciting as digital technology is, you still need analog circuitry to operate on signals from real-world sources. Now, EDN is offering a wealth of analog design information in *A Designer's Guide to Innovative Linear Circuits.* This 186-page collection of articles was developed by Jim Williams, one of America's foremost linear-circuit designers. It includes practical and efficient ways to use op amps, comparators, data converters, and other analog ICs, and discusses the theories behind all the design techniques presented.

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EDN112786

the package to design any physical system that you can describe in mathematical equations (even sensors, actuators, or disk drives), you can use this package to simulate electrical, mechanical, chemical, and hybrid systems. The software's library contains 100 analog components. Because the code is optimized for vector and parallel processing, you can accelerate your simulations by adding processing hardware to your workstation. Even without additional hardware, this software simulates average-sized circuits about 10 times faster than does Spice, the company claims. The package has simulated an 8000-transistor circuit on an IBM mainframe in 15 minutes. The program runs on DEC VAX computers; IBM mainframes; and Sun, Apollo, and MicroVAX II workstations. It provides dc operating-point analysis, dc transfer characteristics, transient analysis, small-signal ac analysis, and parameter sweep. The program lets you define models, and it also accepts models that run in Spice. From $9000 (for workstations) to $60,000 (for mainframes).

Analogy Inc, 8605 SW Creekside Pl, Suite D, Beaverton, OR 97005. Phone (503) 626-9700.

Circle No 356

PC-BASED CAE/CAD

- *Two packages, one for schematic editing, one for pc-board layout*
- *Redraws a 150-IC board layout in <60 sec*

The Criterion I package consists of a schematic editor and component libraries. The Criterion II provides pc-board layout to the Criterion I user. Using an Artist I card from Control Systems (St Paul, MN), the layout package redraws a 150-IC board in <60 sec. This graphics-controller card interfaces to a 1024×768-pixel 16-color display; it has hardware zoom and pan. A second monitor is necessary for status and input control. The schematic editor can use the 640×350-pixel EGA card. Both packages include seven libraries: TTL, CMOS, ECL, analog, digital, μPs, and surface-mount devices. The two packages require 2M bytes of hard-disk storage. Both packages require an IBM PC/XT, PC/AT, or compatible with a mouse and a math coprocessor. The software includes a 30-day money-back guarantee. Criterion I, $1000; Criterion II, $4000; Artist I card, $5200.

Aptos Systems Corp, 4113 Scotts Valley Dr, Scotts Valley, CA 95066. Phone (408) 438-2199.

Circle No 357

FILTER DESIGN

- *Filters can include two to 20 resonators*
- *Calculates rod and tap dimensions*

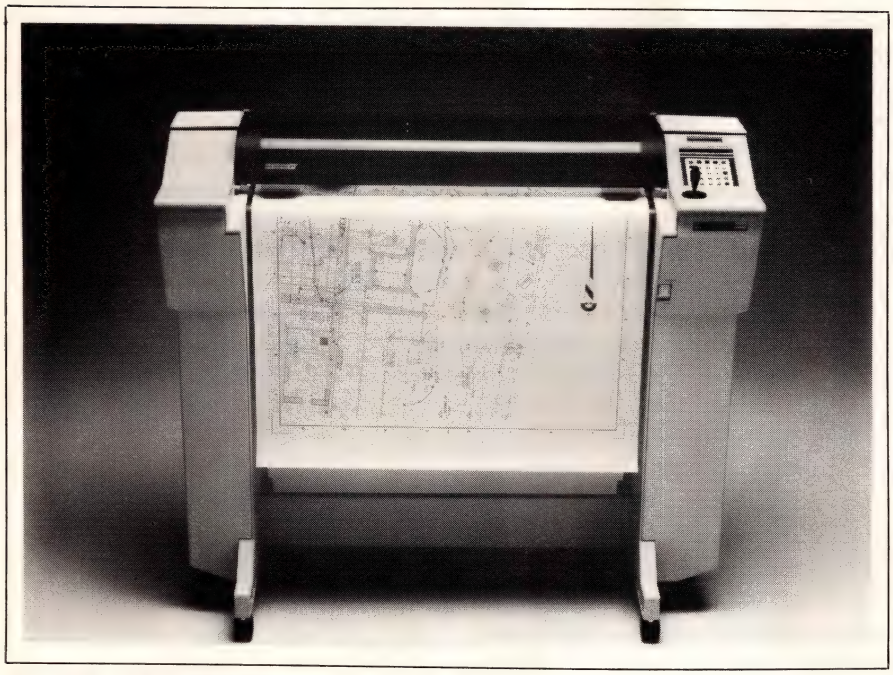
Filter III:Combline Design enables you to design comb-line bandpass filters. The filters use constant-diameter rods and feature exact equal-ripple passband response. The package lets you design filters that can include two to 20 resonators. You can add the capacitive loading to either the cover or the resonator. The program creates equivalent circuits that contain all line-element impedances and resonator-loading capacitances. It generates design files and response tables and calculates current as a function of voltage. The design files include rod dimensions, capacitive-loading elements, tap position, tap-line dimensions, and line-element impedances. You can transfer the current-vs-voltage data to the company's linear-analysis package and produce a graphic display of your filter design. The program runs on IBM's PC/XT and PC/AT, Hewlett-Packard's Vectra PC, and compatibles. $7500.

EEsof Inc, 31194 La Baya Dr, Westlake Village, CA 91362. Phone (818) 991-7530.

Circle No 358

NEW PRODUCTS

COMPUTERS & PERIPHERALS



24-IPS PLOTTER

- *Has an 8-pen turret with automatic pen capping*
- *Offers 0.0005-in. resolution*

Capable of plotting at 24 ips, the 1041GT has an acceleration rate reaching 1.2g and a resolution of 0.0005 in. It makes A- to D-size drawings on a variety of cut-sheet media. Other features include an 8-pen turret with automatic pen capping, an integrated communications interface, nonvolatile setup memory, and self-test diagnostics. Optical sensors in the turret determine whether a selected pen has a ballpoint, fiber, or plastic tip so that the plotter can automatically adjust its parameters for optimum plot quality and throughput. Or you can override the automatic adjustments by programming the pen force, velocity, and acceleration parameters. The nonvolatile setup memory lets as many as four users save such setup parameters as communications mode, baud rate, scaling, rotation, pen velocity/acceleration, and log-on messages. $6495.

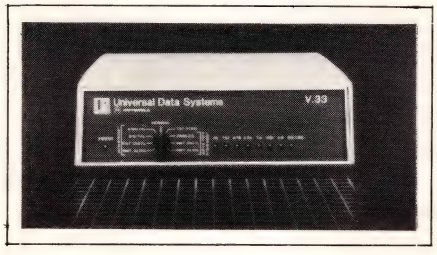
CalComp, 2411 W La Palma Ave, Anaheim, CA 92801. Phone (714) 821-2142.

Circle No 359

LEASED-LINE MODEM

- *Transmits full-duplex data at 14,400 bps*
- *Offers CCITT V.33 and CCITT V.29 compatibility*

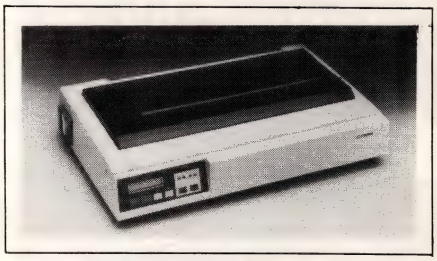
If you have unconditioned 4-wire private telephone lines, you can transmit full-duplex data at speeds reaching 14,400 bps with a Model V.33 modem. It uses Trellis-coded modulation and automatic adaptive



equalization to reduce transmission errors. The unit's diagnostic circuits test for communication faults and locates them to the modem, the phone line, or the terminal equipment. If the line quality deteriorates, the modem automatically falls back to CCITT V.33-compatible, 12,000-bps operation. Further line-quality deterioration results in an automatic reduction to CCITT V.29-compatible, 9600-bps operation. $5995.

Universal Data Systems, 5000 Bradford Dr, Huntsville, AL 35805. Phone (205) 837-8100. TWX 810-726-2100.

Circle No 360



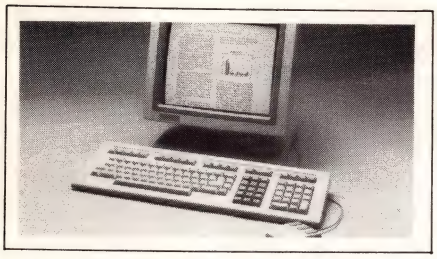
24-PIN PRINTER

- *Prints in seven colors*
- *Uses credit-card-size customizing cartridges*

Producing 300 cps in draft mode and 100 cps in letter-quality mode, the Prowriter C-715 Reliant is a 24-pin dot-matrix printer that prints in seven colors. Plug-in cartridges that are the size of credit cards let the printer emulate the IBM Proprinter XL, Epson LQ-1000, Toshiba 351, Diablo 630, and other printers. You can select print features from the unit's front panel, which is equipped with a 16-digit LCD. This printer provides a 32k-byte buffer, a quiet mode, proportional printing, automatic paper loading, bottom paper feed, a push-pull tractor, and both Centronics parallel and RS-232C serial interfaces. $1295.

C Itoh Digital Products Inc, 19750 S Vermont Ave, Suite 220, Torrance, CA 90502. Phone (213) 327-2110.

Circle No 361



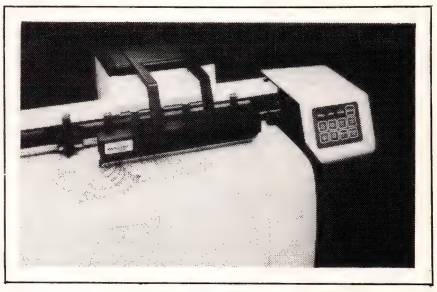
COMPOSITE TERMINAL

- *Lets you preview laser-printer output*
- *Stores 30 spaced, bit-mapped fonts in ROM*

Providing a terminal that lets you preview the output of the manufacturer's line of laser printers, Model T7800 comes with 30 ROM-resident proportionally spaced fonts that you can display on a 1024×780-pixel screen. Or you can use the terminal's 300k bytes of RAM to download fonts, display lists, graphics, and raster patterns from your host computer. The terminal comes with a page-previewing program called Pretext that supports the Tex computerized typesetting language. The terminal has built-in serial drivers for the manufacturer's 810 and 610 laser printers, HP's Thinkjet, DEC's LA-50 and LA-100, and Epson and Okidata printers. The terminal includes a DEC VT220-style keyboard and a 14-in. white-phosphor CRT with a tilt-swivel stand. Amber phosphor is available as an option. $2890.

Talaris Systems Inc, Box 261580, San Diego, CA 92126. Phone (619) 587-0787.

Circle No 362



E-SIZE PLOTTER

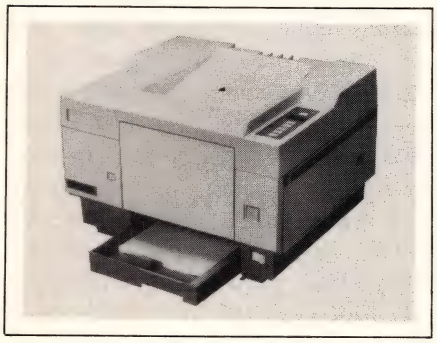
- *Has 22-ips plotting speed*
- *18 adjustable media sizes*

Able to accommodate 18 different media sizes ranging from 8½×11- to 36×48 in., the DMP-56A produces A- through E-size drawings on paper, vellum, or matte film. You can operate this servo-driven plotter with any computer that has an RS-232C interface. The plotter includes menu-driven front-panel selection for choosing and changing such parameters as acceleration, velocity, resolution, pen position, delay time, paper size, character set, font, parity, and baud rate. Because the Digital Microprocessor Plotting Language (DM/PL) is built in, the plotter can execute complex graphics from simple commands. Maximum plotting speed is 22 ips; acceleration rate is adjustable to 2g; resolution can be as fine as 0.001 in.

An optional 6-pen carousel lets the plotter change pens automatically. $5995; carousel, $995.

Houston Instrument, 8500 Cameron Rd, Austin, TX 78753. Phone (800) 531-5205; in TX, (512) 835-0900. TLX 776438.

Circle No 363



LASER PRINTER

- *Produces 12 pages/minute*
- *Lets operator perform all maintenance*

You can handle all the maintenance functions for the L1012 laser printer, which provides 12 pages/minute and 300×300-dots/in. resolution. This printer includes a 250-sheet automatic paper cassette and a second 50-sheet paper tray. Both paper-handling devices accept letter- and legal-size paper, envelopes, and labels. Another standard feature lets you select face-up or face-down stacking. Font cartridges provide different type styles and include superscript, subscript, and underlining. $2995.

Printronix Inc, Box 19559, Irvine, CA 92713. Phone (714) 863-1900. TLX 910-595-2535.

Circle No 364

SMALL TAPE DRIVES

- *Occupies 24¾ in² of desk space*
- *40M bytes of storage per cassette*

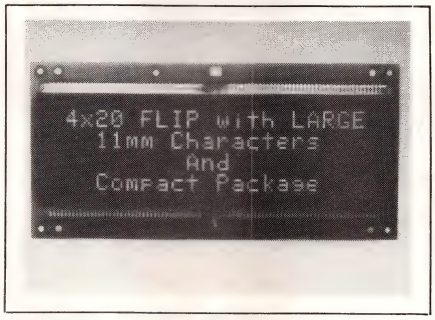
Suitable for use with an IBM PC/XT or PC/AT, the 400 Series backup tape subsystems occupy 24¾ in² of desk space—about the size of a paperback novel. Three models let you select storage capacities of 10M bytes, 20M bytes, or 40M bytes per tape cassette. Each drive uses a patented head-positioning feature and a proprietary error-correction scheme. Menu-driven software is included that lets you copy an entire hard disk or selected files. The 40M-byte drive can also read 10M- and 20M-byte tapes. According to the manufacturer, 400 Series drives can recover data from damaged tape. Prices range from $799 for the 250k-bps, 10M-byte Model 410 to $1095 for the 500k-bps, 40M-byte Model 445.

Irwin Magnetics, 2101 Commonwealth Blvd, Ann Arbor, MI 48105. Phone (313) 996-3300.

Circle No 365

DISPLAY

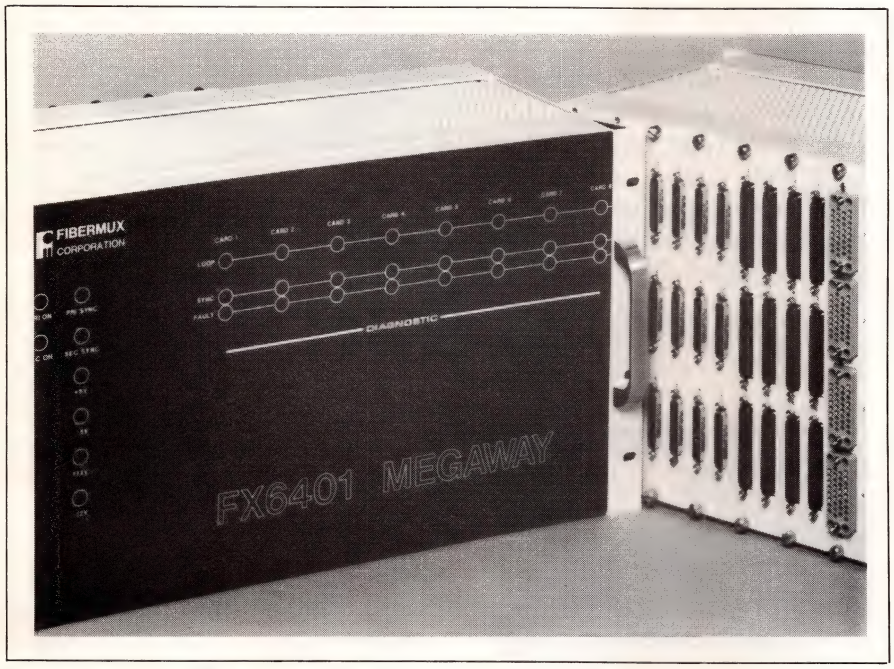
- *4-line×20-character fluorescent module*
- *Readable from 10 ft*



The Model 3601-24-080 4-line×20-character fluorescent display module measures 10×4.75×1.57 in. The 11.3-mm characters are formed from 15×7-dot matrix that you can read easily from a distance of 10 ft, according to the manufacturer. The display requires a 5V dc power supply. An onboard μP controls all the display functions and interfaces to an 8-bit parallel TTL data bus. A 1200-baud serial interface is also standard; a jumper lets you select either TTL or RS-232C input levels. The module displays the full 96-character ASCII font as well as European characters. Display characters are blue-green; the brightness level is 160 fL typ (you can dim it to approximately 80 fL). A spectrum of color filters is available. $274 (100). Delivery, four to six weeks ARO.

IEE Inc, Industrial Products Div, 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 787-0311. TLX 4720556.

Circle No 366



F-O MULTIPLEXER

- *48 channels for use with single- and multimode cables*
- *Transmission speeds from 300 to 2M bps*

This 48-channel multiplexer, the FX6401, is for use with both single- and multimode fiber-optic cables, and it handles speeds from 300 to 2M bps. It works with common interfaces, including RS-232C, RS-449, and MIL-188. Three models are available: for single-mode fiber, the FX6401/SM (to 10 mi); for multimode fiber, the FX6401/H (to 5 mi); and the FX6401/L (to 2 mi). Options for master clocking, selectable in the field, allow various hub and tandem configurations when connected to existing networks. An integrated test set continually monitors end-to-end system performance and switches over to a standby common-logic module and standby fiber when necessary. $3500 to $20,000.

Fibermux Corp, 21630 Lassen St, Chatsworth, CA 91311. Phone (818) 709-3782.

Circle No 367

VOLTMETER

- *Features display span of ±19,999 counts*
- *Specs an accuracy of 99.98%*

The Model 2001 ac-powered, 4½-digit dc voltmeter features true-differential input for noise rejection. Its display span is ±19,999 counts; the accuracy is 99.98%. The voltmeter provides full-scale ranges from ±1.9999 to ±99.99V dc; four programmable decimal points; and autozero and autopolarity capabilities. Common-mode noise rejection is 120 dB. You can configure the voltmeter for 3-wire ratio measurement with 100-MΩ input impedance. The meter fits a standard ⅛-DIN panel cutout (92×45 mm) and requires a depth of less than 104 mm behind the panel. A serial BCD output is optional. Basic unit, $159.

Newport Electronics Inc, 648 E Young St, Santa Ana, CA 92705. Phone (714) 540-4914.

Circle No 368

COMPONENTS & PACKAGING

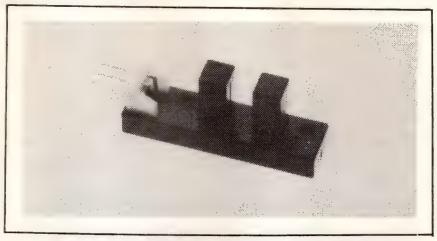


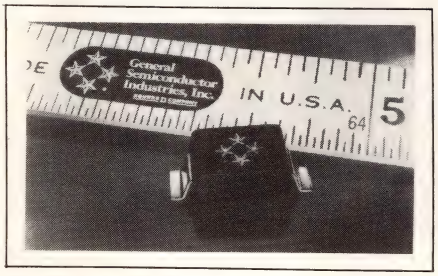
PHOTO-INTERRUPTERS

- *Includes an LED current-limited resistor*
- *Features an IR-sensitive photodiode*

Each member of the TLP1200 Series of photo-interrupters includes an IR LED lamp, a photodetector IC, an LED current-limiting resistor, and a pc board—all incorporated into one package with a connector attached. The photodetector IC features an IR-sensitive photodiode, a signal-amplification circuit, a wave-shaping circuit, and a constant-voltage circuit. The connector is compatible with standard products from such manufacturers as AMP (Japan) and Molex Japan. The photo-interrupter's slit is 0.5 mm wide. The devices' output current is 50 mA; the operating voltage is 5 or 24V dc. $2.60 to $5.20 (100). Delivery, 12 weeks ARO.

Toshiba America Inc, Semiconductor Products Div, 2692 Dow Ave, Tustin, CA 92680. Phone (714) 832-6300.

Circle No 369



SUPPRESSOR

- *Low-profile surface-mount device*
- *Operates over −65 to +150°C*

The SMB Series transient-voltage suppressor comes in a surface-mountable package that measures 0.17×0.14×0.075 in. Most pick-and-place machines can handle the device. It features 600W peak power dissipation during a 1-msec pulse; a theoretical response time of 1×10^{-12} sec; reverse current leakage of 5 μA; and an operating range of −65 to +150°C. The suppressor is available with breakdown voltages from 5 to 220V. Its 0.080-in.-wide flat leads are designed to provide a large contact area for heat dissipation and a low resistance path for surge current flow to ground. Two lead configurations are available: a gull-wing configuration and a J-bend configuration. $0.82 (5000).

General Semiconductor Industries Inc, Box 3078, Tempe, AZ 85281. Phone (602) 968-3101. TWX 910-950-1942.

Circle No 370

VIDEO ENCODER

- *Encodes from analog RGB to NTSC composite video*
- *Has its own power supply*

The Model ENC-1 is a composite video encoder for converting standard analog RGB and synchronous color-video signals to standard NTSC composite video signals. In order to prevent dot (or chroma) blurring on vertical color edges, the device locks the color burst to a sync signal. The encoder has its own power supply, a 9-pin DIN female input connector, and a BNC female output connector. It drives a 75Ω load. Interface cables are available for a variety of graphics boards and applications. $295.

Communications Specialties Inc, 6090 Jericho Tpk, Commack, NY 11725. Phone (516) 499-0907.

Circle No 371

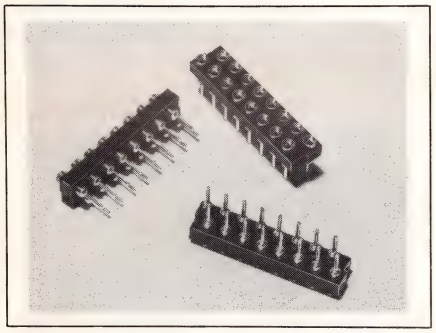
FLAT-PANEL DISPLAY

- *Features a 10:1 contrast*
- *Rise time is 50 msec*

The Model 1001 display provides a contrast of 10:1, a viewing angle of 90°, and a 50-msec rise time. This active dot-matrix display furnishes a resolution of 640×200 dots. The power requirement is 100 mW max. The display interfaces directly to IBM PCs and compatible systems. Evaluation system with display module, connector, and interface-controller board, $3000; in volume, less than $300.

LCSystems, 210 Welsh Pool Rd, Exton, PA 19341. Phone (215) 524-9944.

Circle No 398



ZIP SOCKET

- *Made for 256k-byte dynamic RAM packages*
- *Has a 0.295-in. profile*

Designed for 256k-byte dynamic-RAM packages, the ICZ Series zig-zag pattern socket has a 0.295-in. profile and screw-machined contacts. It's available in a 16-pin design with solder tails; wire-wrappable pins are available on special order. Sixteen-pin solder-tail version (ICZ-161-S-TG), $0.50 (5000).

Robinson Nugent Inc, 800 E Eighth St, New Albany, IN 47150. Phone (812) 945-0211.

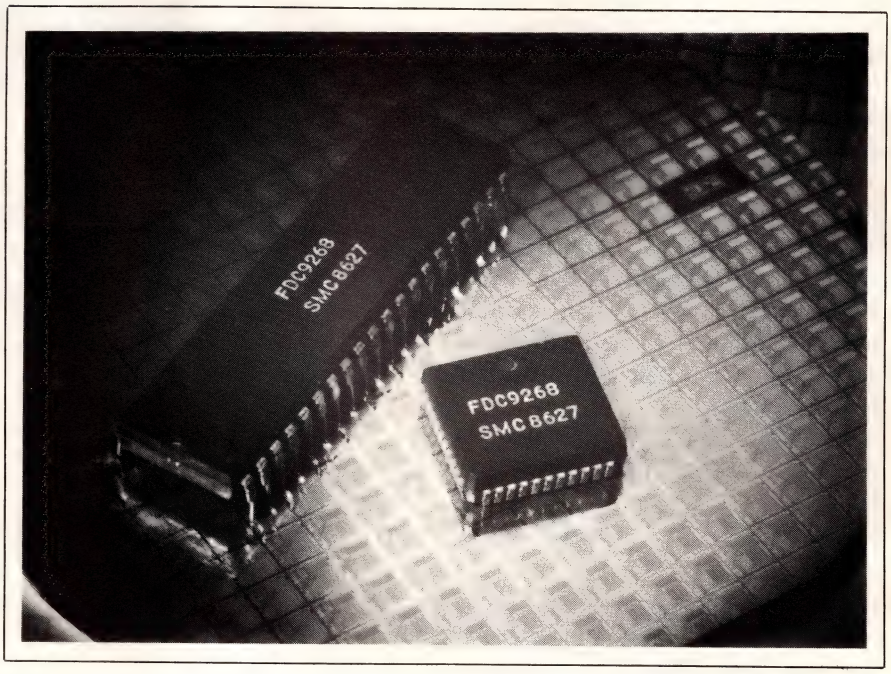
Circle No 399

NEW PRODUCTS

ICs & SEMICONDUCTORS

DISK-DRIVE CONTROLLER

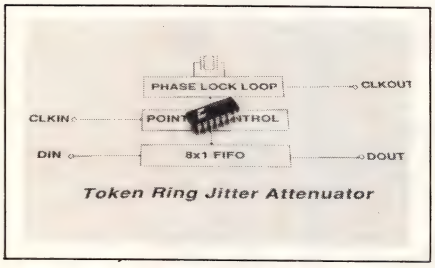
- *Controls quad-density floppy-disk drives*
- *Combines disk control with data separation*



The FDC9268 single/double-density floppy-disk controller combines the industry-standard FDC765A floppy-disk controller with a high-resolution, digital data separator on a single chip. The device provides an interface from a processor to four 3½-, 5¼-, or 8-in. floppy-disk drives. It can support the IBM 3740 single-density format, the System 34 double-density format, and the quad-density format, including double-sided recording. The controller is available in 40-pin plastic and ceramic packages and ceramic DIPs. $14.40 in plastic package (100).

Standard Microsystems Corp, 35 Marcus Blvd, Hauppauge, NY 11788. Phone (516) 273-3100. TWX 510-227-8898.

Circle No 372



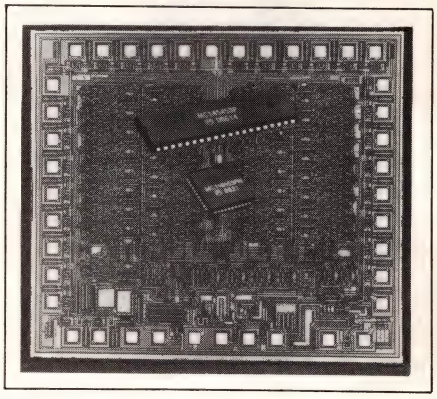
JITTER ATTENUATOR

- *Alleviates token-ring jitter accumulation*
- *Allows increasing sizes of networks*

The CS80600 token-ring jitter attenuator is an addition to the company's family of Smart Analog integrated circuits. The device operates from a 5V supply. It uses an internal phase-lock loop and an elastic store that holds eight Manchester-encoded symbols for removing as many as three unit intervals of jitter. According to the manufacturer, this process increases the possible size of a network to almost double the capacity obtainable without jitter-reduction techniques. In a 14-pin DIP, $8 (1000).

Crystal Semiconductor Corp, Box 17847, Austin, TX 78760. Phone (512) 445-7222. TWX 910-874-1352.

Circle No 373



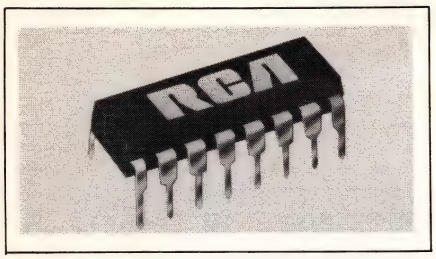
LCD DRIVER

- *Drives 33 LCD segments*
- *Operates in nonmultiplexed mode*

The MC145453 LCD driver has a serial binary-input format; this CMOS IC contains a 36-stage shift register and 33 latches and output buffers that drive as many as 33 nonmultiplexed LCD segments per package. Compared with multiplexed LCD drivers, this device features a wider viewing angle, optimum contrast at low voltage, and better legibility at extreme temperatures, according to the manufacturer. The device's backplane and frontplane drivers directly interface to 7-segment alphanumeric, bargraph, or dot-matrix LCDs. If you use the format of a start bit followed by 33 data bits, plus two trailing bits, you obtain data transfer with no external load signal. The start bit internally generates a load signal, which in turn transfers 33 bits into latches. An internal reset clears the shift register to prepare the driver for the next set of data. In a 40-pin plastic DIP, $3.57 (500).

Motorola Inc, Box 52073, Phoenix, AZ 85072. Phone (512) 928-6880.

Circle No 374



CODEC ICs

- *Meet specs of T1 and CCITT PCM systems*
- *Consume 80 mW*

The CD22354 and CD22357 telecommunications chips provide complete codec and filtering functions and eliminate external components often required for sample-and-hold and autozero operations. The chips consume 80 mW in operating mode and 5 mW in standby mode. The CD22354 chip meets or exceeds the specs of T1 PCM telephone systems in the US; the CD22357 is the equivalent device for European digital phone systems that operate according to CCITT standards. Both devices operate synchronously or asynchronously and from variable data-clock rates ranging from 64 kHz to 2.048 MHz. Both devices are equipped with electrostatic-discharge protection circuitry on all inputs and outputs. Supply voltages of +5 and −5V are required. Either model, in 16-pin DIP, $7.43 (100).

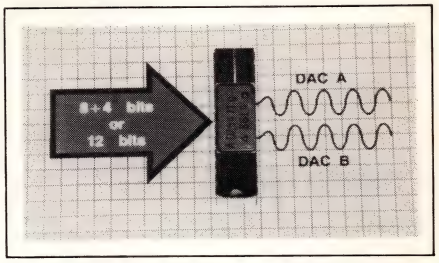
RCA, Solid State Div, Route 202, Somerville, NJ 08876. Phone local office.

INQUIRE DIRECT

DUAL D/A CONVERTERS

- *Holds two 12-bit DACs on one chip*
- *On-chip data registers*

The AD7537 and AD7547 each occupy one-half the area required by two separate 12-bit D/A converters, according to the manufacturer. Both devices contain two 12-bit current-output DACs on one chip; their bus structures differ in order to handle various types of applications. The 7537 offers a 2-byte input structure for right-justified loading from an 8-bit bus. The 7547 incorporates a 12-bit parallel-loading structure that allows you to load data in one 12-bit word. This feature facilitates loading the DAC from a 16-bit data bus. The devices operate from single 12 to 15V supplies. In 24-pin DIPs, from $14.50 (100).



Analog Devices Inc, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 329-4700. TWX 710-394-6577.

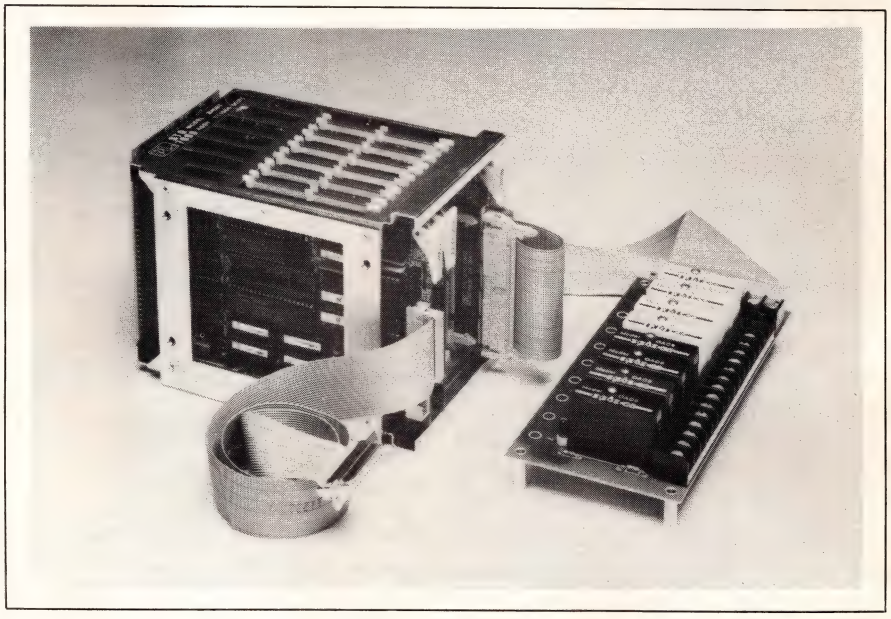
Circle No 376

NEW PRODUCTS

COMPUTER-SYSTEM SUBASSEMBLIES

CONTROLLER

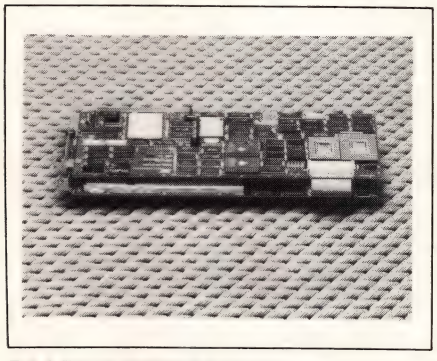
- *Programmable via programs downloaded from an IBM PC*
- *Controls as many as 6000 relays*



Because it has an open architecture, the System 1 industrial controller's ROM-based operating system can accept programs that are written in the RD-1000 ladder-logic language on an IBM PC or compatible. The unit can thus replace prepackaged programmable controllers. It includes an 8088 CPU, 64k bytes of battery-backed CMOS RAM, and an RS-232C port. The controller provides the equivalent of as many as 32 stepper drums, 20 shift registers, 120 timers, 100 counters, and 2000 set points. It controls as many as 6000 relays. When you install an optional 8087 math coprocessor chip, the unit can run 40 PID (proportional integral derivative) loops. System 1, $1695; RD-1000 software, $1750.

Pro-Log Corp, 2560 Garden Rd, Monterey, CA 93940. Phone (800) 538-9570; in CA, (408) 372-4593. TWX 910-360-7082.

Circle No 377



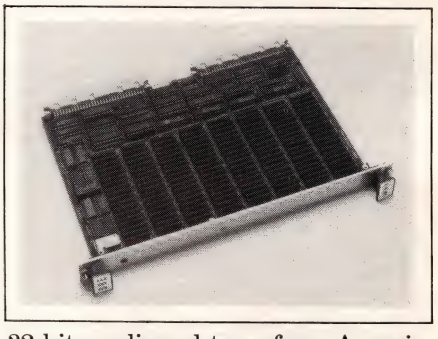
MAP INTERFACE

- *Links IBM PC/XT and PC/AT computers to MAP networks*
- *Implements 7-layer MAP architecture*

Supporting the manufacturing automation protocol (MAP), the MP-500 board set plugs into the backplane of an IBM PC/XT, PC/AT, or compatible computer. The interface requires two card slots: one for the controller board and one for the 10M-bps token-bus modem circuitry. When equipped with the manufacturer's software (downloaded over the MAP network), the interface implements the entire 7-layer communications architecture in the MAP 2.1 spec. The manufacturer also provides PC-resident software drivers that simplify the writing of applications programs. $3500 to $4000. Delivery, 60 days ARO.

Industrial Networking Inc, 3900 Freedom Circle, Santa Clara, CA 95052. Phone (408) 496-0969.

Circle No 378



MEMORY BOARD

- *Contains 4M bytes of dynamic RAM*
- *Supports 8-, 16-, and 32-bit transfers*

The VMEM-4 memory board provides 4M bytes of dynamic RAM for VME Bus-based computer systems. The board supports 8-, 16-, and 32-bit aligned transfers as well as 32-bit unaligned transfers. A variety of transfer operations alleviates concerns about memory boundary alignments. The board accommodates both 16- and 32-bit CPUs. You can configure the addresses for either an A24 or A32 slave operation, and you can set the board's base address for any 4M-byte block within the VME Bus's 16M-byte (A24) or 4G-byte (A32) address range. $1485 (100).

SBE Inc, 2400 Bisso Lane, Concord, CA 94520. Phone (415) 680-7722. TWX 910-366-2116.

Circle No 379

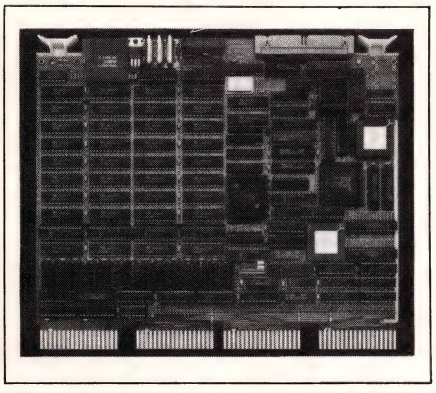
COMM CONTROLLER

- *Drives eight serial I/O ports*
- *Operates on the Multibus II bus*

Powered by an 80186 μP that runs at 8 MHz, the CD22/3800 provides eight serial I/O ports. Running in Multibus II-based computers, the board supports asynchronous and synchronous protocols, such as X.25 and SNA. Onboard memory includes 512k bytes of RAM and as many as 128k bytes of EPROM. Two iSBX connectors let you add daughter boards that support a variety of peripherals. Six ports operate with RS-232C signals, but you can configure two of the eight ports for either RS-422/449 or RS-232C signals. The board performs 8-, 16-, and 32-bit data-transfer operations; it runs self-diagnostic routines on power up. $2020 (100).

Central Data Corp, 1602 Newton Dr, Champaign, IL 61821. Phone (800) 482-0315; in IL, (217) 359-8010. TWX 910-245-0787.

Circle No 380



GRAPHICS CONTROLLER

- *Operates in Unibus or Q Bus computers*
- *Has an onboard 68010 CPU*

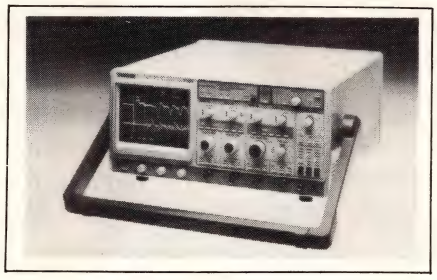
The VCK-Q/U graphics-controller board combines a 68010-based computer with a color-graphics controller. The controller includes features such as windows, zooming, panning, and vertical scrolling. The onboard computer provides 1M byte of RAM, high-speed DMA, serial I/O ports, and a SCSI interface for a dedicated hard disk. The board also includes 1M byte of video memory, two video-overlay memories, and 64k bytes of EPROM or RAM. The primary color display shows a 1024×1024-pixel area of 256 colors that you select from a 4096 or a 16-million color palette. The manufacturer presets the single quad-height board to operate on either DEC's Q Bus- or Unibus-based computers. From $4000. Delivery, 45 days ARO.

Peritek Corp, 5550 Redwood Rd, Oakland, CA 94619. Phone (415) 531-6500.

Circle No 381

NEW PRODUCTS

INSTRUMENTATION & POWER SOURCES



DIGITAL SCOPE

- *50M sample/sec digitizing rate*
- *Doubles as a 100-MHz analog scope*

The COM 7101 is a 4-channel, dual timebase digital oscilloscope that features a 50M-sample/sec digitizing rate. The instrument digitizes 100-MHz repetitive signals as well as 20-MHz transients. It provides a CRT readout of parameters. The device's built-in IEEE-488 interface bus provides full front-panel control and I/O of all CRT data; there are no keyboards and no menus. The device has an on-screen DVM and frequency counter. Other features include a 1k-sample memory on each of four channels, four 1k-sample reference memories, antialiasing circuits, and memory backup. You can also use the device as a 100-MHz analog oscilloscope. $5595.

Kikusui International, 19601 Mariner Ave, Torrance, CA 90503. Phone (800) 545-8784; in CA (213) 371-4662.

Circle No 382

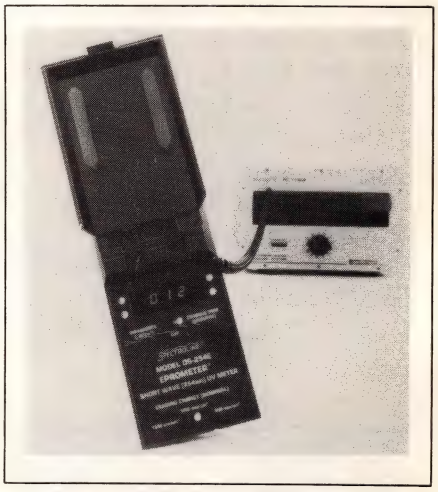
FILM RECORDER

- *Converts movie film to digital images*
- *Interfaces to common graphic terminals*

The CompactColor Model 635 produces digital images of 16- and 35-mm movie frames. The film recorder works with graphics workstations from Apollo, Chromatics, DEC, IBM, Ramtek, Raster Technologies, Seiko, Silicon Graphic IRIS Series, Sun, and Tektronix. The converter features raster blending for smooth lines and curves as well as automatic compensation for luminance changes. Its memory can store data for 24 film profiles. The unit measures 13×17.5×37.25 in. and weighs 135 lbs. $18,950. Delivery, 120 days ARO.

Dunn Instruments, 544 Second St, San Francisco, CA 94107. Phone (415) 957-1600.

Circle No 383



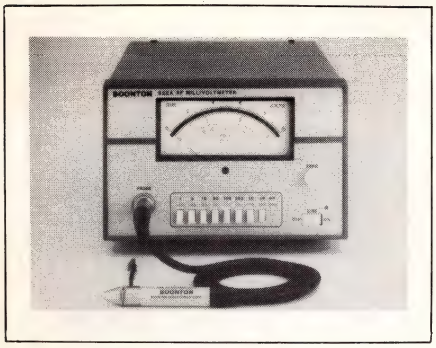
UV RADIOMETER

- *Panel shows erasing time in minutes*
- *Measures UV intensity with overall accuracy of ±5%*

The Model DS-254E Eprometer calculates the minimal erasure time for a given EPROM. When you select a value and insert the sensor in the eraser, the device's panel shows the erasing time in minutes on a 4½-digit LED digital display. The battery-operated device measures UV intensity with an overall accuracy of ±5% traceable to the National Bureau of Standards (NBS). The device reads from 0 to 19,990 $\mu W/cm^2$. $750.

Spectronics Corp, Box 483, Westbury, NY 11590. Phone (516) 333-4840. TWX 510-222-5877.

Circle No 384



RF VOLTMETER

- *Covers a frequency range from 10 kHz to 1.2 GHz.*
- *Has a mirror and a scale meter*

The Model 92EA RF voltmeter features sensitivity from 200 μV to 3V. The device's frequency ranges from 10 kHz to 1.2 GHz, and a terminated 50Ω BNC adapter accepts inputs over the entire range. The instrument has a large mirrored meter with two linear voltage scales and a dBm scale referred to 1 mW in 50Ω. A dBm scale referred to 75Ω and dBV and dBmV scales are optional. Model 92EA, $1760.

Boonton Electronics Corp, 791 Rte 10, Randolph, NJ 07869. Phone (201) 584-1077.

Circle No 385

RESPONSE ANALYZER

- *Shows high-resolution Bode and Nyquist displays*
- *Uses an IBM PC/XT*

The Model 350 frequency response analyzer system comprises an IBM PC/XT, a printer, a plotter, and frequency-response instrumentation. It features on-screen graphics displays in Bode or Nyquist format. The system covers 0.1 mHz to 1.0 MHz and has three input channels. For easy comparison, the circuit-analysis programs present data in the same format as measured data. The system comes with curve-fitting software that you can use to extract the poles and zeros from measured data. It can synthesize the optimal error-amplifier components required to stabilize any feedback loop at the crossover frequency and phase margin you desire. $26,800.

Venable Industries Inc, 3555 Lomita Blvd, Torrance, CA 90505. Phone (213) 539-2522. TLX 752421.

Circle No 386

NEW PRODUCTS

INTERNATIONAL

ANALOG I/O BOARD

- *Provides 12-bit resolution*
- *Has onboard, programmable gain and S/H amplifiers*

The SAN-32 is a double-Eurocard analog I/O board for use in STE Bus systems. You can configure the board to have 64 single-ended or 32 differential analog input channels. You can also configure as many as eight of the channels to operate as analog outputs capable of producing output voltages in the −10.24 to +10.24V range. You can monitor the output voltages by feeding them back to input channels. A/D conversion of the inputs and D/A conversion for the outputs is performed to 12-bit resolution (plus sign). On the standard board, the 12.5-μsec A/D converter allows conversion speeds as high as 100k samples/sec. A high-speed option reduces the conversion time to 5 μsec. A programmable gain amplifier provides input ranges from ±0.1 to ±10V full scale, and a sample/hold amplifier captures input signals in less than 1 μsec. Optional onboard sense resistors allow you to measure current inputs, and optional output circuitry allows you to generate 0- to 20-mA output currents. Another option allows you to use the board in a DMA mode. From £495 for an output-only board to £1250 for a fully populated version.

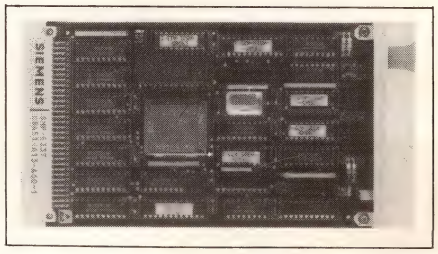
Kemitron Ltd, Hawarden Industrial Park, Manor Lane, Deeside, Clwyd CH5 3PP, UK. Phone (0244) 536123. TLX 61471.

Circle No 388

DMA BOARD

- *Transfers data as fast as 4M bytes/sec on four DMA channels*
- *Handles as many as eight interrupt sources*

The SMP-E337 is a DMA controller board you can use in 8-bit SMP Bus



industrial I/O computer systems. The board has four DMA channels. You can use one of the DMA channels in conjunction with an onboard interrupt controller to control interrupts from as many as eight peripheral devices. The board has a 1M-byte addressing range and can transfer data at rates as high as 4M bytes/sec. It operates with 8-MHz system clocks, and you can use as many as five wait cycles to accommodate memory and I/O accesses. A hold/hold-acknowledge interface allows you to daisy-chain as many as eight SMP-E337 boards. DM 1430.

Siemens AG, Zentralstelle für Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025.

Circle No 389

DYNAMIC RAM

- *CMOS RAM organized as 256k×4 bits*
- *Features 80-nsec access time*

The HM44258P2-8 is a 256k×4-bit CMOS dynamic-RAM module that features a row-address-strobe access time of 80 nsec and a cycle time of 151 nsec. You can operate the RAM with static-column addressing. In low-power standby mode, the module draws 10 mW. It's housed in a 22-pin single in-line package that has a maximum overall height of 0.35 in. £53.20 (1000).

Hybrid Memory Products Ltd, W Chirton Industrial Estate, North Shields, Tyne and Wear NE29 8SE, UK. Phone (091) 2580690. TLX 53206.

Circle No 390

VOLTAGE REFERENCE

- *Specs 35-ppm/°C typ temperature coefficient*
- *Output is unconditionally stable*

Housed in a SOT-23 package for surface mounting, the SR25D is a 2.5V precision bandgap reference. The device is unconditionally stable; it requires no external capacitor for stability. The output voltage has a nominal value of 2.5V ±2% and a typical temperature coefficient of 35 ppm/°C (70 ppm/°C max). The output's slope resistance is 1.2Ω typ. The device requires a current drive of 0.08 to 5 mA and has a typical knee current of 60 μA. £0.65 (100).

Ferranti Electronics Ltd, Fields New Rd, Chadderton, Oldham OL9 8NP, UK. Phone 061-624 0515. TLX 668038.

Circle No 391

Ferranti Electric Inc, 87 Modular Ave, Commack, NY 11725. Phone (516) 543-0200.

Circle No 392

IEEE-488 INTERFACE

- *Conforms to IEEE-488-1978 and IEEE-488A-1980 specifications*
- *Has four DMA channels*

Providing IEEE-488 bus talker, listener, and controller functions, the CC-91 double-Eurocard VME Bus board interfaces VME Bus systems to IEEE-488 bus instrumentation systems. The IEEE-488 interface is routed to standard IEEE-488 and IEC625 front-panel connectors, and to the board's P2 connector. The board has four DMA channels, two of which are dedicated to data transfers between the VME Bus and the IEEE-488 bus, and two of which are available for general VME Bus system use. The board has 23 address, 16 data, and 6 address-modifier lines, allowing it to address 16M bytes of VME Bus memory, and to transfer data between memory blocks with different address-modifier codes. The board generates interrupts when the IEEE-488 bus requires servicing. It also detects bus errors and generates appropriate error-interrupt vectors. In addition, the board has a VME Bus data-bus requester with a software-programmable request level. Gld 4250.

Compcontrol bv, Stratumsedijk 31, 5611 NB Eindhoven, The Netherlands. Phone (040) 124955. TLX 51603.

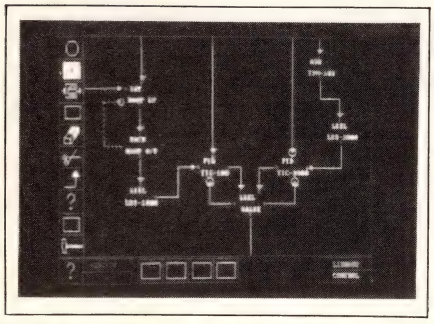
Circle No 393

Compcontrol Inc, 15466 Los Gatos Blvd, Suite 109-365, Los Gatos, CA 95030. Phone (408) 356-3817. TWX 510-601-2895.

Circle No 394

NEW PRODUCTS

SOFTWARE



PROCESS CONTROL

- *Mouse-driven module helps you design control strategies*
- *Allows you to use an IBM PC as a process-control station*

Paragon Control is a graphics software package that consists of two integrated modules: the icon-based Configurator and the real-time Run module. The package runs on the IBM PC/XT, PC/AT, and compatible computers. The controller allows a personal computer to function as a process-control station. You can graphically create and test control strategies, then connect the computer to I/O devices (single-loop controllers, PLCs, and plug-in I/O cards) for real-time process monitoring and control. Minimum requirements include 512k bytes of RAM, a 10M-byte hard disk, and MS-DOS 3.0 or higher. $5000.

Intec Controls Corp, Box 614, Mansfield, MA 02048. Phone (617) 543-4041.

Circle No 400

MODELING SYSTEM

- *Maintains a database of shapes*
- *Runs on workstations as well as the IBM PC/AT*

The Object-Oriented Graphical Modeling System of modules (OOGMS) provides more than 40 classes of objects for constructing graphics systems and lets you manipulate these objects on screen. The package runs on the IBM PC/AT and compatible machines, as well as on the MicroVAX II and on Apollo, Sun, and other engineering workstations. When you set the parametric limitations of models or submodels, the program preserves object-class control and still allows parametric variation in objects within those limitations. For hierarchical graphics modeling, display, and interaction, a system-function library (GMF) offers a set of functions written in C. The system's graphics language interpreter (GML) controls and animates the models you create. The object-oriented environment (OOE) has a hierarchical framework that organizes functions and provides run-time support. Finally, Draw is a high-level mouse- and icon-driven graphics editor and composer. The system provides an interface to low-level display packages, such as CGI (Common Graphics Interface), GKS (Graphical Kernel System), and VDI (Video Display Interface). Binary Draw module, $2500; complete package in binary form, $4500.

Sherrill-Lubinski, Hunt Plaza, #110, 240 Tamal Vista Blvd, Corte Madera, CA 94925. Phone (415) 927-1724.

Circle No 401

DATA ACQUISITION

- *Asyst interface combines analysis functions*
- *Can call subroutines from assembly-language code*

The PCI-20046S-5, a data-acquisition software package, combines Basic, C, Turbo-Pascal, and Asyst language interfaces for use with the company's PCI-20000 System (a hardware/software system that supports data-acquisition, test, measurement, and control instruments). When it's used with the PCI-20000 System and Asyst Modules 1 and 2 (from Macmillan Software), the Asyst language interface integrates analysis functions, including Fourier analysis, with graphics. Each language interface requires an IBM PC, PC/AT, PC/XT, or compatible computer and PC-DOS 2.0 or higher. The system can call all subroutines from assembly-language code. It also features thermocouple calls

and RTD linearization. The routines are written in machine language, so they optimize execution speed—you can take as many as 89,000 readings/sec with some hardware. $450.

Burr-Brown, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TWX 910-952-1111.

Circle No 402

ANALYSIS TOOL

- *Has a run-time program to write trace files*
- *Includes a utility for manipulating trace files*

TCAT (Test Coverage Analysis Tool) consists of a QuickBasic language system, a run-time program for collecting test-coverage data and writing trace files, and an analyzer that produces the coverage numbers. The analysis package provides a systematic procedure for checking all parts of a program and points out where new algorithms can improve the efficiency of the program. It helps you identify the parts of the code that have not yet been tested and the parts that are exercised frequently. The system provides support for releases 1.02 and 2.0 of Microsoft's QuickBasic. Single-CPU license, $2500; multiple-CPU license, $9000.

Software Research Associates, Box 2432, San Francisco, CA 94126. Phone (415) 957-1441. TLX 340235.

Circle No 403

LISP DEVELOPMENT

- *Links VAX Lisp to other programming tools*
- *Can operate in a computer network*

The AIT Lisp Toolkit helps in the development and delivery process of your Lisp program in a VAX/VMS system. It links VAX Lisp with other DEC-layered products, which include Rdb (Relational Database), GKS (Graphics Kernel System), FMS (Forms Management System), and Decnet. The package also links the VAX Lisp editor to the CMS (Code Management System) and MMS (Module Management System) locally or over a network. A natural-language processor and a windowing feature are part of the package. The software runs on VAX, MicroVAX, GPX, VAXstation II, and any AI workstation that runs VAX Lisp; it can also integrate the Automated Reasoning Tool (Art) from Inference Corp (Los Angeles, CA). From $6000.

Artificial Intelligence Technologies Inc, 1 Skyline Dr, Hawthorne, NY 10532. Phone (914) 347-6860.

Circle No 404

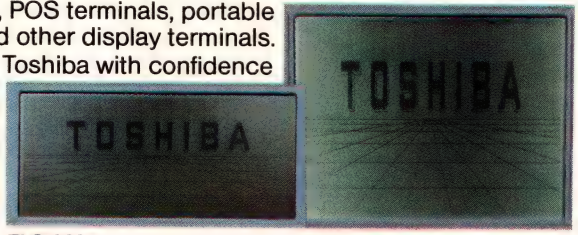
2,000 sharper-than-ever characters all on a portable LCD display.

Toshiba's newest LCD modules give you 640 × 200 dot displays in a choice of two viewing sizes. One is approximately the size of a magazine, and the other about half that size.

Both sizes put an enormous amount of information on view . . . an array of 80 characters × 25 lines. But still bulk and power consumption are at a minimum. Battery powered, these slim modules interface with various systems through LCD controller without renewing software.

Toshiba's advanced technology has also eliminated surface reflection and developed a sharper contrast which gives a brighter and easier to read viewing screen. And for low light or dark viewing an optional backlightable LCD is available.

These versatile LCDs are ideally suited for applications as displays for personal computers, POS terminals, portable word processors and other display terminals. You can also look to Toshiba with confidence for a wide range of sizes and display capacity to suit your LCD requirements.



TLC-363 *TLC-402*

Specifications

		TLC-402	TLC-363B
Display			
Number of Characters		80×25 (2,000 characters)	80×25 (2,000 characters)
Dot Format		8×8, alpha-numeric	8×8, alpha-numeric
Overall Dimensions (W × H × D)		274.8×240.6×17.0 mm	275.0×126.0×15.0 mm
Maximum Ratings			
Storage Temperature		−20° ~ 70° C	−20° ~ 70° C
Operating Temperature		0° ~ 50° C	0° ~ 50° C
Supply Voltage	V_{DD}	7 V	7 V
	$V_{DD} - V_{EE}$	20 V	20 V
Input Voltage		$0 \leq V_{IN} \leq V_{DD}$	$V_{SS} \leq V_{IN} \leq V_{DD}$
Recommended Operating Conditions			
Supply Voltage	V_{DD}	5±0.25V	5±0.25V
	V_{EE}	−11±3V Var.	−11±3V Var.
Input Voltage	High	V_{DD} − 0.5V min.	V_{DD} − 0.5V min.
	Low	0.5V max.	0.5V max.
Typical Characteristics (25°C)			
Response Time	Turn ON	300 ms	300 ms
	Turn OFF	300 ms	300 ms
Contrast Ratio		3	3
Viewing Angle		15 – 35 degrees	15 – 35 degrees

Design and specifications are subject to change without notice.

TOSHIBA

Toshiba America, Inc.: Electronic Components Business Sector: Head Office: 2692 Dow Avenue, Tustin, CA 92680, U.S.A. Tel. (714) 832-6300
Chicago Office: 1101 A Lake Cook Road, Deerfield, IL 60015, U.S.A. Tel. (312) 945-1500
Toshiba Europa (I.E.) GmbH: Electronic Components Div.: Hammer Landstrasse 115, 4040 Neuss 1, F.R. Germany Tel. (02101) 1580
Toshiba (UK) Ltd.: Electronic Components Div.: Toshiba House, Frimley Road, Frimley, Camberley, Surrey GU 165JJ, England Tel. 0276 62222
Toshiba Electronics Scandinavia AB: Vasagatan 3, 5 TR S-111 20 Stockholm, Sweden Tel. 08-145600

EDN PRODUCT MART

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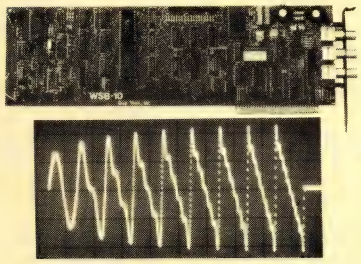

- For IBM-PC/XT/AT and compatibles
- Generates user-definable signal
- Up to 2000 points per envelope

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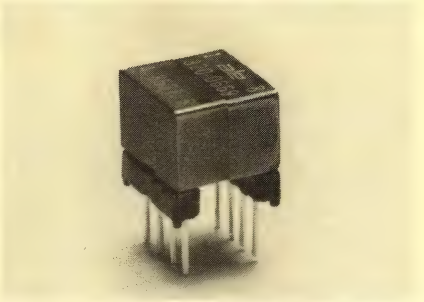

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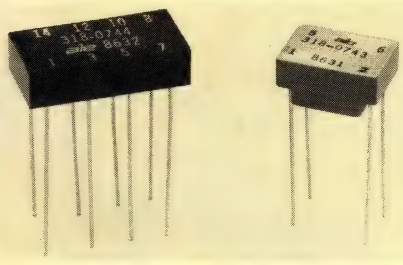

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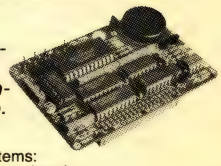

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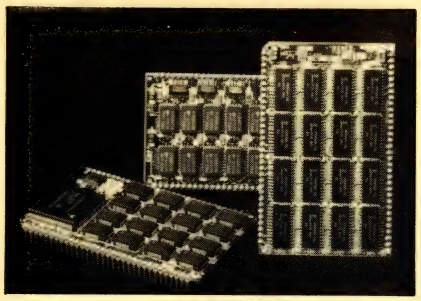

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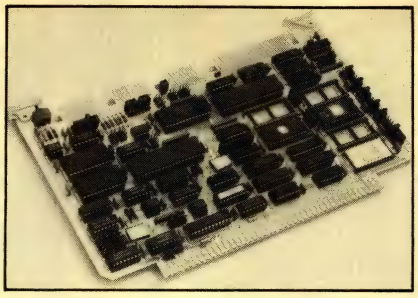

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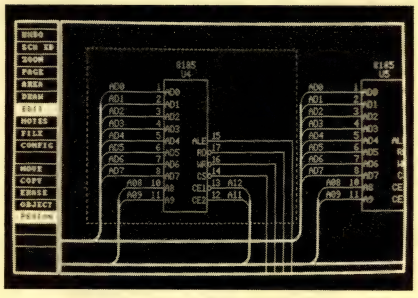

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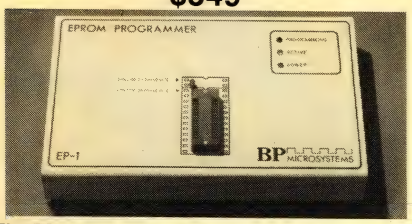

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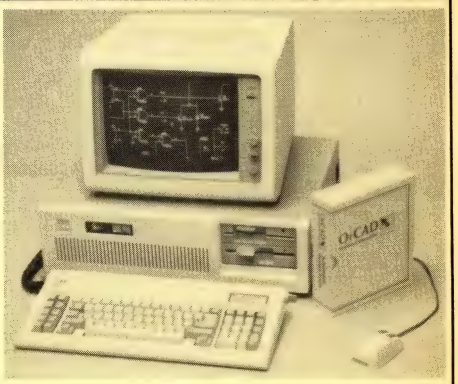

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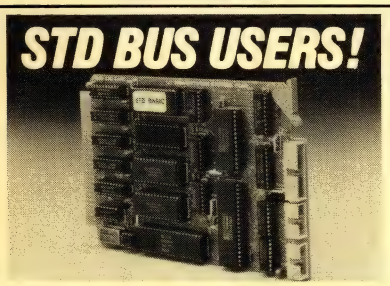

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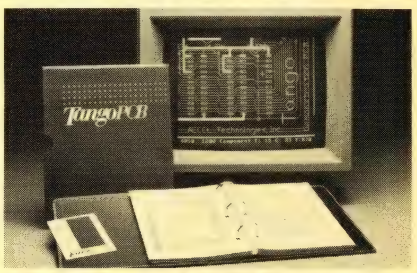

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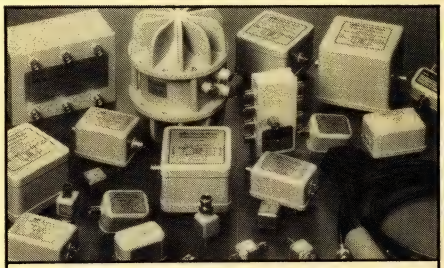

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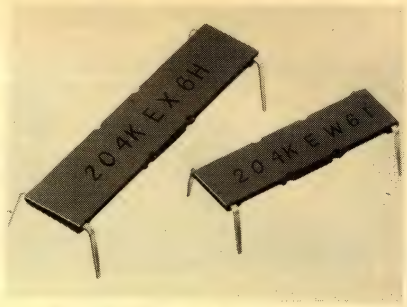

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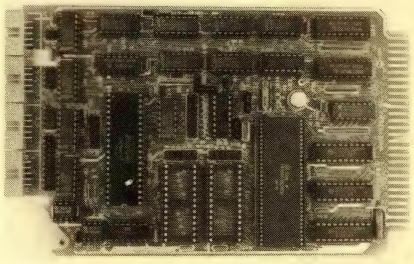

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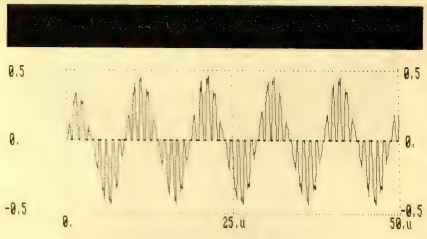

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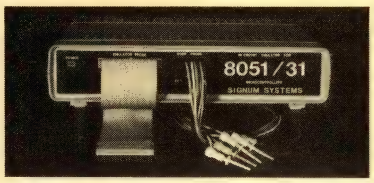

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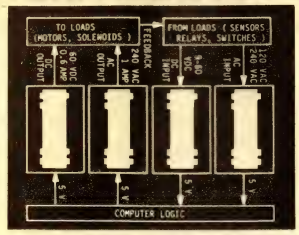

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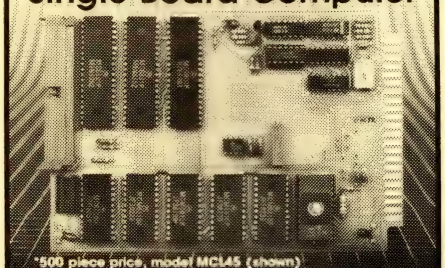

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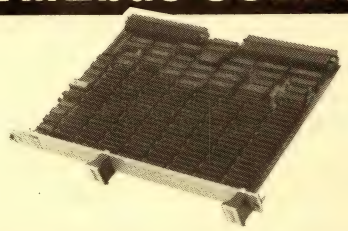

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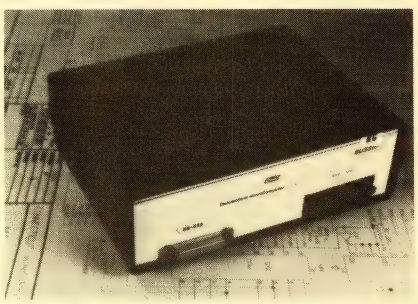

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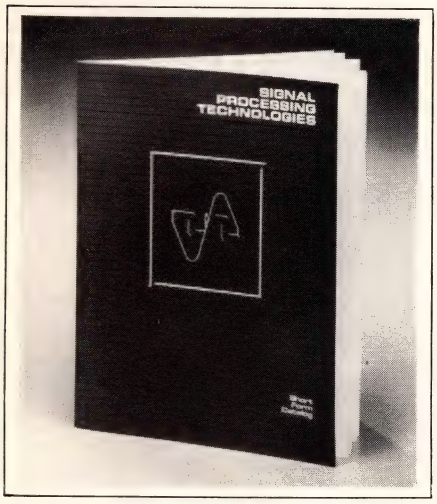


Catalog covers VLSI ICs

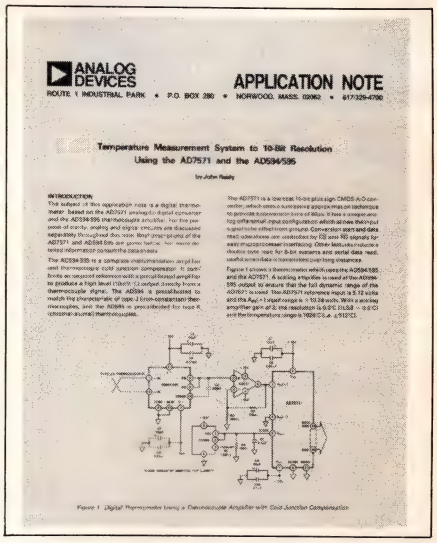
This short-form catalog describes the manufacturer's standard VLSI products, including D/A and A/D converters, comparators, and calibrators. The inside cover of the 24-pg booklet contains a tabular overview of the various product groups; following pages present the features, characteristics, interface circuits, and applications of each product. A final section addresses process capabilities (CMOS, BEMOS, digital bipolar, linear bipolar), packaging, testing, custom capabilities, and quality-assurance screening procedures.

Honeywell Inc, Signal Processing Technologies, 1150 E Cheyenne Mountain Blvd, Colorado Springs, CO 80906.

Circle No 405

App note for temperature-measurement system

This 4-pg application note details how to design a 10-bit, high-accuracy, temperature-measurement system. The digital thermometer system described is based on the AD7571 A/D converter and the AD594/595 thermocouple amplifier. The note outlines two techniques for computing and displaying data. In one method, a digital thermometer


ANALOG DEVICES

APPLICATION NOTE

Temperature Measurement System to 10-Bit Resolution
Using the AD7571 and the AD594/595

by John Reddy

INTRODUCTION

that provides a nonlinear output and has a resolution of 0.5°C and a temperature range of ±512°C uses a thermocouple with cold-junction compensation. In the second method, a digital thermometer uses an EPROM for linearization; the AD7571 operates in the ROM mode, and a 2716 EPROM performs the

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I certify that the statements made by me above are correct and complete. Robert LaFemina, (signed) Manager, Administrative Services.

linearization and binary-to-BCD conversion. The note also contains schematics and comparison tables.

Analog Devices, Literature Ctr, 70 Shawmut Rd, Canton, MA 02021.

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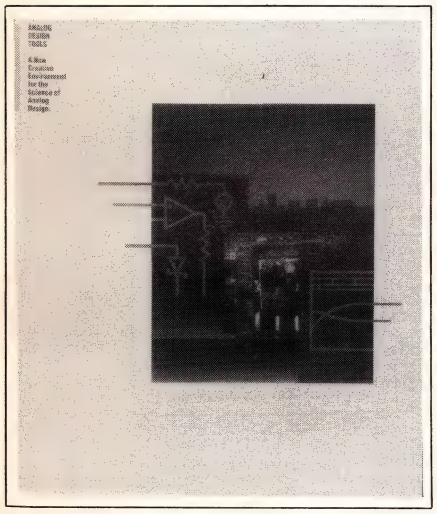

Brochure and videotape highlight CAE tools

This 8-pg brochure on the Analog Workbench family of CAE tools for analog-circuit design is complemented by an 8-minute product-demonstration videotape (in VHS format). Analog Workbench is a set of integrated software modules that runs on Sun, Apollo, and HP workstations and the IBM PC/AT. The 4-color brochure covers the modules' use of simulated instruments (eg, oscilloscopes and spectrum and network analyzers), and Spice Plus simulation software. And, it describes software options for power-supply design, safe-operating-area analysis, statistical analysis, and parametric plotting.

Analog Design Tools Inc, 66 Wilbur Pl, Menlo Park, CA 94025.

Circle No 407

Catalog of CMOS ICs

This catalog describes the manufacturer's family of high-speed CMOS components suitable for real-time DSP and general-computing applications. Products covered include multipliers, multiplier accumulators, pipeline registers, register files, ALUs, and special-purpose components (for example, a 32-bit, cascadable barrel shifter/normalizer and a 64×1-bit digital correlator). The catalog features functional and timing diagrams, pinout-configuration tables, charts of electrical-performance and switching characteristics, and data on absolute maximum ratings and recommended operating conditions. It also includes technical articles and application notes.

Logic Devices Inc, 628 E Evelyn Ave, Sunnyvale, CA 94086.

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BUSINESS/CORPORATE STAFF

F Warren Dickson
Vice President/Publisher
Newton, MA 02158
(617) 964-3030
Telex 940573
Diann Siegel, Assistant

Peter D Coley
Associate Publisher/
Advertising Sales Director
Newton, MA 02158
(617) 964-3030
Stacey Vorias, Assistant

NEW ENGLAND
Bob Sommer, Regional Manager
275 Washington St
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Your Career: Taking Stock

Sanford Rose, *Sanford Rose Associates*

Among all the advice on career management that's available in scores of books and magazine and newspaper articles, one truism stands out: Self-help pays off. Yet despite the considerable rewards of continual self-evaluation and career planning, it's easy for most people, when they find a comfortable job, to settle in and simply do their work.

But too much comfort on the job can backfire. Once professionals become fixed in the "comfort zone," their motivation to change, and their perception of events that forecast or mandate change, diminishes. In the electronics industry, however, change is inherent. Engineers' jobs in particular are subject to the ramifications of sweeping technological shifts and a fluctuating job market. Consequently, engineers who are unprepared for changes and who overestimate the security of their jobs risk losing control of their careers.

Overly dependent employees, in fact, may find that their lack of career initiative costs them their jobs. Recent mass layoffs in the electronics industry prove that employees can't leave responsibility for their careers to their employers. Assuming that your employer will always reward good performance, for example, can leave you professionally vulnerable. One engineer, who agreed to manage the 2-year closing of one of his employer's facilities, was terminated after completing the job, even though the closing had proceeded in a smooth and orderly fashion. The engineer hadn't recognized that by accepting a short-term position with only caretaking responsibilities, he had essentially phased himself out of a more active position with his employer.

To avoid career complacency and to stay abreast of the factors stimulating change, you should take an annual inventory of your career. Your inventory's starting point should be a determination of your short- and long-term career goals. What do you want from your career? Are you still following your original career goals, or have your goals changed? Examine the abilities that determine your value to your present employer and to a prospective one. Do you need to take some technical courses to bring your technical skills up to date? Do you have latent abilities that you can develop to further your career?

Continue your inventory by measuring your progress at the company against that of your colleagues. Are you leading the pack, trailing it, or just keeping pace? When considering your progress, you must also ask whether your employer offers the kinds of opportunities that you need to reach your career goals.

Investigation of your goals must proceed along with an investigation of the development of your skills. How do you and your associates perceive your job performance? What are your strengths and weaknesses? Are you in the forefront of your company's technical work, or are you in the "comfort zone?" Will you advance in your present job? If you work for a large company, are there job possibilities for you in another department or division of your company? Ask your manager for an evaluation of your work and a frank appraisal of your future at your company.

Next, analyze the opportunities that exist in the marketplace for a person with your experience and education. What types of jobs fit your skills and are consistent with your career goals? The most obvious opportunities to consider are those at other companies in the electronics industry, but don't limit your analysis to just these outlets. Switching to another industry isn't always as difficult as it appears. Many manufacturing sectors, such as the automotive and instrumentation industries, now use technologies that were once found, say, only in the computer-hardware field.

Technical skills are at a premium in these industries, and employers needing talented managers and administrators are more interested in finding people with the right capabilities than in hiring from within

Set your professional priorities

When evaluating your professional goals and your career's progress, you can often clarify your thoughts by listing the job factors you consider important, giving them a numerical ranking, and then determining the factors that are lacking in your job and those that you want to ensure you find in your next career move. The **chart** can help you conduct such an exercise.

In the left-hand column, assign each job element a number from one to 21 according to the element's importance to you. Assign a "21" to the most important factor, "20" to the second most important factor, and so on. Do not use any number twice.

In the columns labeled "present job" and "proposed job," split the point total for each job factor between the two columns. For example, if "climate and location" rates a 3 in the first column, and you're satisfied with your current location, then enter a "3" in the "present job" column and a "0" in the "proposed job" column. If you assigned "income growth" an ideal ranking of 15, but you believe your present job only moderately satisfies this need, you might enter a "6" in the second column and a "9" in the third column.

The completed ranking in the third column gives you an idea of the changes in your situation that most need attention. Keep in mind that a ranking of 0 in the third column is not an indication that the associated job factor is not important to you; change is the key idea. Those elements that have the highest numbers assigned to them in the last column are going to be job factors that are important to you but unsatisfactorily met in your present job.

IMPORTANCE FACTOR	ELEMENT	PRESENT JOB	PROPOSED JOB
	INCOME GROWTH		
	LONGEVITY IN EMPLOYMENT		
	EMPLOYER STABILITY		
	EMPLOYER PROGRESSIVENESS		
	PROMOTIONAL OPPORTUNITIES		
	AN AUTHORITY IN MY FIELD		
	TRUST IN MANAGEMENT		
	RECOGNITION OF MY ABILITIES		
	QUALITY OF COLLEAGUES		
	INVOLVEMENT WITH STATE OF ART		
	UTILIZATION OF EDUCATION AND EXPERIENCE		
	FREEDOM TO EXERCISE INITIATIVE		
	FREEDOM FROM ROUTINE CHORES		
	PROFESSIONAL PRACTICE GROWTH		
	MANAGEMENT OR SUPERVISORY GROWTH		
	SATISFACTION FROM WORK		
	ONGOING PROFESSIONAL EDUCATION		
	SPOUSE'S PROFESSIONAL CAREER		
	FAMILY CONCERNS		
	HOBBIES AND OUTSIDE INTERESTS		
	CLIMATE AND LOCATION		

their own industry. For example, one design engineer working in the computer industry accepted a job in the automotive industry and received a substantial salary increase. In his new job, he became involved in designing computerized automatic test equipment that auto mechanics use to diagnose vehicular performance problems at dealer service centers.

Compare the opportunities available in other companies with those at your present employer. The economic outlook for a company and its industry should be part of any consideration. Keep in mind that growing companies usually offer more potential for career advancement, but that small, start-up companies give engineers even more technical opportunities.

For example, after merging with a large, multinational corporation, an electronics company planned to phase out one of its product lines over the next five years and then relocate the division that had responsibility for the product. The company offered the position of division manager—a well-paid, comfortable job with decreasing responsibilities over the 5-year period—to one of its engineers. Instead of taking the position, however, the engineer and five associates negotiated a license for the technology that the company intended to phase out. The group formed a new company, which is now so successful that the group plans to make a public stock offering.

If an inventory of your career begins to show that a job change would best further your career goals, then you should begin immediately to seek interviews with the companies you've targeted as having good job opportunities. Respond to recruiting advertisements in trade journals and newspapers. Be receptive to employment recruiters who contact you. Attend career fairs geared to technical personnel, and register with technical employment services.

By conducting your annual career inventory honestly and thoughtfully, you'll know whether you're ready to deal with change, whether it's necessary, and what you must do personally and professionally to come to terms with it. Even if your current job appears to be leading you toward your goals, you owe it to yourself to re-examine your career annually so that you're prepared for change.

Even if your current job appears to be leading you toward your goals, you owe it to yourself to re-examine your career annually so that you're prepared for change.

Change can be exciting and rewarding and add new zest to people's lives both on and off the job. All it takes is a positive outlook and the will to prepare for it. **EDN**

Author's biography

Sanford Rose is the chief executive officer of Sanford Rose Associates, an Akron, OH-based recruiter of technical personnel. Rose holds a degree in industrial management from Ohio State University. He is a member of the IEEE and the National Association of Personnel Consultants.

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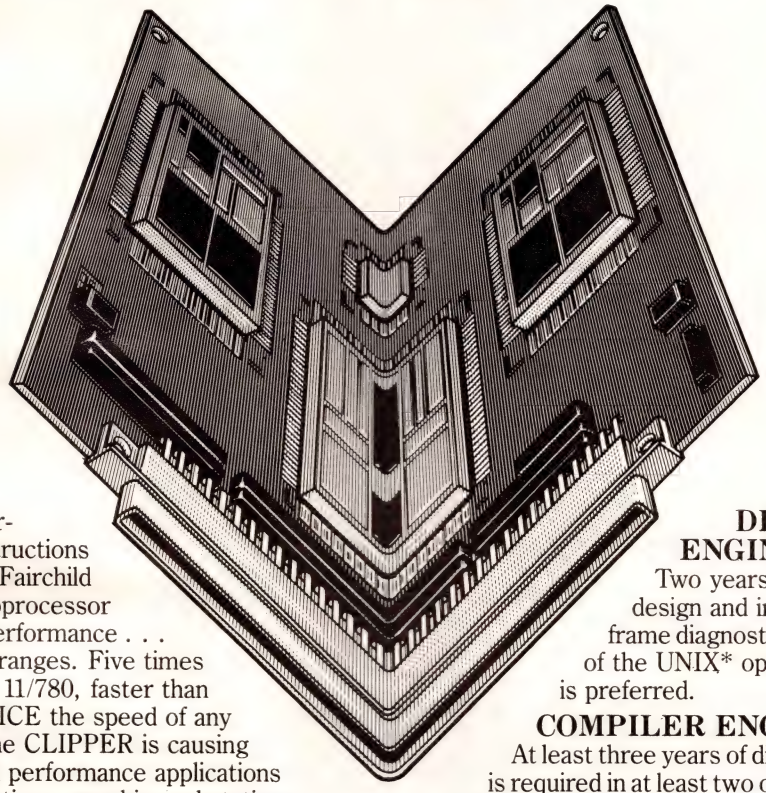

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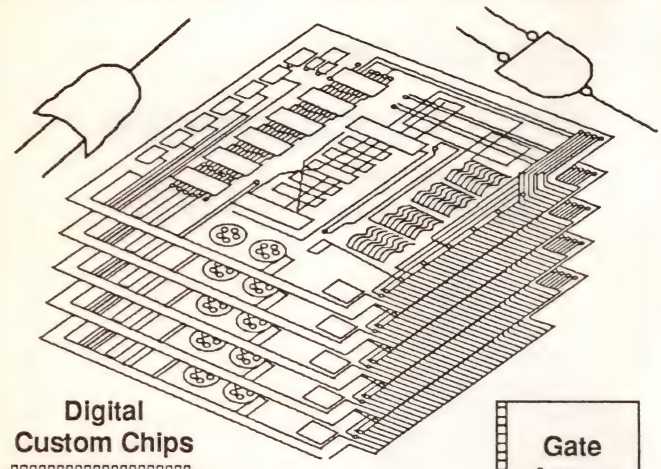

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Degrees (List)	Major Field	GPA	Year Degree Earned	College or University

POSITION DESIRED

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EXPERIENCE

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Duties and Accomplishments: Industry of Current Employer:

_____

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_____

Reason for Change: _____

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Job Title: _____
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Duties and Accomplishments: _____

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LOOKING AHEAD

EDITED BY GEORGE STUBBS

WORLDWIDE GaAs IC MARKET
(MILLIONS OF UNITS)

	1986	1987	1988	1989	1990
USA	103	153	226	338	506
EUROPE	6	28	50	90	163
JAPAN	15	30	60	121	243
TOTAL	124	211	336	549	912

(SOURCE: HTE MANAGEMENT INC)

GaAs IC market: Slower growth than expected

Gallium arsenide—the IC material that promises extremely high speeds, low power consumption, and submicron geometries—has been on the edge of revolutionizing the semiconductor industry for some time. Manufacturers and market forecasters have repeatedly hailed the imminent transformation of many segments of the electronics industry as a result of the advantages GaAs can bring. But it's time to exhale a bit.

Market-research companies are now starting to trim bloated forecasts of GaAs market growth by as much as half (see "Looking Ahead," EDN, April 3, pg 291). For example, HTE Management Inc (Scotts Valley, CA) is predicting a $912 million worldwide market for GaAs ICs in 1990. Integrated Circuit Engineering Corp (ICE) (Scottsdale, AZ) is even more conservative, projecting a $525 million market in 1990 and a $950 million market in 1991. Both HTE and ICE foresee a steady growth rate, but one that's slower than previous predictions cited.

Both research companies also suggest that GaAs is a technology still waiting for a set of applications that can exploit its potential and thus be worth the higher costs. Many of the projected applications for GaAs ICs "have yet to materialize with the breadth and depth necessary to ensure commercial viability," say HTE researchers. ICE echoes this concern: "Even if a manufacturer can make a GaAs IC [for] a reasonable price, the market must be developed for the component."

HTE also notes that progress in silicon technology, particularly ECL, is nudging aside GaAs for certain high-speed applications. Current ECL ICs rival the performance of depletion-mode GaAs ICs in the 1-GHz region of operation (see "High-speed logic ICs," EDN, August 21, pg 112). Both HTE and ICE believe that the truly substantial market growth for GaAs ICs will occur in the early 1990s.

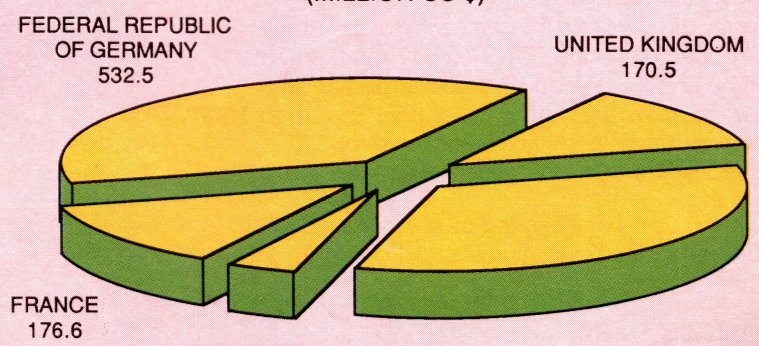
Use of position sensors to double in Europe by '95

Demand on the part of European nations for position sensors will double over the period extending from 1985 to 1995, according to the market-research company Frost & Sullivan Inc (F&S) of New York, NY. Sales of the devices in Europe, measured in constant 1985 US dollars, totaled $695 million in 1985. In 1995, that total should reach $1.4 billion; leading the market is Germany, with a projected $532.5 million in sales for that year.

Robotics applications account for only 5% of the use of the devices, according to F&S. Typical applications of position sensors range from the laying of guns in tank turrets to the physical control of pallets in materials handling. Indeed, materials handling accounts for the same percentage of the market as the military/aerospace sector does; each represents 15% of the total demand for position sensors in Europe. Use of the devices in the military/aerospace sector, however, is expected to grow at a faster rate.

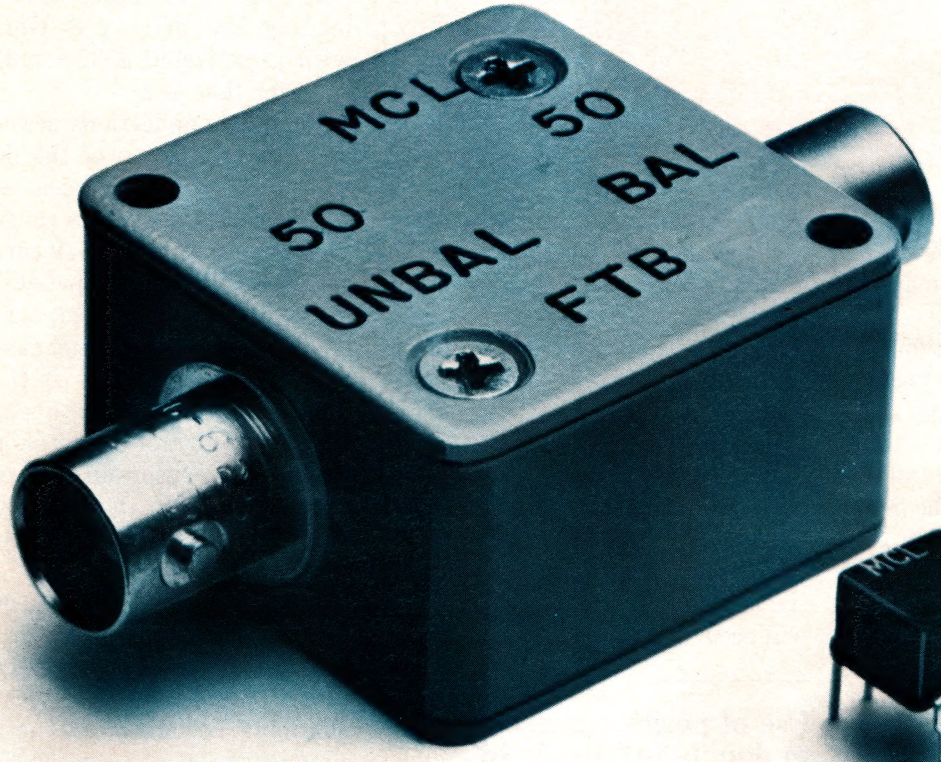
In France and the UK, position sensors are most frequently used in military and aerospace applications. In the UK, use of the devices is also particularly heavy in the petrochemical industry. In the Federal Republic of Germany, machine-tool demand for position sensors predominates over other uses, followed by materials handling.

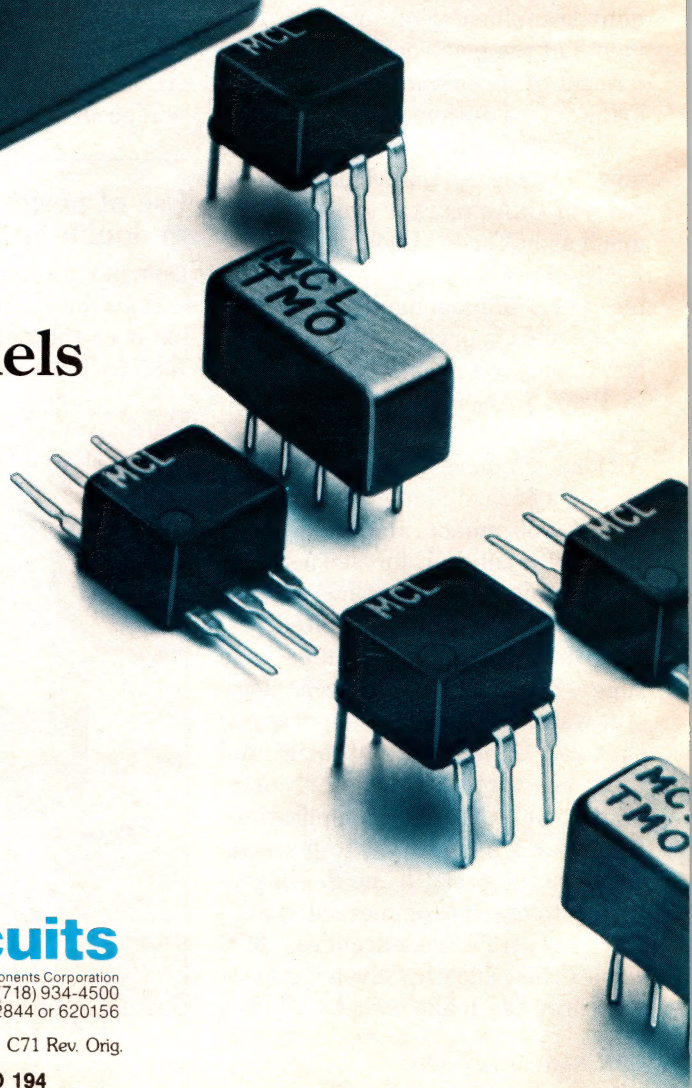
1995 EUROPEAN POSITION-SENSOR DEMAND BY COUNTRY
(MILLION US $)



(SOURCE: FROST & SULLIVAN INC)

RF transformers





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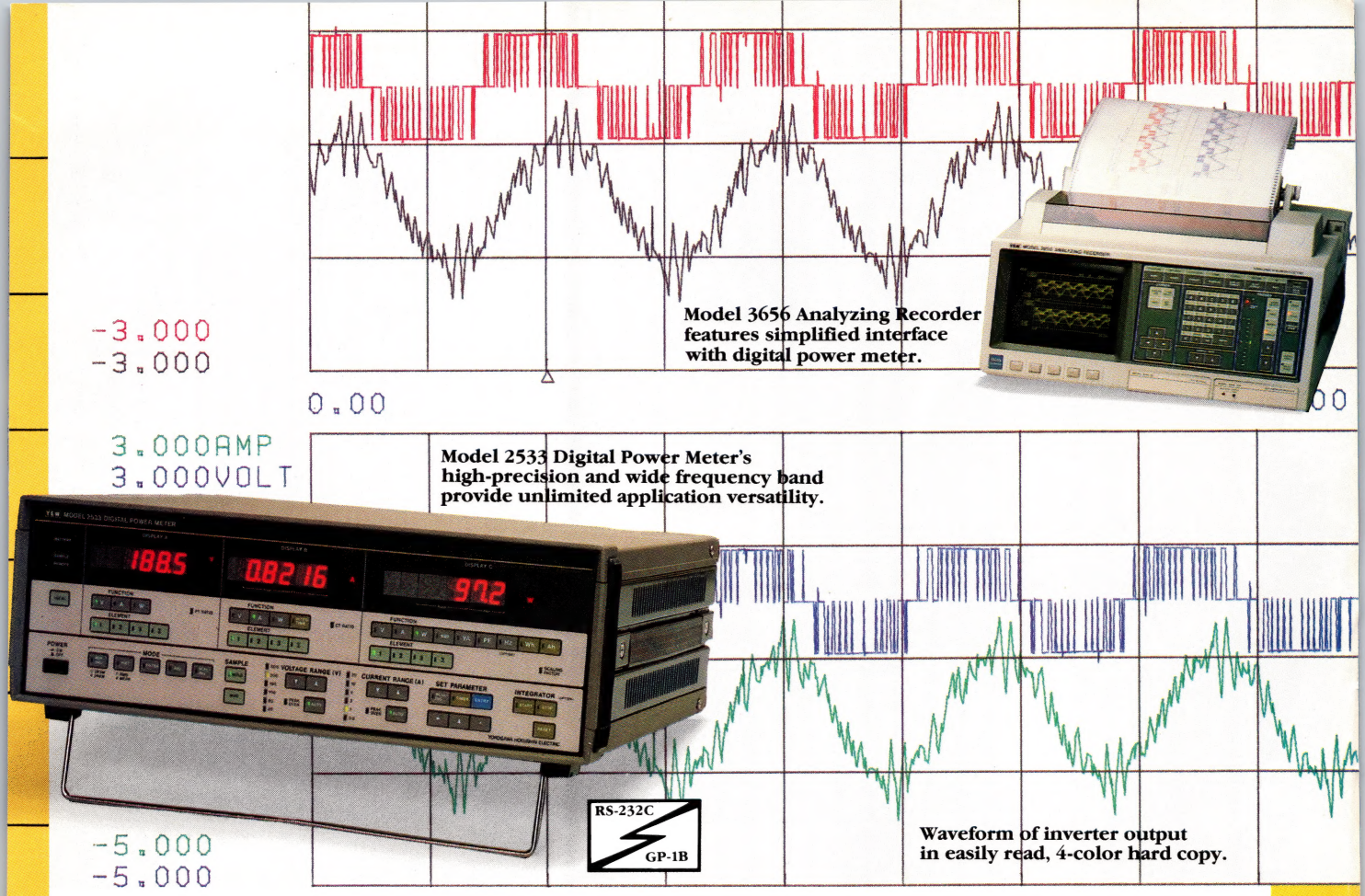

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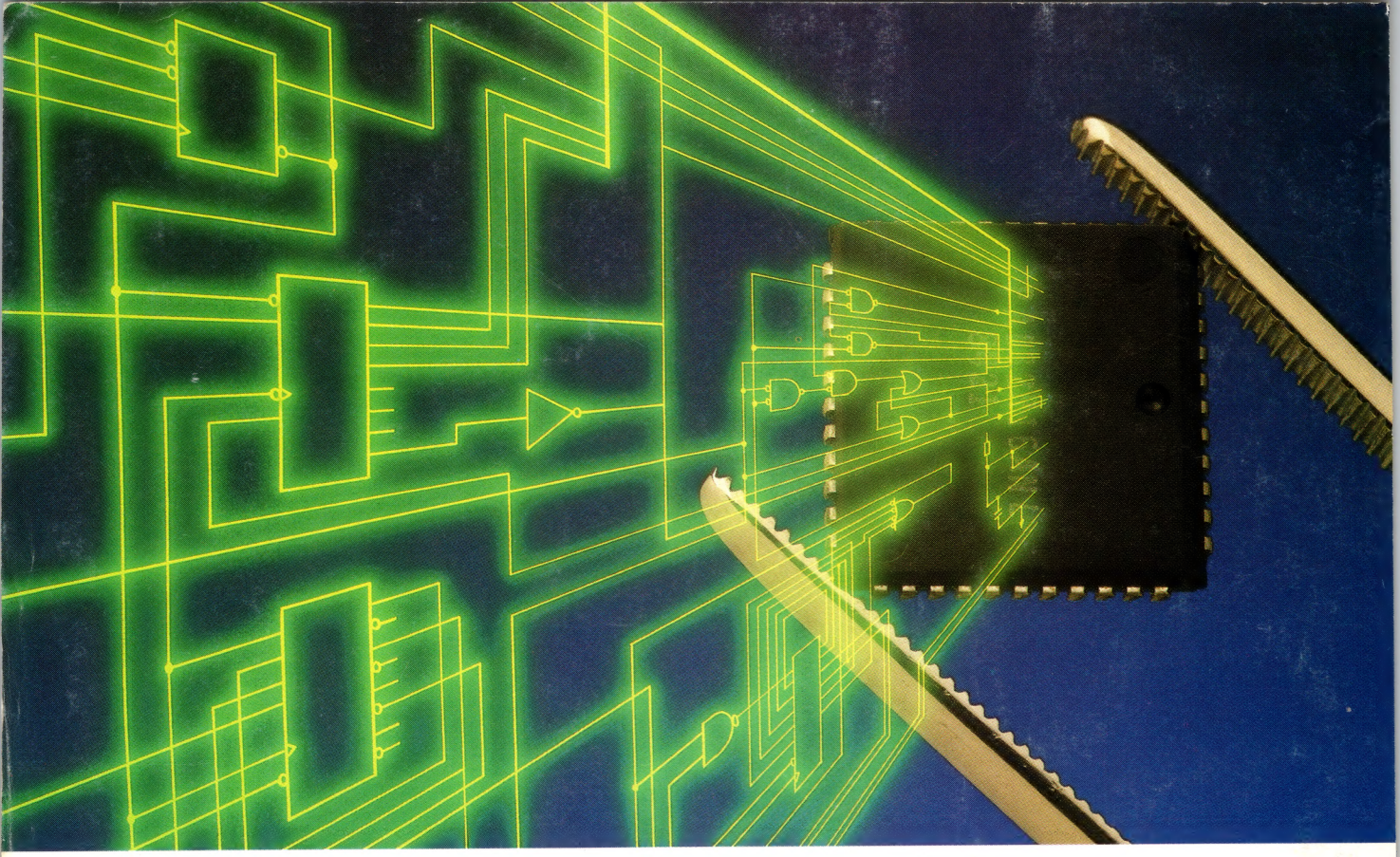

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